NCV885300

Automotive Grade Non-Synchronous Buck Controller

The NCV885300 is an adjustable−output non−synchronous buck controller which drives an external P−channel MOSFET. The device uses peak current mode control with internal slope compensation. The IC incorporates an internal regulator that supplies charge to the gate driver.

Protection features include internal soft−start, undervoltage lockout, cycle−by−cycle current limit, hiccup−mode overcurrent protection, hiccup−mode short−circuit protection.

Additional features include: power good signal, low quiescent current sleep mode and externally synchronizable switching frequency.

Features

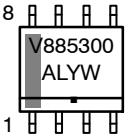
- Ultra Low Iq Sleep Mode
- Adjustable Output with 800 mV ±2.0% Reference Voltage
- Wide Input of 3.1 to 44 V with Undervoltage Lockout (UVLO)
- Power Good (PG)
- Internal Soft−Start (SS)
- Fixed−Frequency Peak Current Mode Control
- Internal Slope Compensating Artificial Ramp
- Internal High−Side PMOS Gate Driver
- Regulated Gate Driver Current Source
- External Frequency Synchronization (SYNC)
- Programmable Cycle−by−Cycle Current Limit (CL)
- Hiccup Overcurrent Protection (OCP)
- Output Short Circuit Hiccup Protection (SCP)
- Space−Saving 8−PIN SOIC Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

ON Semiconductor®

http://onsemi.com

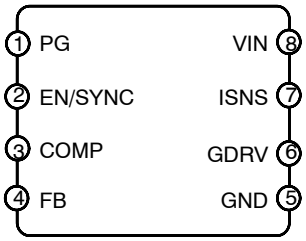
MARKING DIAGRAM

SOIC−8
SUFFIX D
CASE 751



V885300 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCV885300D1R2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

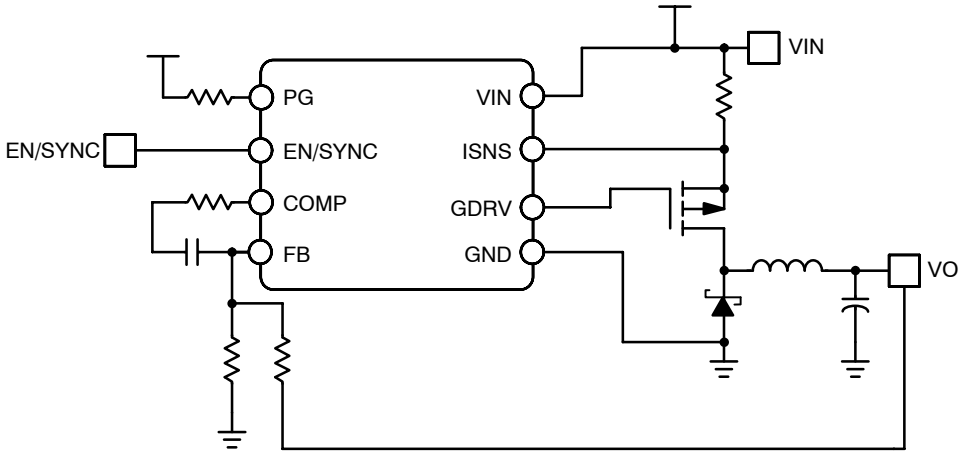


Figure 1. NCV885300 Application Diagram

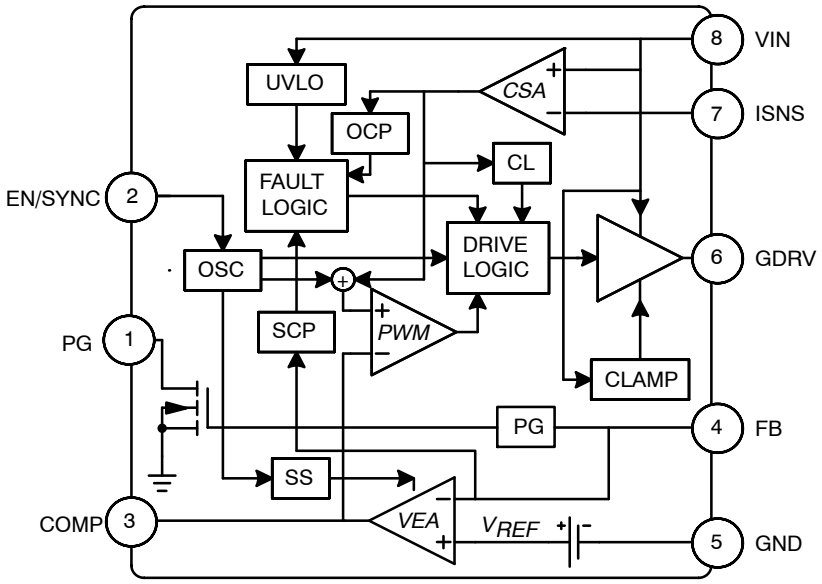


Figure 2. NCV885300 Simple Block Diagram

PIN DESCRIPTIONS

No	Pin Symbol	Function
1	PG	Power good output. Use a pull−up resistor to 5.0 V. PG is pulled low when power is not good.
2	EN/SYNC	Enable and synchronization input. The falling edge synchronizes the internal oscillator. The part is disabled into sleep mode when this pin is brought low for longer than the enable time−out period.
3	COMP	Output of the voltage error amplifier. An external compensator network from COMP to GND is used to stabilize the converter and tailor transient performance.
4	FB	Output voltage feedback. A resistor from the output voltage to FB with another resistor from FB to GND creates a voltage divider for regulation and programming of the output voltage.
5	GND	Ground reference.
6	GDRV	Gate driver output. Connect to gate of the external P−channel MOSFET. A series resistance can be added from GDRV to the gate to tailor EMC performance.
7	ISNS	Current sense input. Connect this pin to the source of the external P−channel MOSFET, through a current−sense resistor to VIN to sense the switching current for regulation and current limiting.
8	VIN	Main power input for the IC.

MAXIMUM RATINGS (Voltages are with respect to GND unless otherwise indicated.)

Rating	Value	Unit
DC Voltage (VIN, ISNS, GDRV)	−0.3 to 44	V
Peak Transient Voltage (Load Dump on VIN)	44	V
DC Voltage (EN/SYNC, PG)	−0.3 to 6.0	V
DC Voltage (COMP, FB)	−0.3 to 3.6	V
DC Voltage Stress (VIN − GDRV)	−0.7 to 12	V
Operating Junction Temperature Range	−40 to 150	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Pb−Free 60 to 150 seconds at 217°C	265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

PACKAGE ATTRIBUTES

Characteristic	Value
ESD Capability Human Body Model Machine Model Charge Device Model	 2.0 kV 200 V >1.0 kV
Moisture Sensitivity Level	MSL 1 260°C
Package Thermal Resistance Junction−to−Ambient, $R_{\theta JA}$	 100°C/W

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 3.4 V < V_{IN} < 36 V, EN = 5 V, no sync, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Quiescent Current	$I_{q,sleep}$	V_{IN} = 13.2 V, EN = 0 V, Sleep Mode		2.5	6.0	μA
	$I_{q,off}$	V_{IN} = 13.2 V, EN = 5 V or toggled, V_{FB} = 1 V, No Switching		2.0	3.0	mA
	$I_{q,on}$	V_{IN} = 13.2 V, EN = 5 V or toggled, V_{FB} = 0 V, Switching		3.0	5.0	mA
Undervoltage Lockout	V_{uvlo}	V_{IN} decreasing	2.9	3.1	3.3	V
Undervoltage Lockout Hysteresis	$V_{uvlo,hys}$		50	150	300	mV
Overvoltage Lockout	V_{ovlo}		36.9	38	39.3	V
OSCILLATOR						
Switching Frequency	F_{SW}		306	340	374	kHz
Slope Compensation	m_a			51		mV/μs
Minimum On Time	t_{onmin}		90	110	140	ns
Minimum Off Time	t_{offmin}			93		%
Max Duty Cycle	D_{max}			100		%
Soft−Start Time	t_{ss}		1.0	1.5	2.0	ms
Soft−Start Delay	$t_{ss,dlly}$		200	300	400	μs
EN/SYNC						
Low Threshold	$V_{s,il}$				0.8	V
High Threshold	$V_{s,ih}$		2.0			V
Input Current	I_{sync}			5.0	10	μA
SYNC Frequency Range	f_{sync}	Relative to Nominal Switching Frequency	80		300	%
SYNC Delay	$t_{s,dly}$	From SYNC falling edge to GDRV falling edge		50	100	ns
SYNC Duty Cycle	D_{sync}		25		75	%
Disable Delay Time	t_{en}	% of F_{SW}		300		%
POWER GOOD						
Rising Threshold	PG_{rise}	% of V_{ref}	87	90	93	%
Falling Threshold	PG_{fall}	% of V_{ref}	90	93	96	%
Power Good Pulldown	V_{pg}				0.40	V
VOLTAGE ERROR AMP						
DC Gain	A_v		55	80	91	dB
Gain−Bandwidth Product	G_{BW}		1.7	2.4	3.1	MHz
FB Bias Current	$I_{vfb,bias}$			0.1	1.0	μA
Charge Currents	$I_{src,vea}$	Source, V_{FB} = 0.9 V, V_{COMP} = 1.2 V	1.2	1.8	2.5	mA
	$I_{snk,vea}$	Sink, V_{FB} = 0.7 V, V_{COMP} = 1.2 V	0.5	0.8	1.0	
Reference Voltage	V_{ref}		784	800	816	mV
High Saturation Voltage	$V_{c,max}$		2.2	2.3		V
Low Saturation Voltage	$V_{c,min}$			0.001	0.3	V
CURRENT SENSE AMP						
Common−Mode Range	CMR		3.1		40	V
Differential Mode Range	DMR		300			mV
Amplifier Gain	A_{csa}			2.0		V/V
Input Bias Current	$I_{sns,bias}$			30	50	μA

ELECTRICAL CHARACTERISTICS

(−40°C < T_J < 150°C, 3.4 V < V_{IN} < 36 V, EN = 5 V, no sync, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT LIMIT / OVER CURRENT PROTECTION						
Cycle−by−Cycle Current Limit Threshold	V_{cl}		85	100	115	mV
Cycle−by−Cycle Current Limit Response Time	t_{cl}				200	nsec
Over Current Protection Threshold	V_{ocp}	% of V_d	125	150	175	%
Over Current Protection Response Time	t_{ocp}				200	ns
GATE DRIVERS						
Leading Edge Blanking Time	$t_{on,min}$				100	ns
Gate Driver Pull Up Current	I_{sink}	V_{IN} − V_{GDRV} = 4 V		200	300	mA
Gate Driver Pull Down Current	I_{src}	V_{IN} − V_{GDRV} = 4 V		200	300	mA
Gate Driver Clamp Voltage (V_{IN} − V_{GDRV})	V_{drv}		6.0	8.0	10	V
Power Switch Gate to Source Voltage	V_{gs}	V_{IN} = 4 V	3.8			V
SHORT CIRCUIT PROTECTION						
Startup Blanking Time	$\%t_{scp,dly}$	From start of soft−start, percent of soft−start time	105		300	%
Short−Circuit Threshold Voltage	$\%V_{scp}$		65	70	75	%
Hiccup Time	$t_{hcp,dly}$	(% of Soft−Start Time)		135		%
SC Response Time	t_{scp}	Switcher Running		60	200	ns
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{sd}	T_J rising	160	170	180	°C
Thermal Shutdown Hysteresis	$T_{sd,hys}$	T_J Shutdown − T_J Startup	10	15	20	°C
Thermal Shutdown Delay	t_{tsd}	T_J > Thermal Shutdown Threshold to stop switching			200	ns

TYPICAL CHARACTERISTICS CURVES

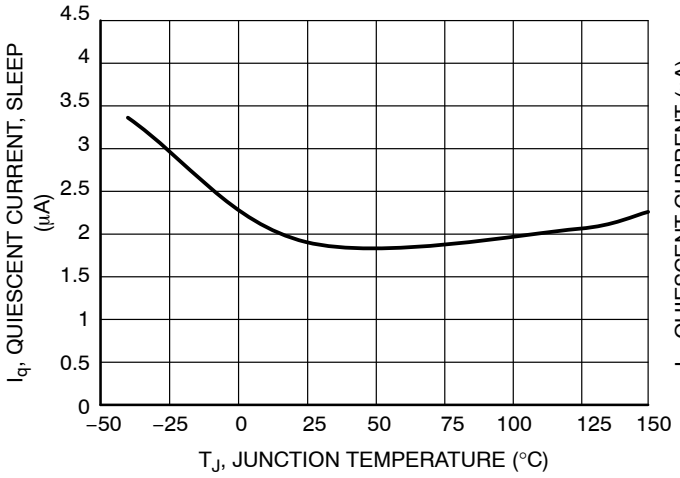


Figure 3. Quiescent Current (Sleep) vs. Junction Temperature

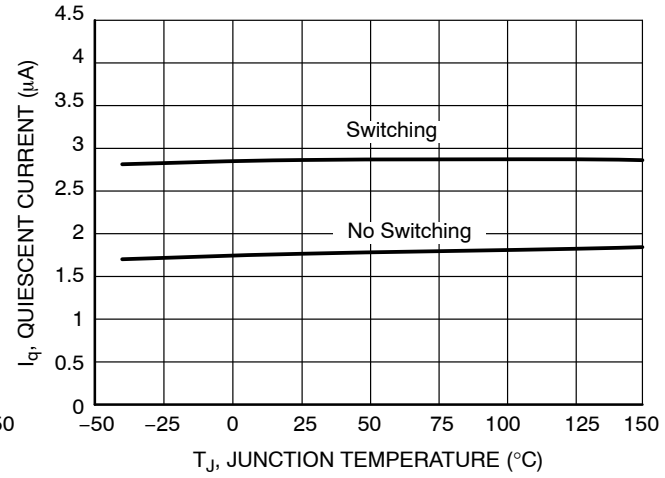


Figure 4. Quiescent Current vs. Junction Temperature

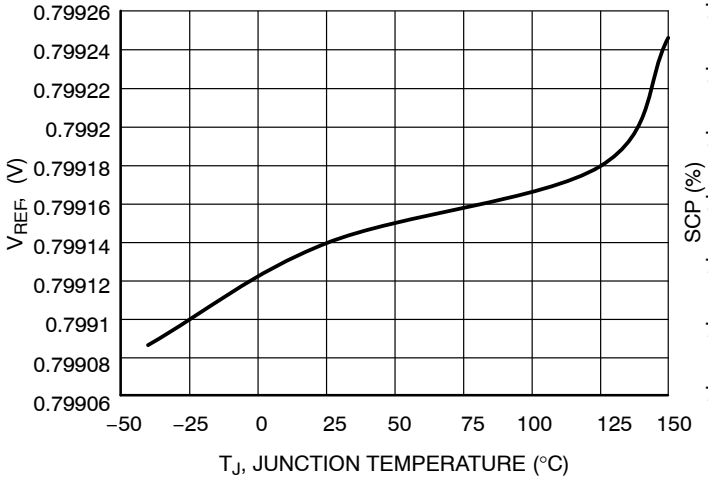


Figure 5. Reference Voltage vs. Junction Temperature

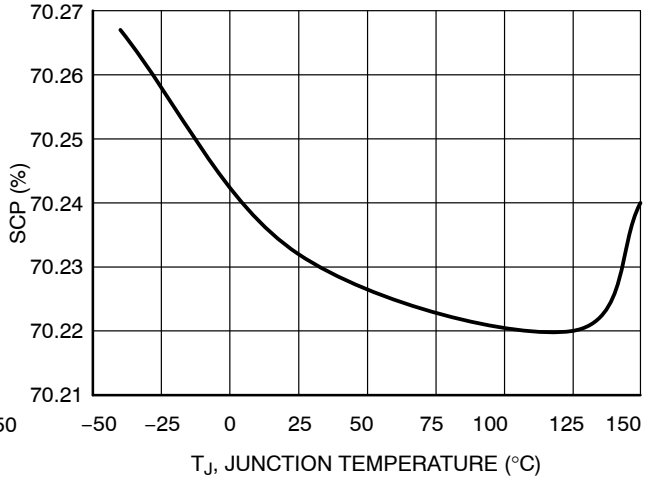


Figure 6. Short−Circuit Protection Threshold vs. Junction Temperature

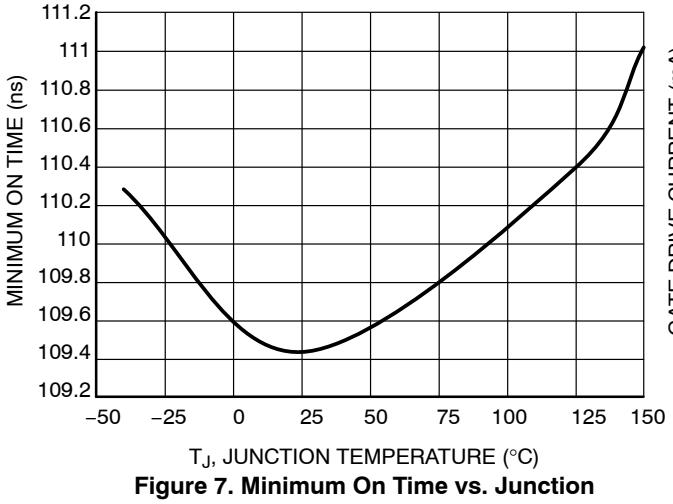


Figure 7. Minimum On Time vs. Junction Temperature

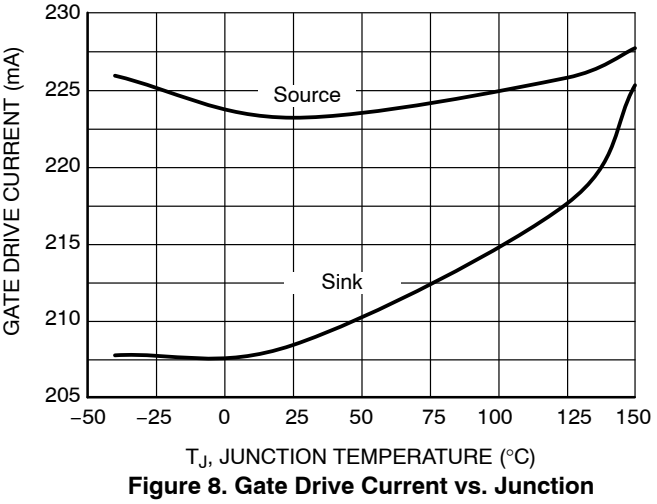


Figure 8. Gate Drive Current vs. Junction Temperature

TYPICAL CHARACTERISTICS CURVES

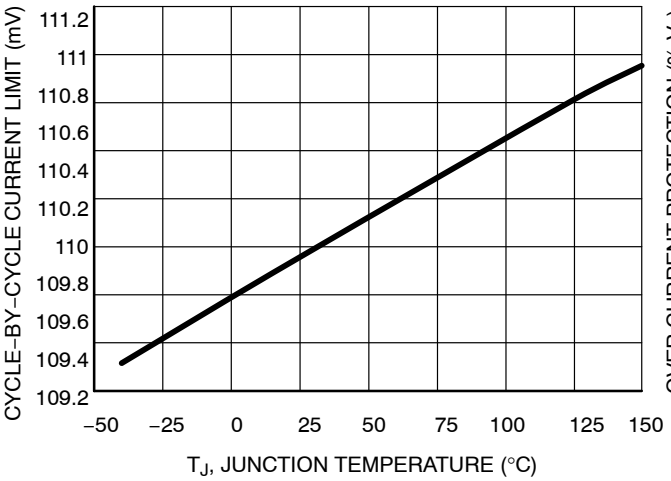


Figure 9. Cycle−by−Cycle Limit vs. Junction Temperature

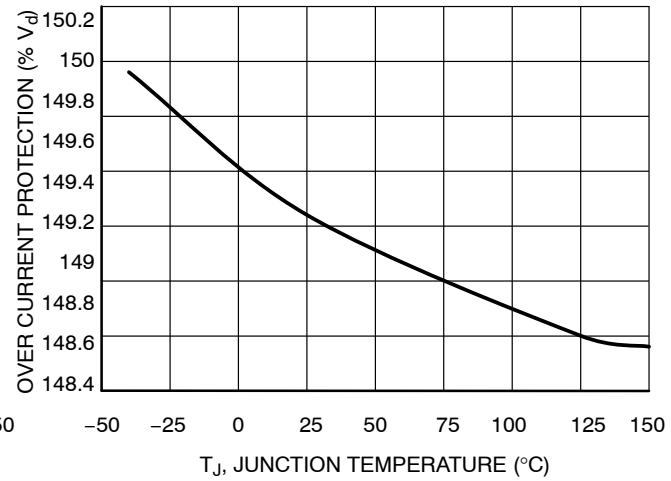


Figure 10. Over Current Protection vs. Junction Temperature

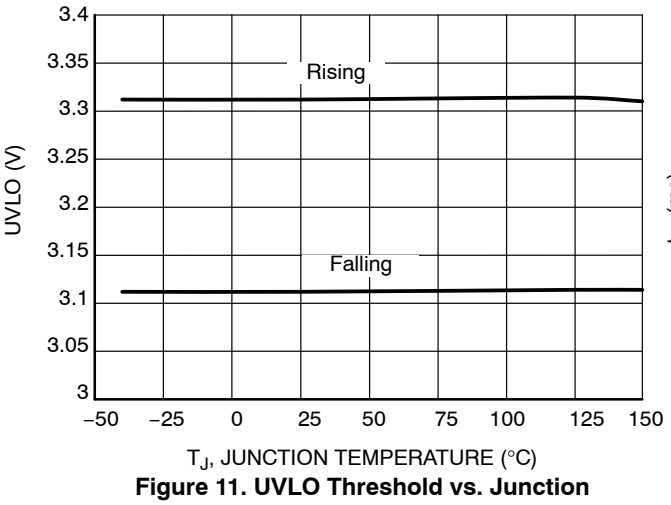


Figure 11. UVLO Threshold vs. Junction Temperature

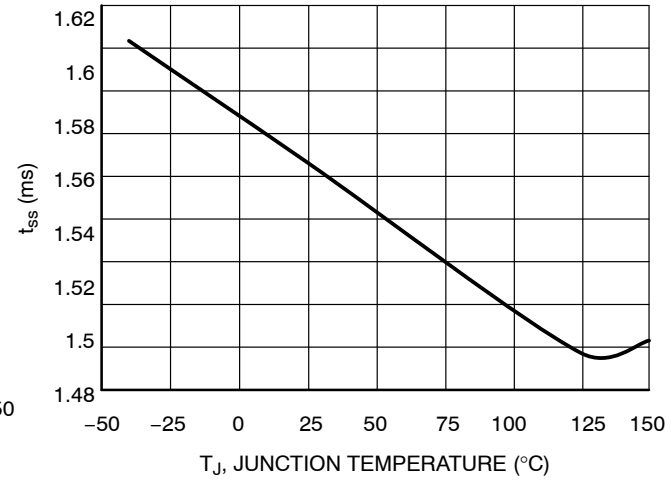


Figure 12. Soft−Start Time vs. Junction Temperature

THEORY OF OPERATION

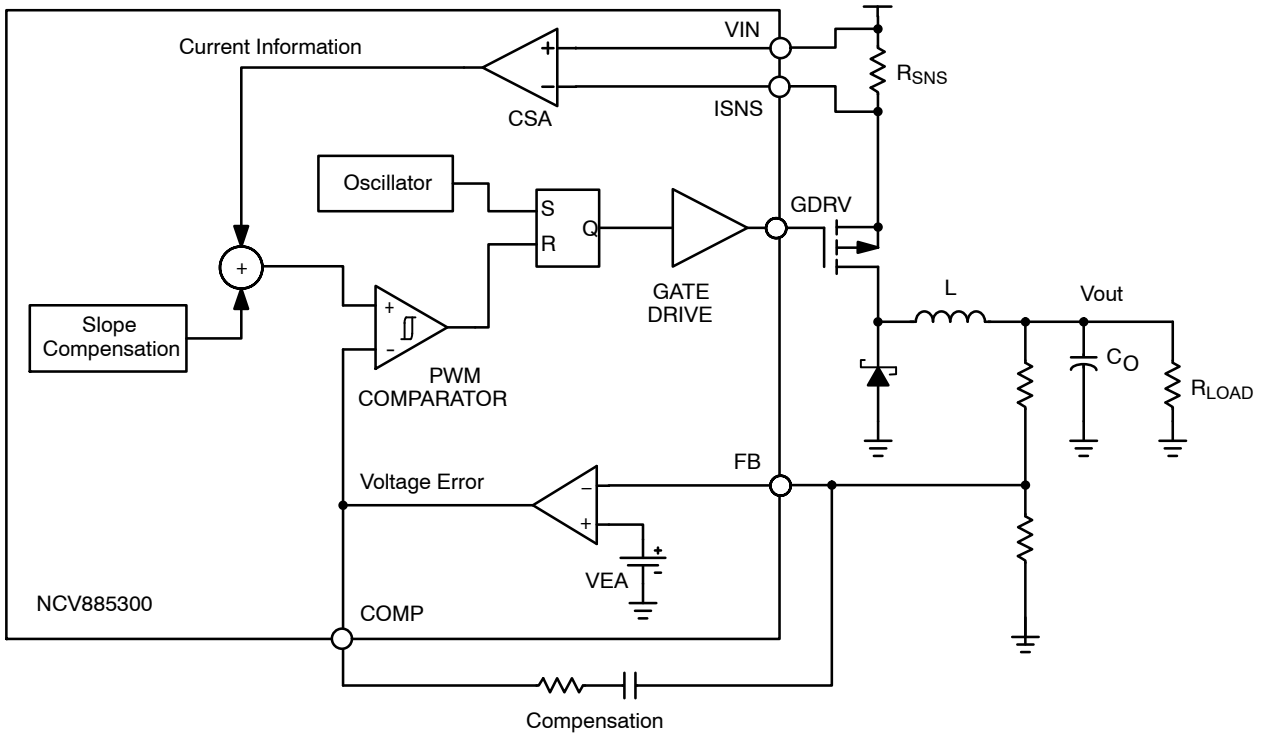


Figure 13. Current Mode Control Schematic

Current Mode Control

The NCV885300 SMPS incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as a fixed−frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived from the resistor in the power path, the signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse−by−pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows for a simpler compensation.

The NCV885300 also includes a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Overcurrent Protection

The NCV885300 features two current limit protections: peak current mode and overcurrent hiccup mode. When the current sense amplifier detects a voltage above the peak current limit between V_{IN} and ISNS after the current limit leading edge blanking time, the peak current limit causes the power switch to turn off for the remainder of the cycle. Set the current limit with a resistor from V_{IN} to ISNS, with $R = 0.100 / I_{limit}$.

If the voltage across the current sense resistor exceeds the overcurrent threshold voltage the part enters overcurrent hiccup mode. The part will remain off for the hiccup time and then go through the power on reset procedure.

Short Circuit Hiccup Protection

When the output voltage falls below the short circuit trip voltage the part enters short circuit latch off. When a short is detected the NCV885300 disables the outputs and attempts to re−enable the outputs after the short circuit hiccup time. The part remains off for the hiccup time and then goes through the power on reset procedure. If the short has been removed then the output stage re−enables and operates normally; however, if the short is still present the cycle begins again. Internal heat dissipation is kept to a minimum as current will only flow during the reset time of the protection circuitry. The hiccup mode is continuous until the short is removed.

Gate Drive

To turn on the P−Channel MOSFET, the gate driver turns on a current source to ground. A clamp ensures that the gate drive voltage does not exceed 10 V. When the clamp starts conducting the current source starts to turn off. To turn off the external MOSFET, the gate driver turns on a current source to V_{IN}.

EN/SYNC

This pin has three modes. When a dc logic high (CMOS/TTL compatible) voltage is applied to this pin the NCV885300 operates at the default frequency. When a dc logic low voltage is applied to this pin the NCV885300 enters a low quiescent current sleep mode. When a square wave of at least 40% of the switching frequency is applied to this pin the switcher operates at the same frequency as the square wave. If the signal is slower than 40% of the switching frequency, it will be interpreted as enabling and disabling the part. The falling edge of the square wave corresponds to the start of the switching cycle.

Power Good

The power good pin is high when the reference voltage reaches 90% of its target of 800 mV. The pin should be pulled up with a 10 kΩ resistor to 5 V. The output voltage of the controller may be used in this case.

Overvoltage Lockout

To protect the IC, if the voltage on the VIN pin the exceeds V_{ovlo} the NCV885300 will shutdown. When the voltage drops below this voltage the part will go through the normal soft−start procedure.

Undervoltage Lockout

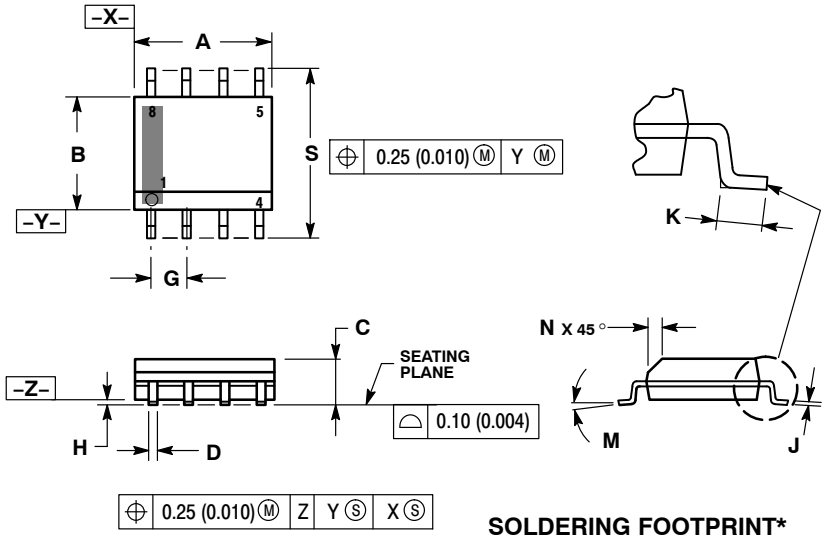
Undervoltage lockout protection is engaged when the input voltage drops below the V_{uvlo} signal. The part will remain off until the input voltage rises above the V_{uvlo} value plus hysteresis. Depending on the desired output voltage, it is possible to engage the short-circuit hiccup mode before undervoltage lockout occurs.

Soft−Start

To ensure moderate inrush current and reduce output overshoot, the NCV885300 features a soft start which periodically adds charge to a capacitor until the final reference voltage is achieved. When using an external SYNC signal, charging is based on the switching frequency. If, for example, the NCV885300 is synchronized to twice the free running (not synced) frequency, the soft−start will be half as long.

PACKAGE DIMENSIONS

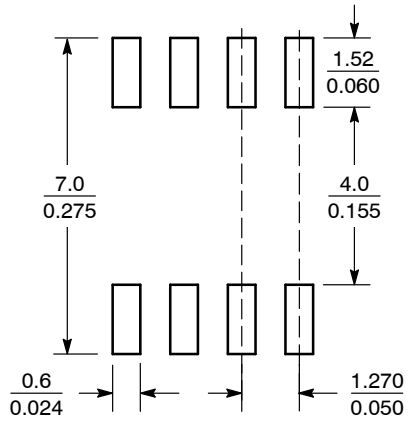
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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