# NSBA115TF3

# Digital Transistors (BRT)
# R1 = 100 kΩ, R2 = ∞ kΩ

## PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS** ($T_A$ = 25°C)

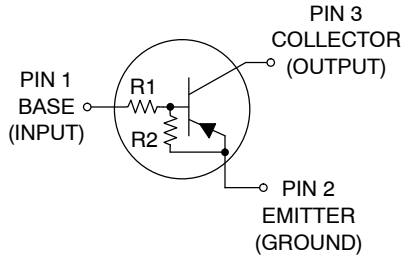
| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector−Base Voltage | $V_{CBO}$ | 50 | Vdc |
| Collector−Emitter Voltage | $V_{CEO}$ | 50 | Vdc |
| Collector Current − Continuous | $I_C$ | 100 | mAdc |
| Input Forward Voltage | $V_{IN(fwd)}$ | 40 | Vdc |
| Input Reverse Voltage | $V_{IN(rev)}$ | 5 | Vdc |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**ON Semiconductor®**

**http://onsemi.com**

**PIN CONNECTIONS**




**MARKING DIAGRAM**


**SOT−1123**
**CASE 524AA**
**STYLE 1**

XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

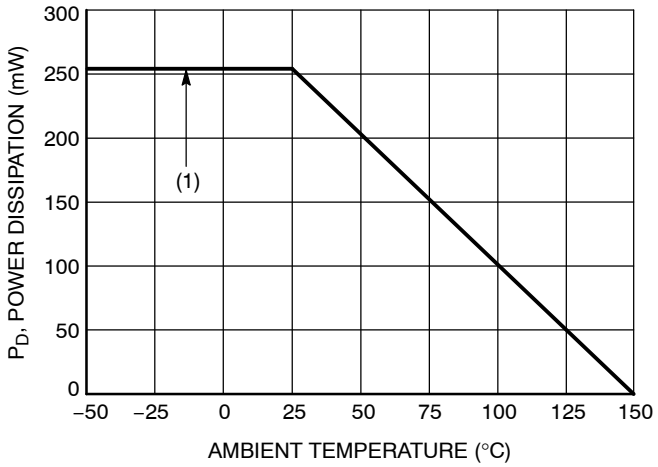
**ORDERING INFORMATION**

See detailed ordering, marking, and shipping information in the package dimensions section on page 2 of this data sheet.

**Table 1. ORDERING INFORMATION**

| Device | Part Marking | Package | Shipping† |
|---|---|---|---|
| NSBA115TF3T5G | Q (90°)* | SOT−1123 | 8,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
* (xx°) = Degree rotation in the clockwise direction.




(1) SOT−1123; 100 mm$^2$, 1 oz. copper trace

**Figure 1. Derating Curve**

**Table 2. THERMAL CHARACTERISTICS**

| Characteristic | | Symbol | Max | Unit |
|---|---|---|---|---|
| **THERMAL CHARACTERISTICS (SOT−1123) (NSBA115TF3)** | | | | |
| Total Device Dissipation | | $P_D$ | | |
| $T_A$ = 25°C | (Note 1) | | 254 | mW |
| | (Note 2) | | 297 | |
| Derate above 25°C | (Note 1) | | 2.0 | mW/°C |
| | (Note 2) | | 2.4 | |
| Thermal Resistance, Junction to Ambient | (Note 1) | $R_{\theta JA}$ | 493 | °C/W |
| | (Note 2) | | 421 | |
| Thermal Resistance, Junction to Lead | (Note 1) | $R_{\theta JL}$ | 193 | °C/W |
| Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | −55 to +150 | °C |

1. FR−4 @ 100 mm$^2$, 1 oz. copper traces, still air.
2. FR−4 @ 500 mm$^2$, 1 oz. copper traces, still air.

**Table 3. ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Base Cutoff Current ($V_{CB}$ = 50 V, $I_E$ = 0) | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector−Emitter Cutoff Current ($V_{CE}$ = 50 V, $I_B$ = 0) | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter−Base Cutoff Current ($V_{EB}$ = 6.0 V, $I_C$ = 0) | $I_{EBO}$ | – | – | 0.1 | mAdc |
| Collector−Base Breakdown Voltage ($I_C$ = 10 μA, $I_E$ = 0) | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Collector−Emitter Breakdown Voltage (Note 3) ($I_C$ = 2.0 mA, $I_B$ = 0) | $V_{(BR)CEO}$ | 50 | – | – | Vdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (Note 3) ($I_C$ = 5.0 mA, $V_{CE}$ = 10 V) | $h_{FE}$ | 160 | 350 | – | |
| Collector−Emitter Saturation Voltage (Note 3) ($I_C$ = 10 mA, $I_B$ = 0.3 mA) | $V_{CE(sat)}$ | – | – | 0.25 | Vdc |
| Input Voltage (off) ($V_{CE}$ = 5.0 V, $I_C$ = 100 μA) | $V_{i(off)}$ | – | 0.62 | – | Vdc |
| Input Voltage (on) ($V_{CE}$ = 0.2 V, $I_C$ = 1.0 mA) | $V_{i(on)}$ | – | 1.0 | – | Vdc |
| Output Voltage (on) ($V_{CC}$ = 5.0 V, $V_B$ = 2.5 V, $R_L$ = 1.0 kΩ) | $V_{OL}$ | – | – | 0.2 | Vdc |
| Output Voltage (off) ($V_{CC}$ = 5.0 V, $V_B$ = 0.5 V, $R_L$ = 1.0 kΩ) | $V_{OH}$ | 4.9 | – | – | Vdc |
| Input Resistor | R1 | 70 | 100 | 130 | kΩ |
| Resistor Ratio | $R_1/R_2$ | – | – | – | |

3. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.

## TYPICAL CHARACTERISTICS – NSBA115TF3

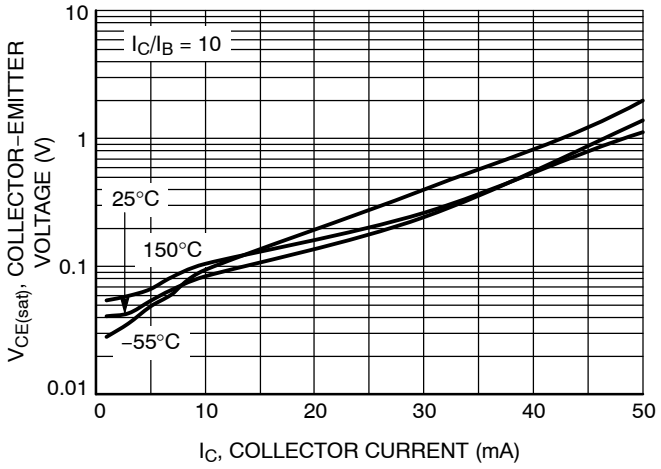



**Figure 2. $V_{CE(sat)}$ vs. $I_C$**

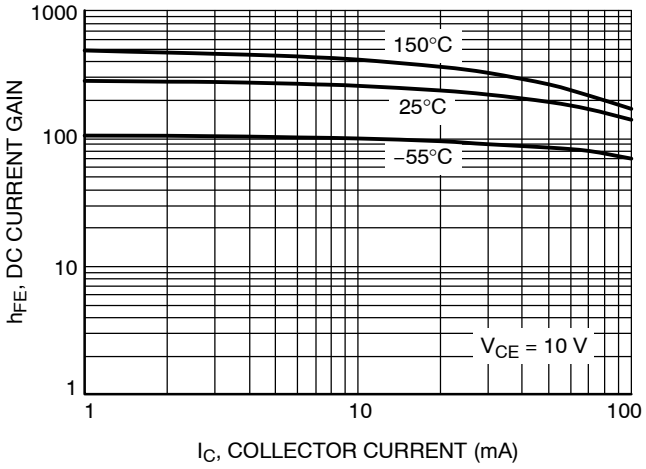



**Figure 3. DC Current Gain**

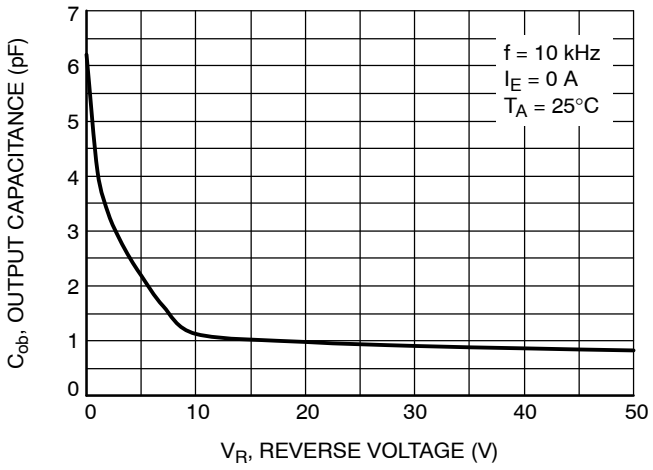



**Figure 4. Output Capacitance**

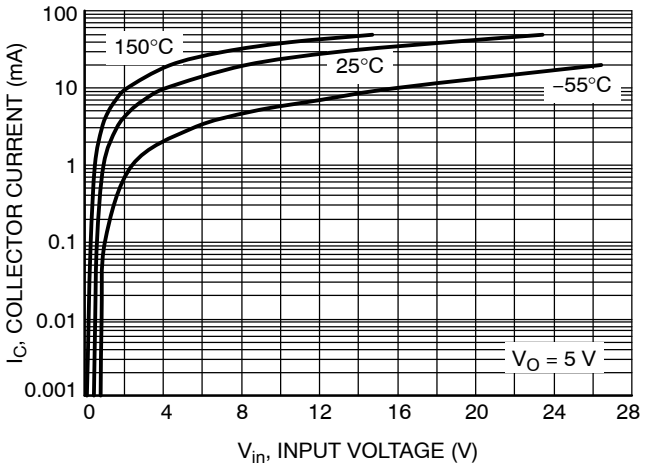



**Figure 5. Output Current vs. Input Voltage**

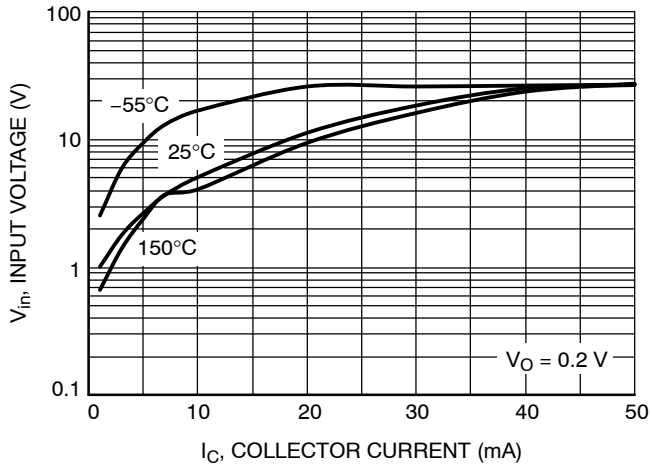
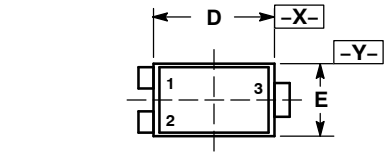


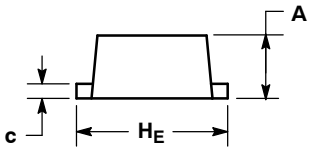

**Figure 6. Input Voltage vs. Output Current**

## PACKAGE DIMENSIONS

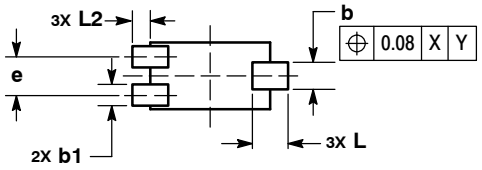
**SOT−1123**
CASE 524AA
ISSUE C




TOP VIEW




SIDE VIEW



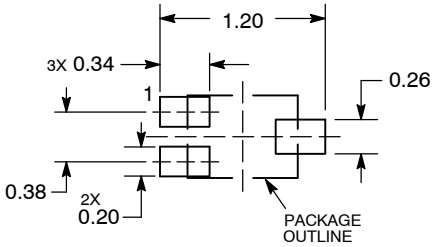

BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.34 | 0.40 |
| b | 0.15 | 0.28 |
| b1 | 0.10 | 0.20 |
| c | 0.07 | 0.17 |
| D | 0.75 | 0.85 |
| E | 0.55 | 0.65 |
| e | 0.35 | 0.40 |
| $H_E$ | 0.95 | 1.05 |
| L | 0.185 REF | |
| L2 | 0.05 | 0.15 |

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81−3−5817−1050

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative