P4C1256
HIGH SPEED 32K x 8 STATIC CMOS RAM

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Specialist Distributor of High Technology Memories & Logic.

FEATURES

- High Speed (Equal Access and Cycle Times)
  —12/15/20/25/35 ns (Commercial)
  —15/20/25/35/45 ns (Industrial)
- Low Power
  —880 mW Active
- Single 5 Volts ±10% Power Supply
- Easy Memory Expansion Using $\overline{CE}$ and $\overline{OE}$ Inputs
- Common Data I/O
- Three-State Outputs
- Fully TTL Compatible Inputs and Outputs
- Advanced CMOS Technology
- Fast t_{OE}
- Automatic Power Down
- Packages
  —28-Pin 300 mil DIP and SOJ

DESCRIPTION

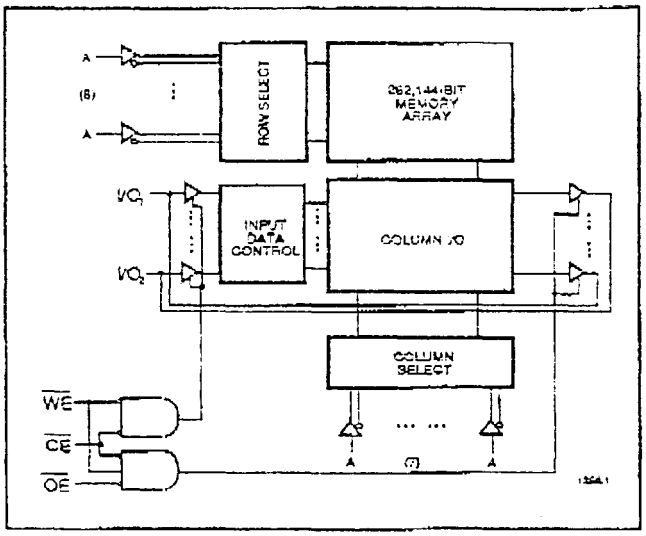
The P4C1256 is a 262,144-bit high-speed CMOS static RAM organized as 32Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

Access times as fast as 12 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P4C1256 is a member of a family of PACE RAM™ products offering fast access times.

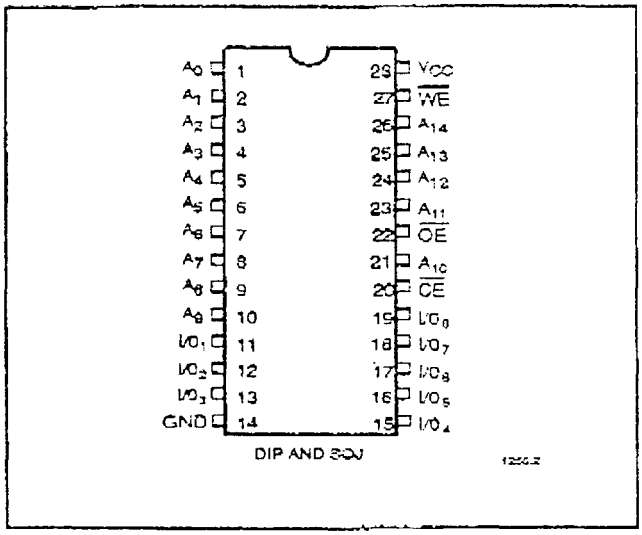
The P4C1256 device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{14}. Reading is accomplished by device selection ($\overline{CE}$) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or $\overline{WE}$ is LOW.

Package options for the P4C1256 include 28-pin 300 mil DIP and SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PERFORMANCE SEMICONDUCTOR CORPORATION

Means Quality, Service and Speed

RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

Temperature Range (Ambient)	Supply Voltage
Commercial (0°C to 70°C)	$4.5V \le V_{CC} \le 5.5V$
Industrial (-40°C to 85°C)	$4.5V \le V_{CC} \le 5.5V$

MAXIMUM RATINGS

Stresses greater than those listed can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Maximum Ratings for extended periods can adversely affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage with Respect to GND	-0.5	7.0	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5	V_{CC} + 0.5	V
T_A	Operating Ambient Temperature	-55	125	°C
S_{TG}	Storage Temperature	-65	150	°C
I_{OUT}	Output Current into Low Outputs		25	mA
I_{LAT}	Latch-up Current	>200		mA

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	Output High Voltage I/O_0 - I/O_7	I_{OH} = -4 mA, V_{CC} = 4.5V	2.4		V
V_{OL}	Output Low Voltage (I/O_1 - I/O_8)	I_{OL} = 8 mA I_{OL} = 10 mA		0.4 0.5	V V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{LI}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$	-5	+5	µA
I_{LO}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, $\overline{CE} = V_{CC}$	-5	+5	µA
I_{OS}	Output Short-Circuit Current	V_{OUT} = GND, V_{CC} = Max (Single output not to exceed 30 second duration)		-350	mA
I_{SB1}	V_{CC} Current CMOS Standby Current	V_{CC} = 5.5V, I_{OUT} = 0 mA, $\overline{CE} = V_{CC}$		10	mA

CAPACITANCES

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	pF

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Test Conditions	-12	-15	-20	-25	-35	-45	Unit
I_{CC}	Dynamic Operating Current	*	165	160	155	150	145	140	mA

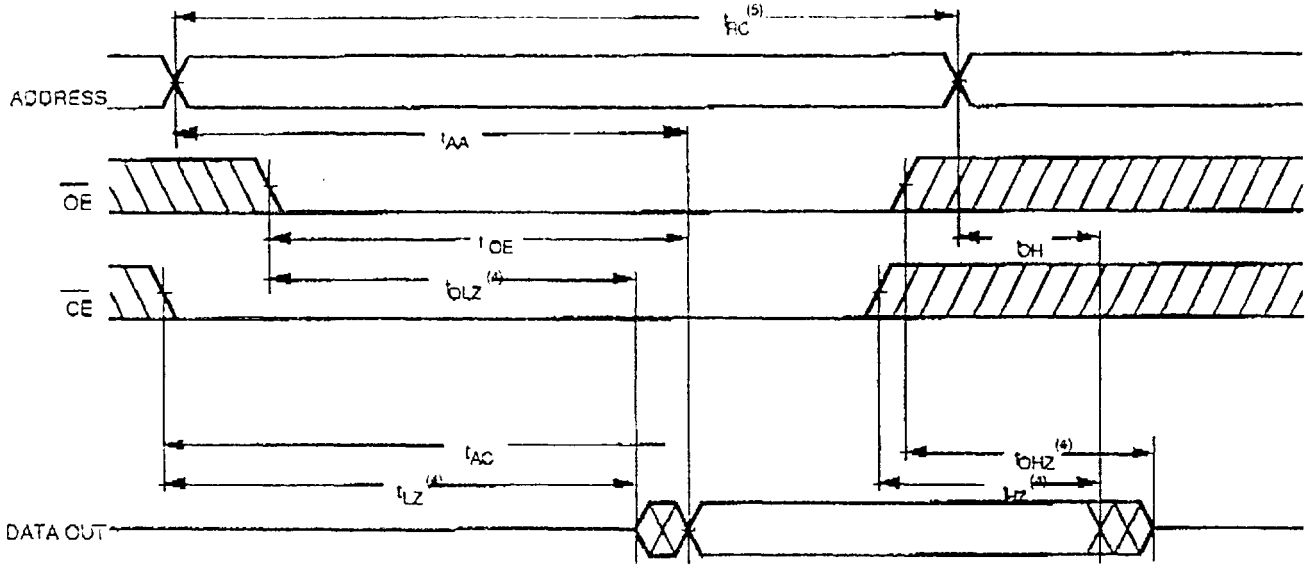
*Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$, and $\overline{WE} \leq V_{IL}$ (max). Switching inputs are 0V and 3V.

AC ELECTRICAL CHARACTERISTICS - READ CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

Sym	Parameter	-12		-15		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address Access Time		12		15		20		25		35		45	ns
t_{AC}	Chip Enable Access Time		12		15		20		25		35		45	ns
t_{OH}	Output Hold from Address Change	2		2		2		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		5		8		9		11		15		20	ns
t_{OE}	Output Enable Low to Data Valid		5		7		9		10		15		20	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		5		7		9		11		15		20	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		12		15		20		20		20		25	ns

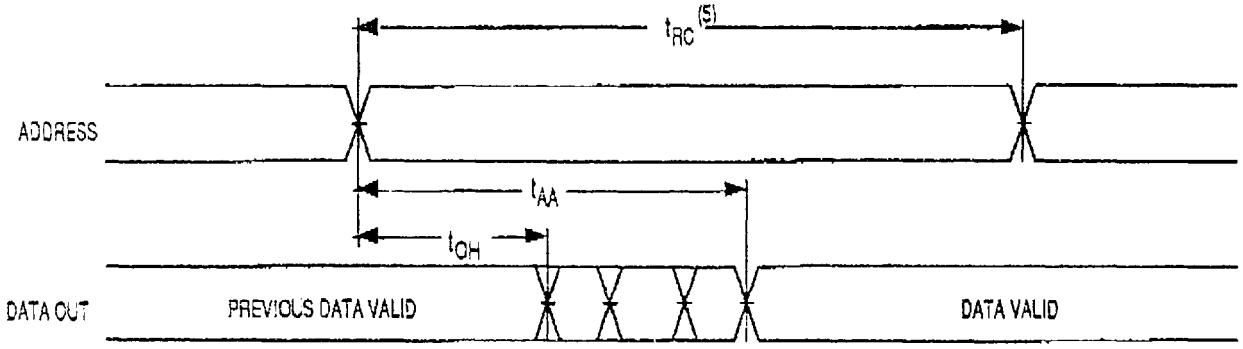
READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED) [1]



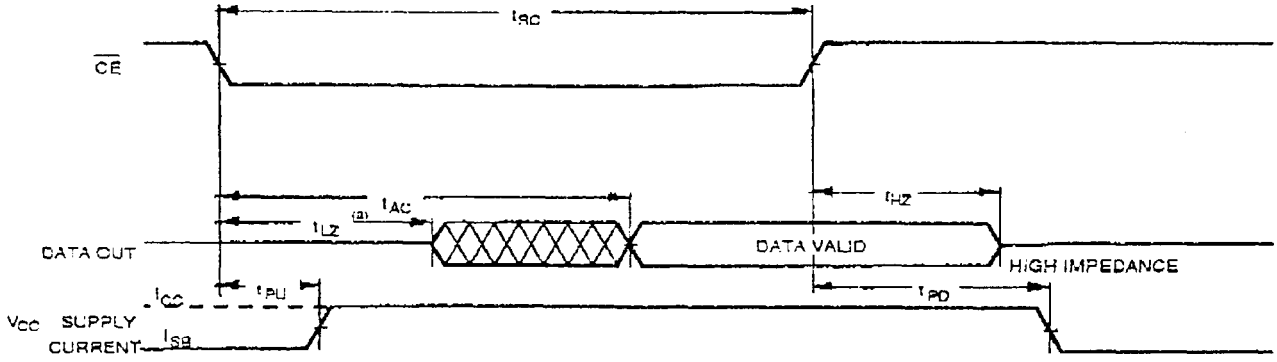
NOTES:

1. $\overline{WE}$ is HIGH for READ cycle.
2. $\overline{CE}$ is LOW and $\overline{OE}$ is LOW for READ cycle.
3. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ transition LOW.
4. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
5. READ Cycle Time is measured from the last valid address to the first transitioning address.

READ CYCLE NO. 2 (ADDRESS CONTROLLED)



READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)

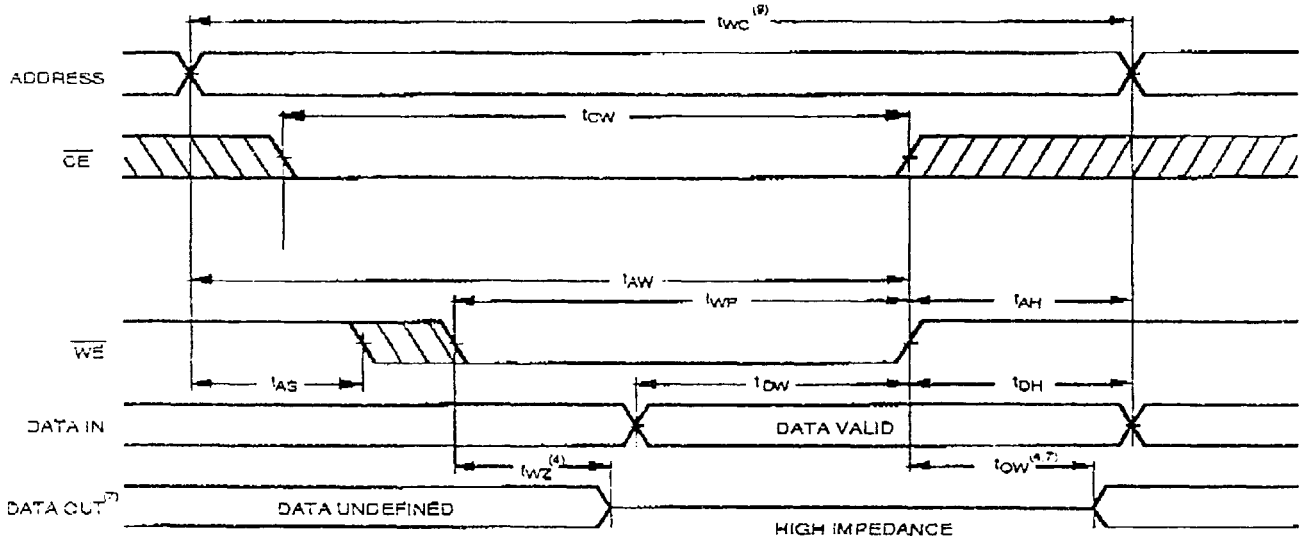


AC CHARACTERISTICS - WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

Sym	Parameter	-12		-15		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t_{CW}	Chip Enable Time to End of Write	9		10		15		18		22		30		ns
t_{AW}	Address Valid to End of Write	9		10		15		20		25		35		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	9		11		15		18		22		25		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	8		9		11		13		15		20		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		7		8		10		11		15		18	ns
t_{OW}	Output Active from End of Write	3		3		3		3		5		5		ns

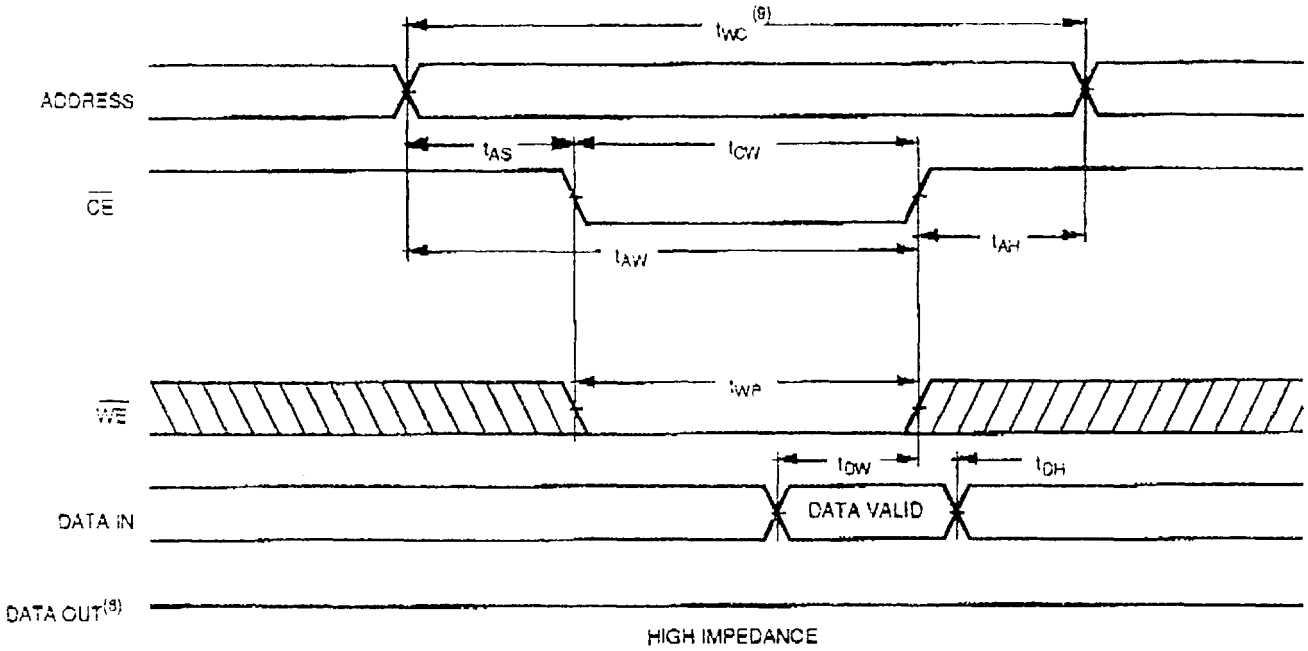
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) [6]



Notes:

6. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
7. $\overline{OE}$ is LOW for this WRITE cycle to show twz and tow.
8. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
9. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CE}$ CONTROLLED) [9]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{I/O}$	Power
Standby	H	X	X	High Z	Standby
Standby	X	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	High Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	High Z	Active

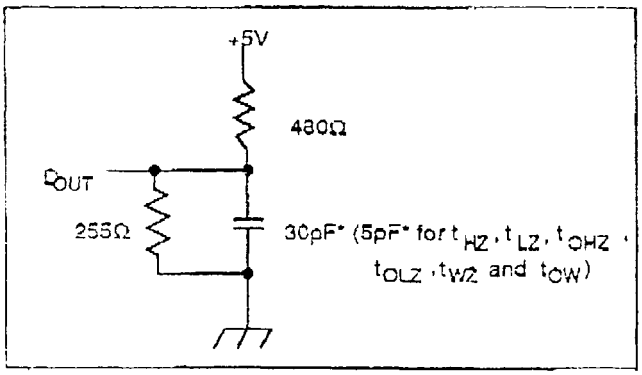


Figure 1. Output Load

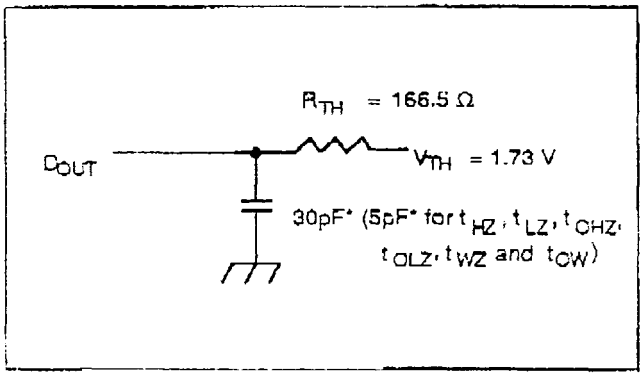


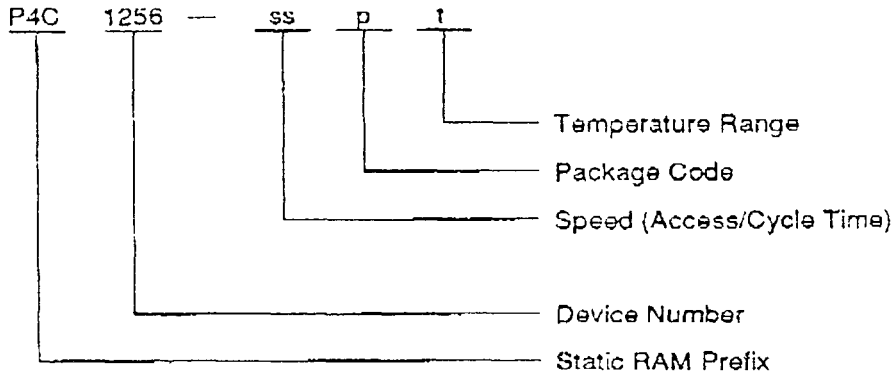
Figure 2. Thevenin Equivalent

* Including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C1256, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION

Performance Semiconductor's part numbering scheme is as follows:



l = Ultra-low standby power designator L, if available.
ss = Speed (access/cycle time in ns), e.g., 25, 35
p = Package code, i.e., P, J, C, DW, L.
t = Temperature range, i.e., C, M, MB.

PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
I	Industrial Temperature Range, -40°C to +85°C

SELECTION GUIDE

The P4C1256 is available in the following temperature, speed and package options.

Temp. Range	Package	Speed (ns)					
		-12	-15	-20	-25	-35	-45
Commercial Temperature	Plastic DIP Plastic SOJ	-12PC -12JC	-15PC -15JC	-20PC -20JC	-25PC -25JC	-35PC -35JC	N/A N/A
Industrial Temperature	Plastic DIP Plastic SOJ	N/A N/A	-15PI -15JI	-20PI -20JI	-25PI -25JI	-35PI -35JI	-45PI -45JI

N/A = Not Available