PALCE16V8 Family

EE CMOS 20-Pin Universal Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- **Pin and function compatible with all 20-pin GAL devices**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - — 5-ns propagation delay for "-5" version
  - — 7.5-ns propagation delay for "-7" version
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Peripheral Component Interconnect (PCI) compliant**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**
- **5 ns version utilizes a split leadframe for improved performance**

GENERAL DESCRIPTION

The PALCE16V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

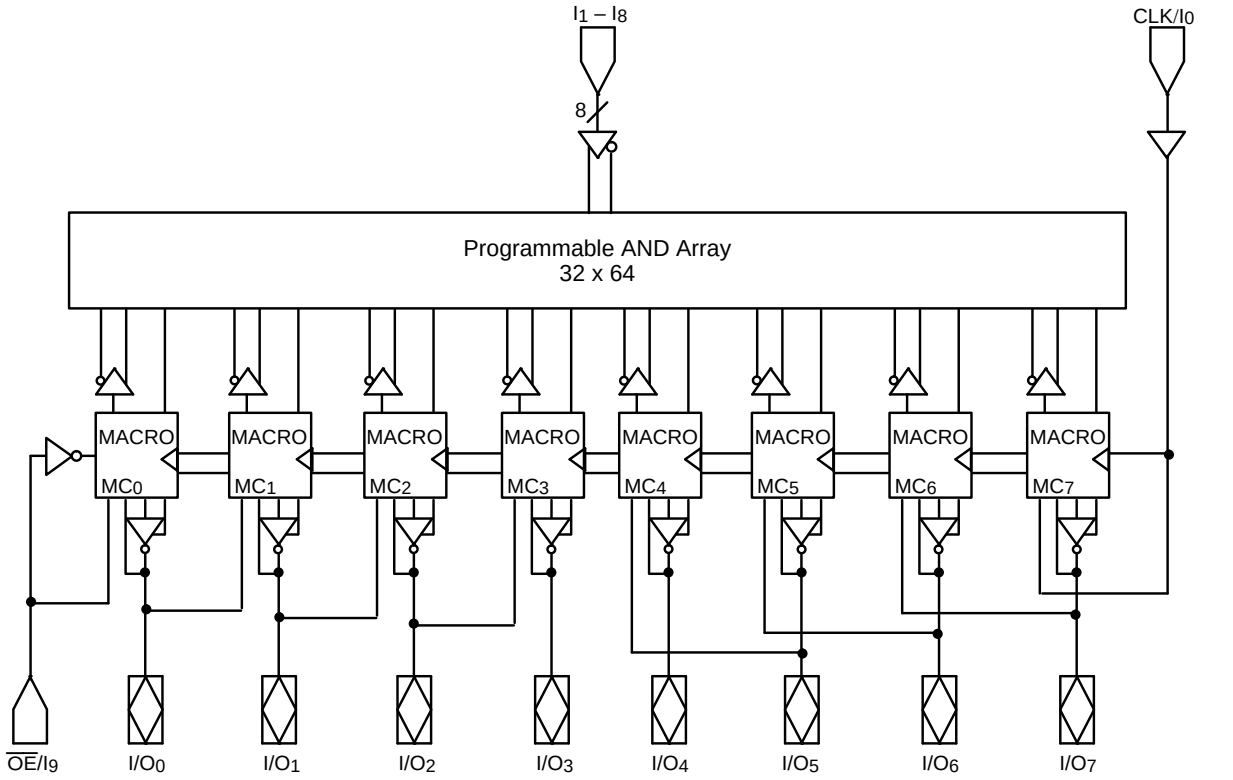
The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE16V8 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar.

Publication# **16493** Rev. **D** Amendment **/0**
Issue Date: **February 1996**

BLOCK DIAGRAM



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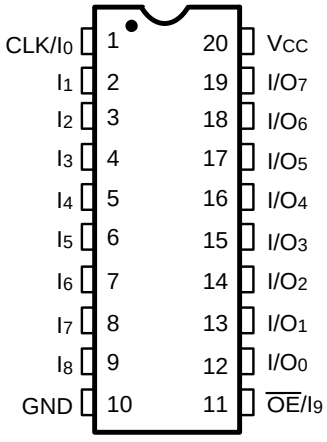
CONNECTION DIAGRAMS
Top View

DIP/SOIC



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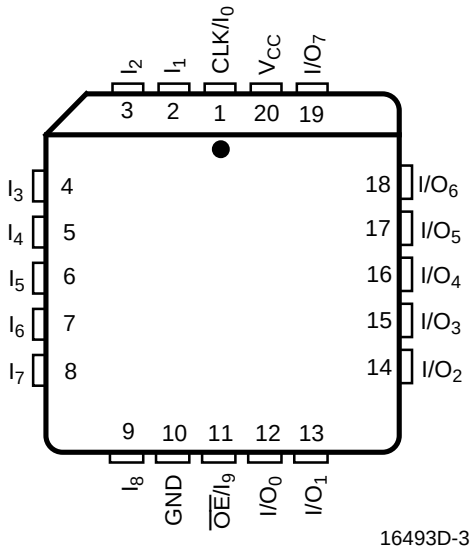
Note: *Pin 1 is marked for orientation.*

PLCC/LCC



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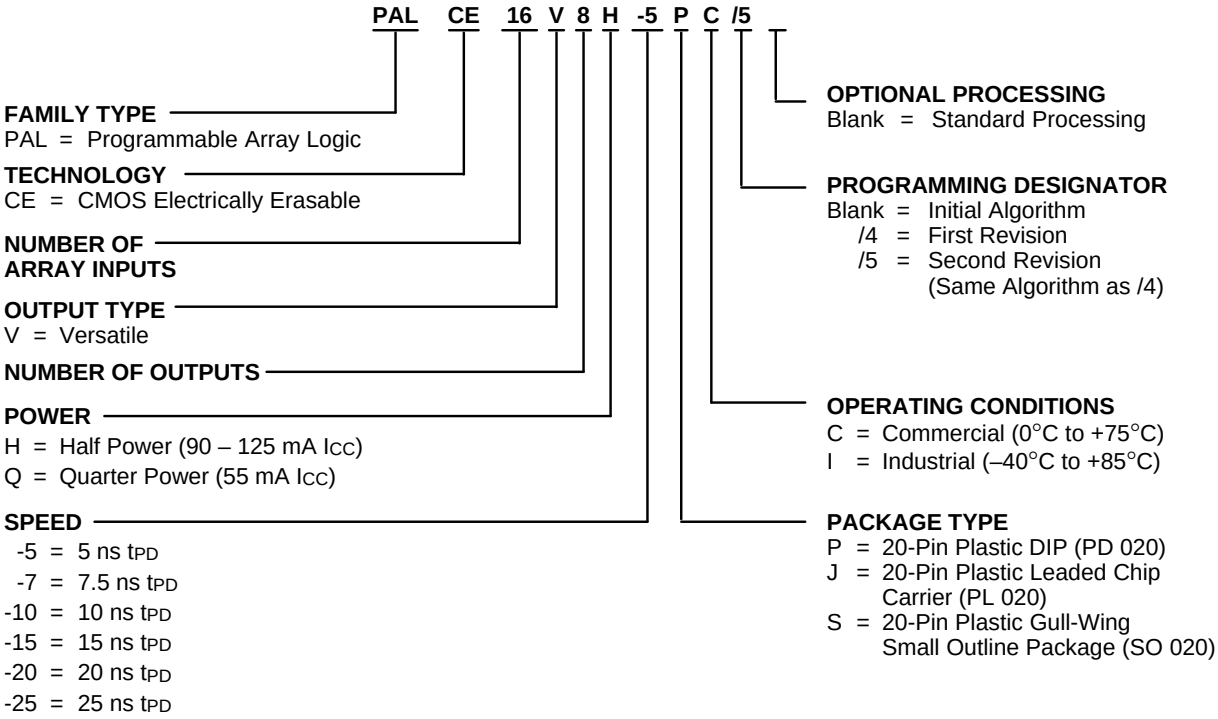
PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
$\overline{OE}$	=	Output Enable
V_{CC}	=	Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE16V8H-5	JC	/5
PALCE16V8H-7	PC, JC	
PALCE16V8H-10	PC, JC, SC, PI, JI	/4
PALCE16V8Q-10	PC, JC, SC	/5
PALCE16V8H-15	PC, JC, SC, PI, JI	Blank, /4
PALCE16V8Q-15	PC, JC	
PALCE16V8Q-20	PI, JI	
PALCE16V8H-25	PC, JC, SC, PI, JI	
PALCE16V8Q-25	PC, JC, PI, JI	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

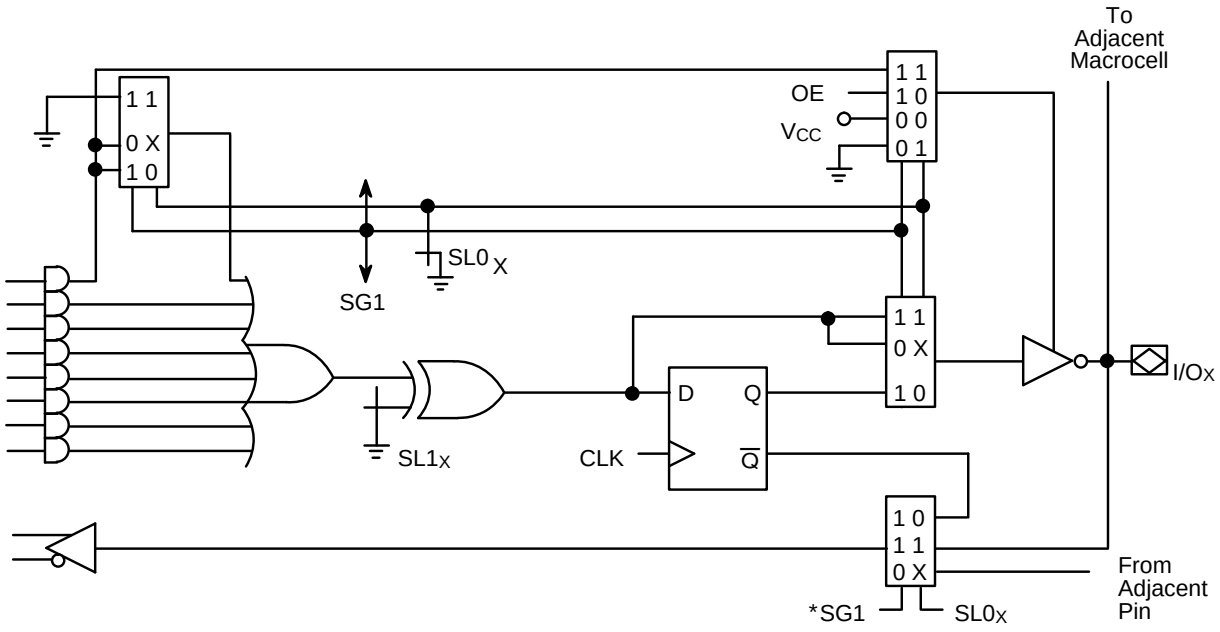
FUNCTIONAL DESCRIPTION

The PALCE16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8 are automatically configured from the user's design specification. The design specification is processed by development software to verify the design and create a programming file (JEDEC). This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8. The programmer will program the PALCE16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8. Here the user must use the PALCE16V8 device code. This option allows full utilization of the macrocell.



**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

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PALCE16V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8 will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 15 and 16. Pins 15 and 16 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

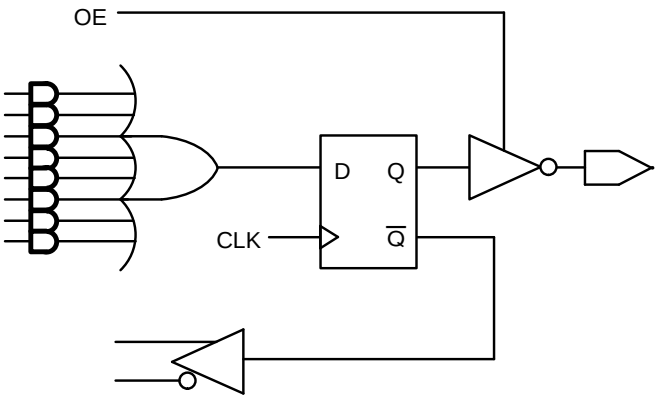
Table 1. Macrocell Configuration

SG0	SG1	SL0x	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

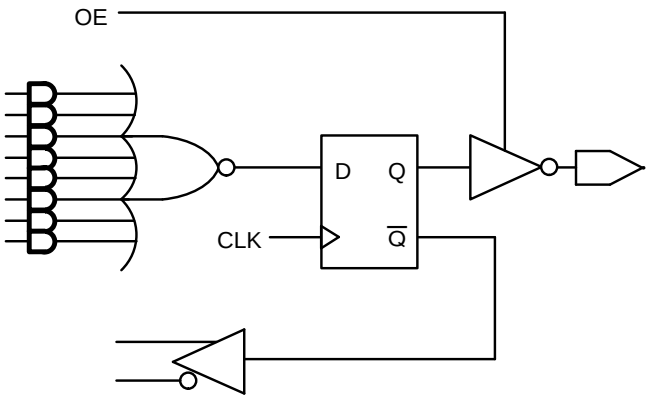
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save “DeMorganizing” efforts.

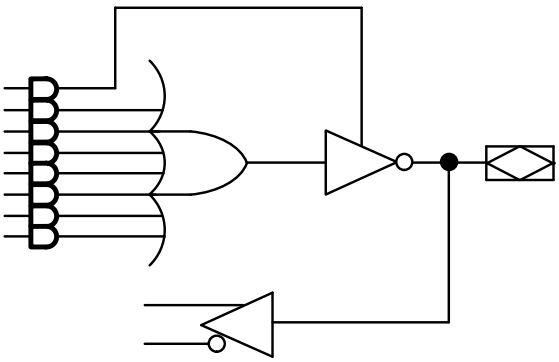
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



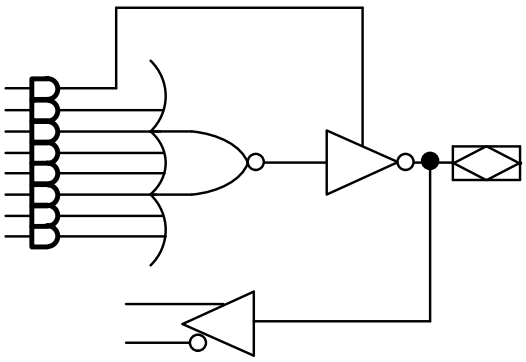
Registered Active Low



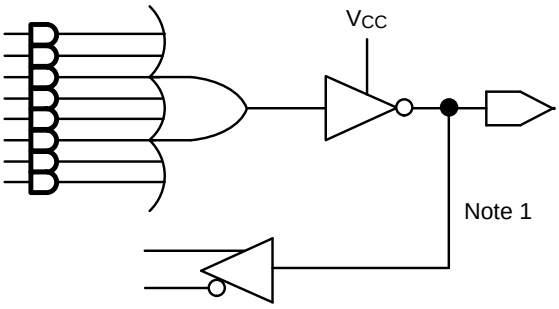
Registered Active High



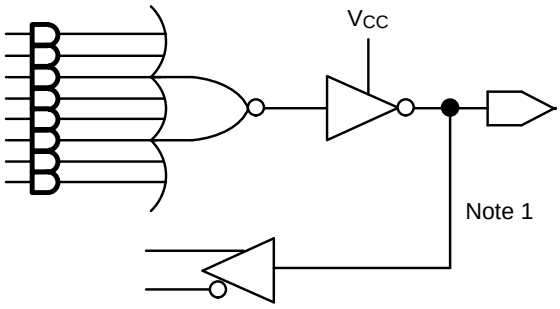
Combinatorial I/O Active Low



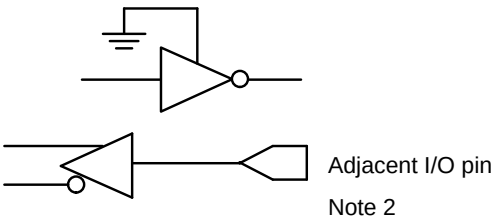
Combinatorial I/O Active High



Combinatorial Output Active Low



Combinatorial Output Active High



Dedicated Input

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Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *This configuration is not available on pins 15 and 16.*

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALCE16V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

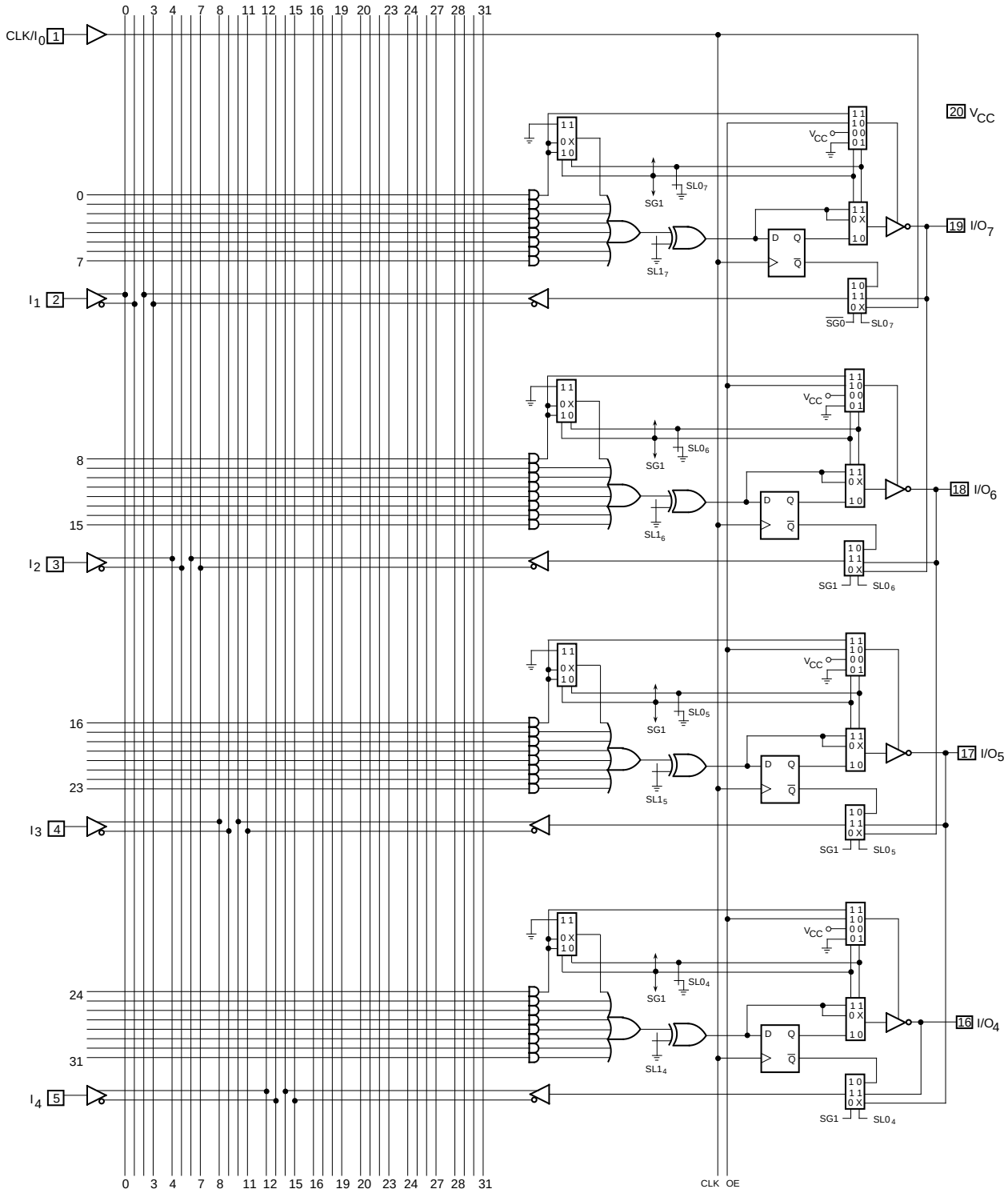
Technology

The high-speed PALCE16V8 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

PCI Compliance

The PALCE22V10H-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The PALCE22V10H-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design.

LOGIC DIAGRAM



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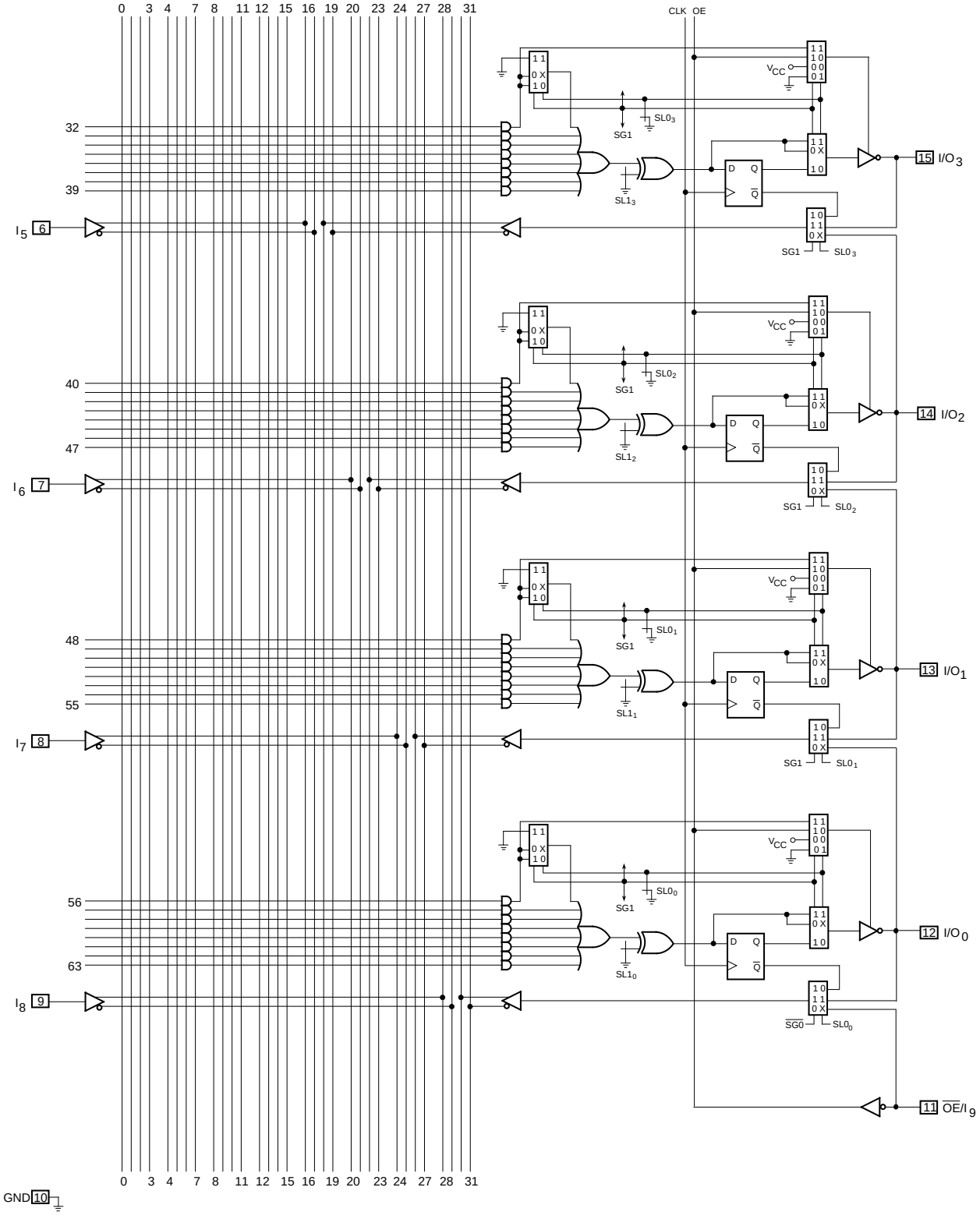
LOGIC DIAGRAM (continued)



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(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Static)	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{IN} = 0 V V_{CC} = Max		125	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 5)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	5	ns
t_S	Setup Time from Input or Feedback to Clock			3		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)				1	ns
t_{WL}	Clock Width	LOW		3		ns
t_{WH}		HIGH		3		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	142.8		MHz
		Internal Feedback (f_{CNT}),	$1/(t_S+t_{CF})$ (Note 6)	166		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	166		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			2	6	ns
t_{ER}	Input to Output Disable Using Product Term Control			2	5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
6. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

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Ambient Temperature with Power Applied . . . . . –55°C to +125°C

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DC Input Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
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V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 5)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output		8 Outputs Switching	3	7.5	ns
			1 Output Switching	3	7	ns
t_S	Setup Time from Input or Feedback			5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)				1	ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	100		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 6)	125		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	ns
t_{PXA}	$\overline{OE}$ to Output Disable			1	6	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	9	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
6. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Temperature (T_A) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Dynamic)	Commercial Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz		115	mA
	Industrial Supply Current			130	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 4)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	71.4		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz		55	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 4)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	71.4		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Temperature (T_A) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC} (Dynamic)	Commercial Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz	H		90	mA
			Q		55	
I_{CC} (Dynamic)	Industrial Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz	H		130	mA
			Q		65	

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

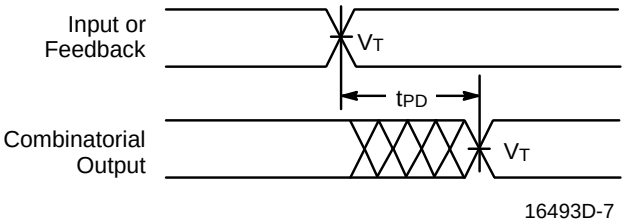
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-20		-25		
				Min	Max	Min	Max	Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		20		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		13		15		ns
t_H	Hold Time			0		0		0		ns
t_{CO}	Clock to Output				10		11		12	ns
t_{WL}	Clock Width	LOW		8		10		12		ns
t_{WH}		HIGH		8		10		12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	45.5		41.6		37		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CO})$ (Note 4)	50		45.4		40		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		50.0		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		18		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		18		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		18		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		18		20	ns

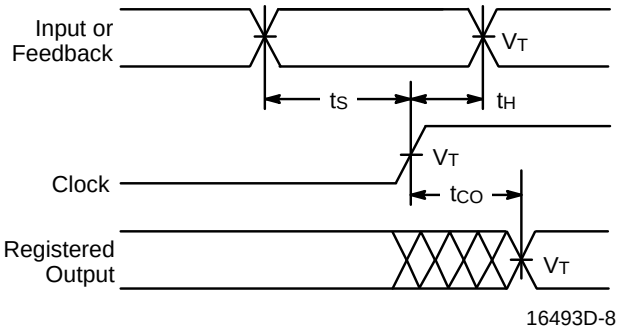
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

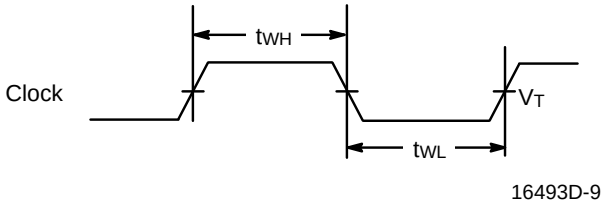
SWITCHING WAVEFORMS



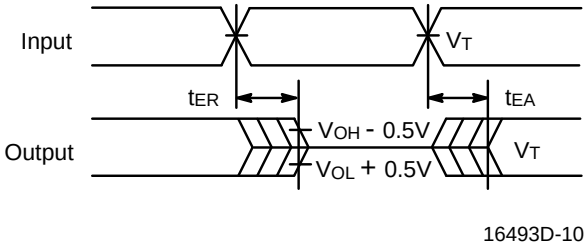
Combinatorial Output



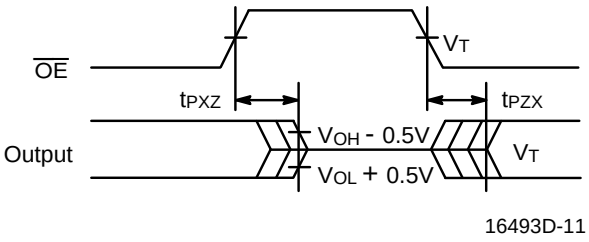
Registered Output



Clock Width



Input to Output Disable/Enable

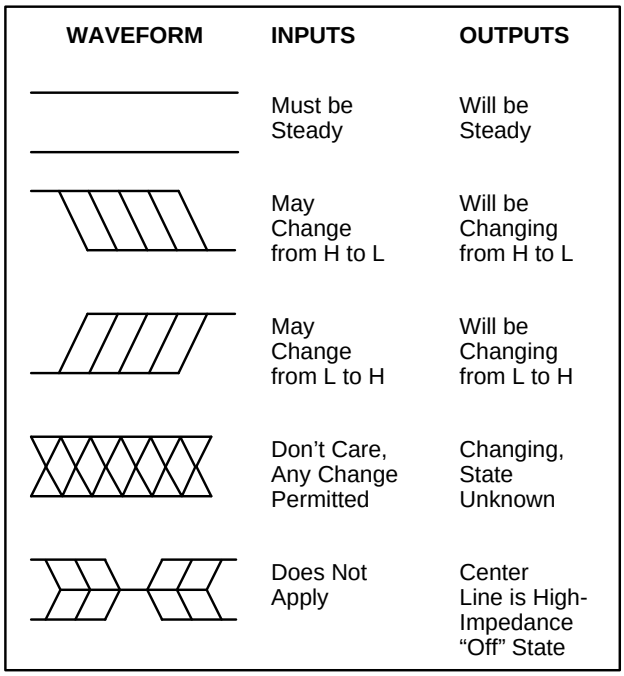


$\overline{OE}$ to Output Disable/Enable

Notes:

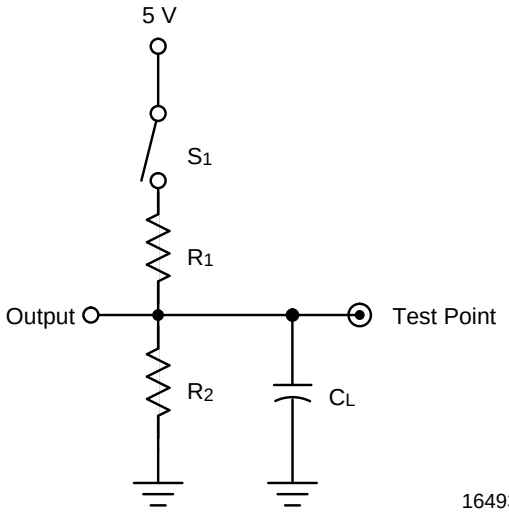
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT

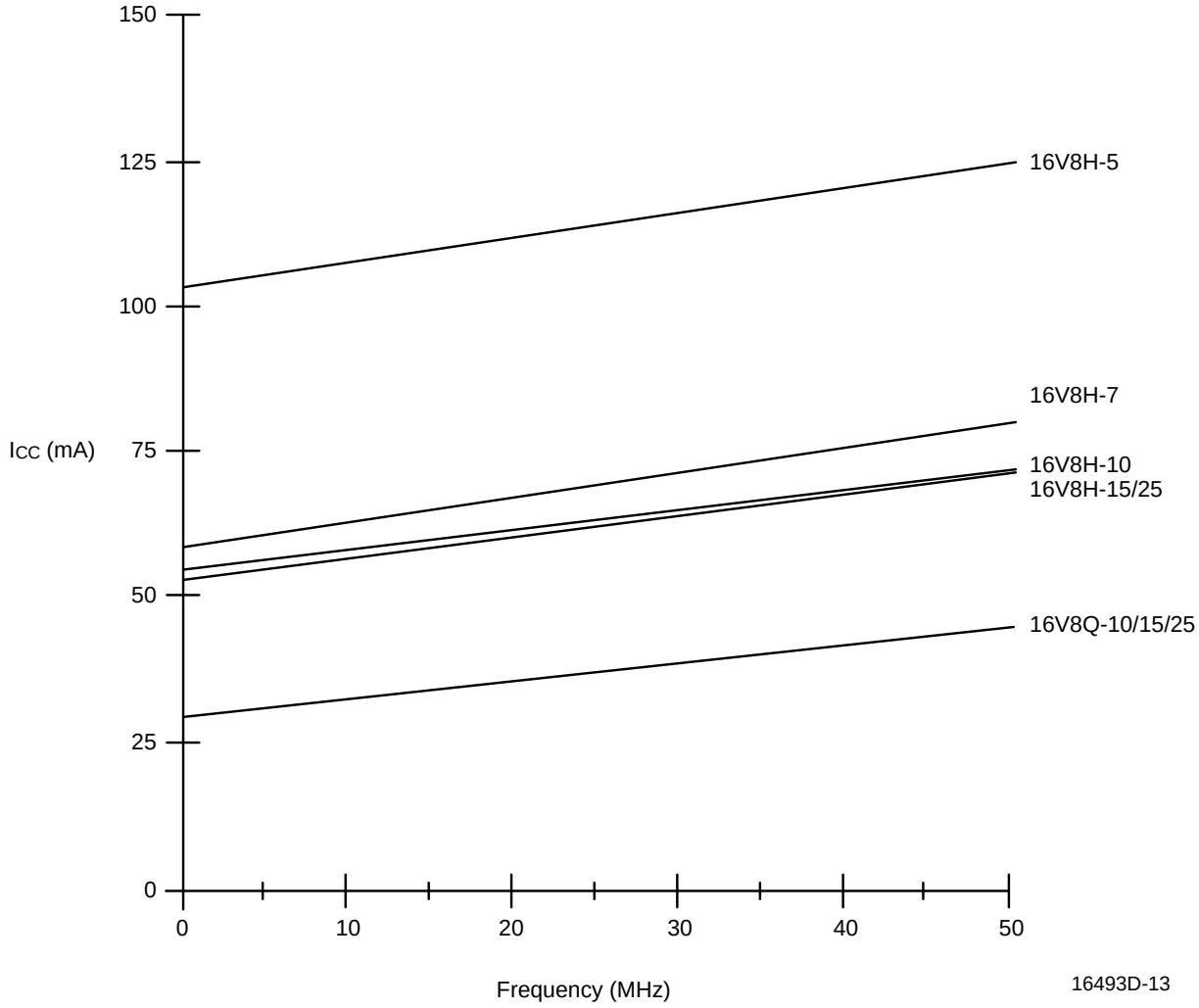


16493D-12

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF		H-5: 200 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

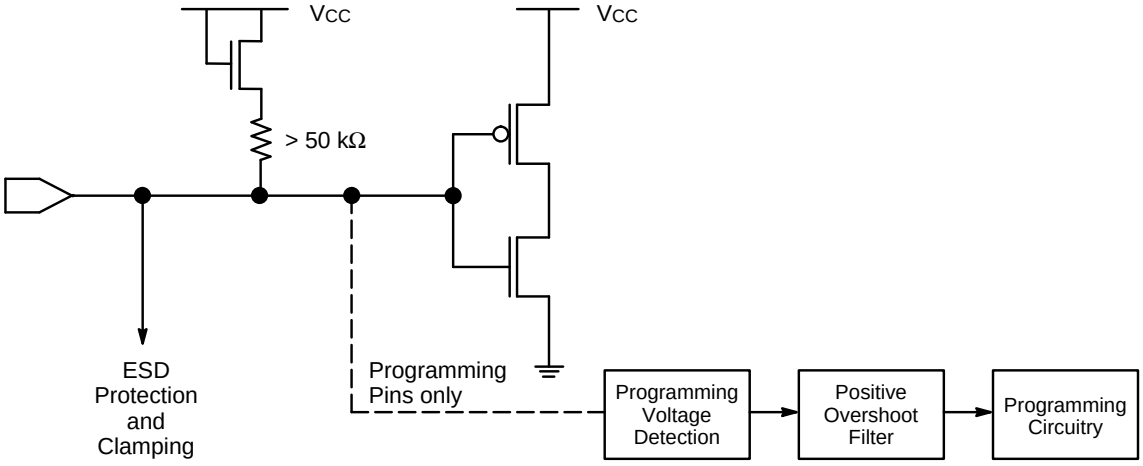
The PALCE16V8 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

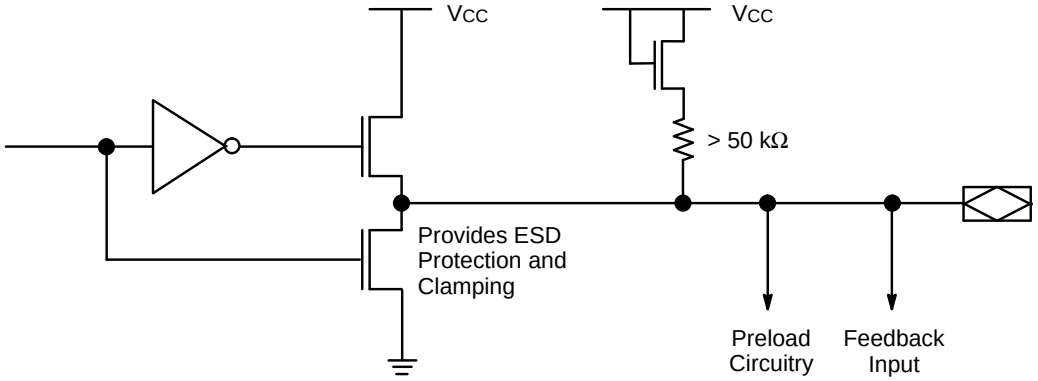
ROBUSTNESS FEATURES

PALCE16V8X-X/5 devices have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 versions. Selected /4 devices are also being retrofitted with these robustness features. See chart below for device listings.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSIONS AND SELECTED /4 VERSIONS*



Typical Input



Typical Output

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*

Device	Rev Letter	
	Filter Only	Filter and Pullups
PALCE16V8H-10	E, F, K	L
PALCE16V8H-15	D, E, F, G, I, J, K	L, M
PALCE16V8Q-15	D, G, J	M
PALCE16V8H-25	D, G, J	M
PALCE16V8Q-25	D, G, J	M

Topside Marking:

AMD CMOS PLD's are marked on the top of the package in the following manner:

PALCEXXXX
Date Code (3 numbers) Lot ID (4 characters)– –(Rev. Letter)

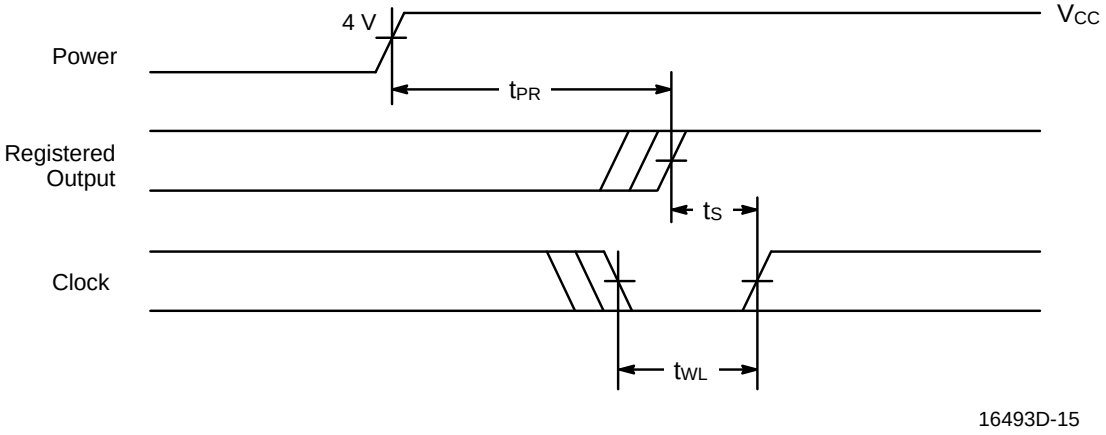
The Lot ID and Rev Letter are separated by two spaces.

POWER-UP RESET

The PALCE16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

/4 Devices (PALCE16V8H-10/4)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			PDIP	PLCC	
θ_{jc}	Thermal Impedance, Junction to Case		25	22	°C/W
θ_{ja}	Thermal Impedance, Junction to Ambient		71	64	°C/W
θ_{jma}	Thermal Impedance, Junction to Ambient with Air Flow	200 lfpm air	61	55	°C/W
		400 lfpm air	55	51	°C/W
		600 lfpm air	51	47	°C/W
		800 lfpm air	47	45	°C/W

/5 Devices (PALCE16V8H-7/5)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			PDIP	PLCC	
θ_{jc}	Thermal Impedance, Junction to Case		29	23	°C/W
θ_{ja}	Thermal Impedance, Junction to Ambient		70	61	°C/W
θ_{jma}	Thermal Impedance, Junction to Ambient with Air Flow	200 lfpm air	64	53	°C/W
		400 lfpm air	58	47	°C/W
		600 lfpm air	53	44	°C/W
		800 lfpm air	X	X	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

PALCE16V8Z FAMILY

Zero-Power 20-Pin EE CMOS Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero-Power CMOS technology**
  - — 15-µA Standby Current (-15/25)
  - — 30-µA Standby Current (-12)
  - — 12-ns propagation delay for "-12" version
  - — 15-ns propagation delay for "-15" version
- **Unused product term disable for reduced power consumption**
- **Available in Industrial operating range**
  - — T_C = –40°C to +85°C
  - — V_{CC} = +4.5 V to +5.5 V
- **HC- and HCT-Compatible inputs and outputs**
- **Pin and function compatible with all 20-pin GAL devices**
- **Electrically-erasable CMOS technology provides reconfigurable logic and full testability**
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP and PLCC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

The PALCE16V8Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8Z will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

The PALCE16V8Z provides zero standby power and high speed. At 30-µA maximum standby current, the PALCE16V8Z allows battery powered operation for an extended period.

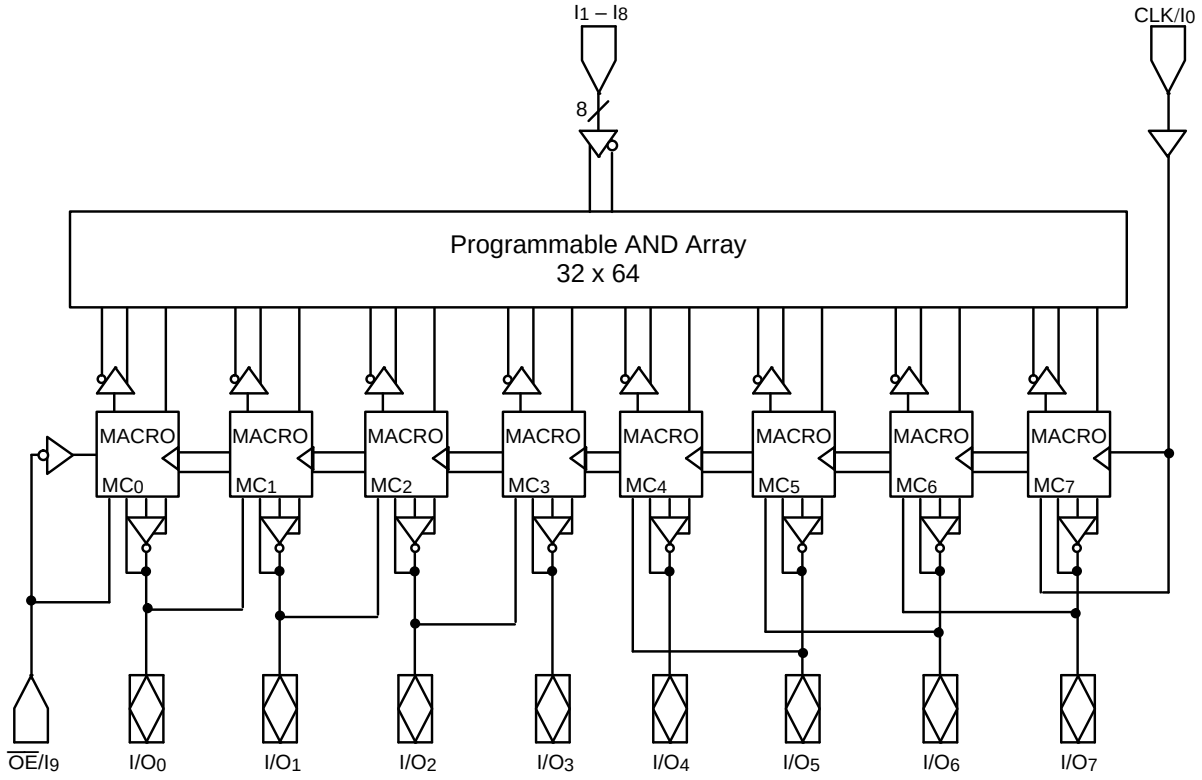
The PALCE16V8Z utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE16V8Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar.

Publication# **13061** Rev. **E** Amendment **/0**
Issue Date: **February 1996**

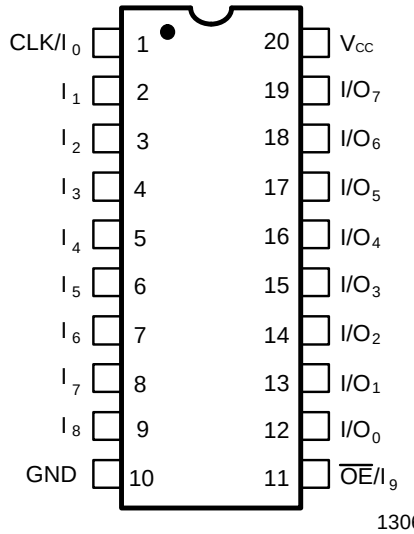
BLOCK DIAGRAM



13061E-1

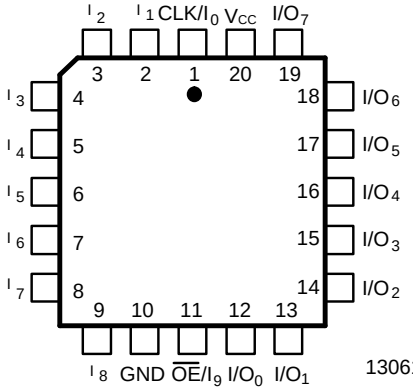
CONNECTION DIAGRAMS
Top View

DIP



13061E-2

PLCC



13061E-3

Note:
Pin 1 is marked for orientation

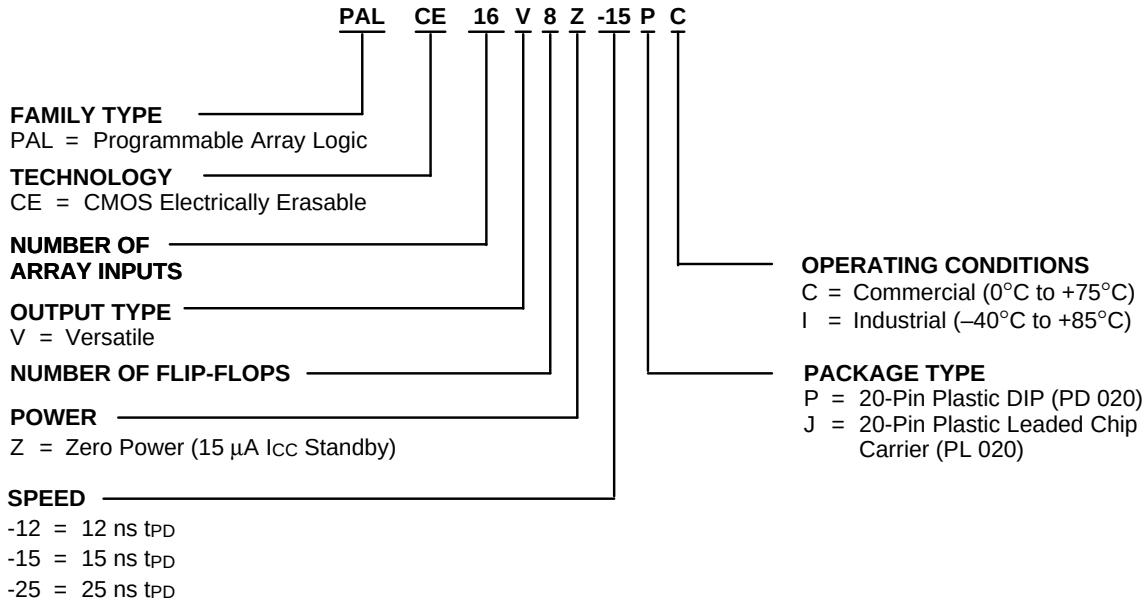
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
$\overline{OE}$ = Output Enable
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE16V8Z-12	PI, JI
PALCE16V8Z-15	PI, JI, PC, JC
PALCE16V8Z-25	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

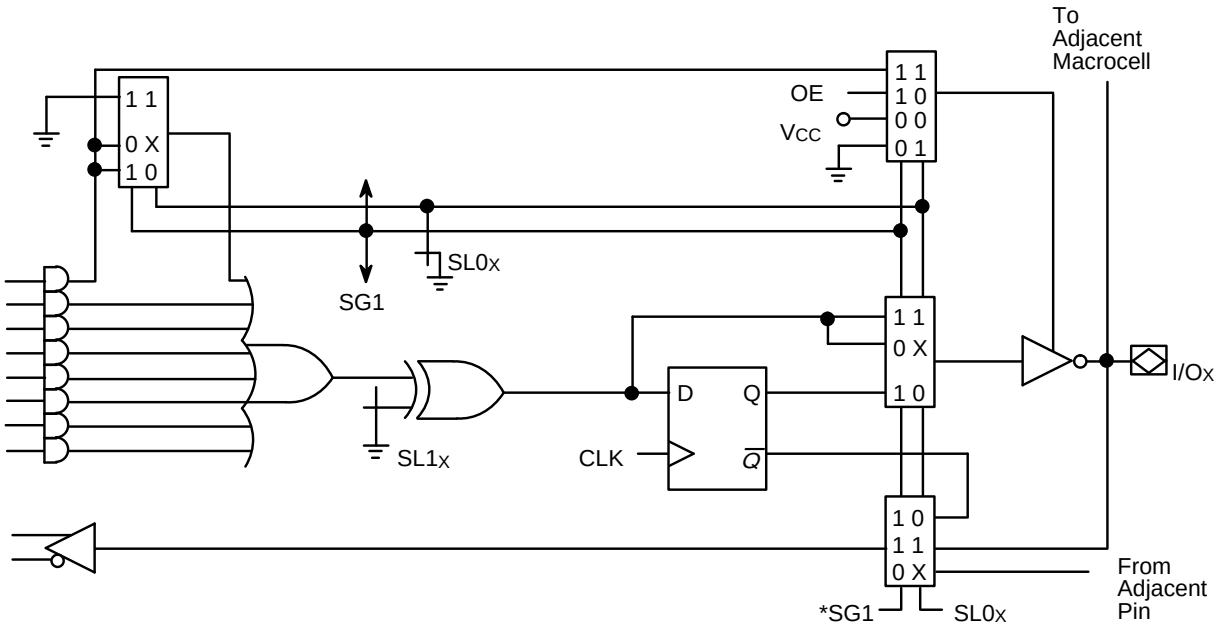
The PALCE16V8Z is the zero-power version of the PALCE16V8. It has all the architectural features of the PALCE16V8. In addition, the PALCE16V8Z has zero standby power and unused product term disable.

The PALCE16V8Z is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8Z are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8Z. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8Z. The programmer will program the PALCE16V8Z in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8Z. Here the user must use the PALCE16V8Z device code. This option allows full utilization of the macrocell.



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**In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

Figure 1. PALCE16V8Z Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8Z will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8Z has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of MC_3 and MC_4. MC_3 and MC_4 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

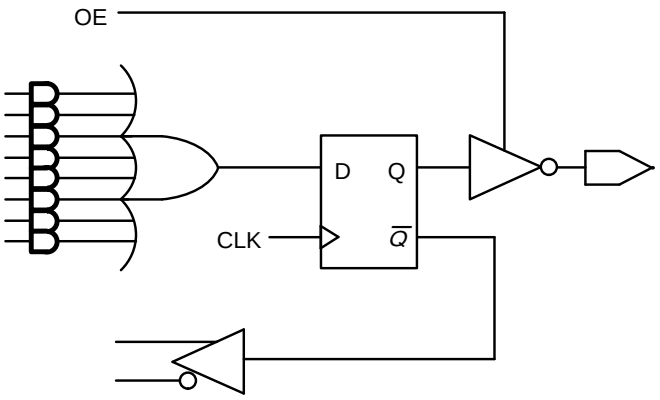
Table 1. Macrocell Configuration

SG0	SG1	SL0x	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

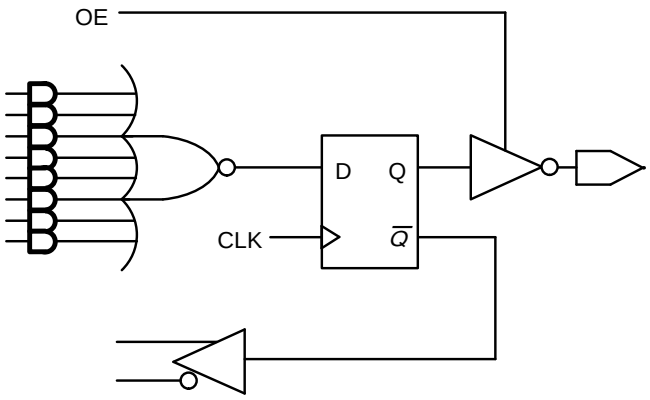
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save “DeMorganizing” efforts.

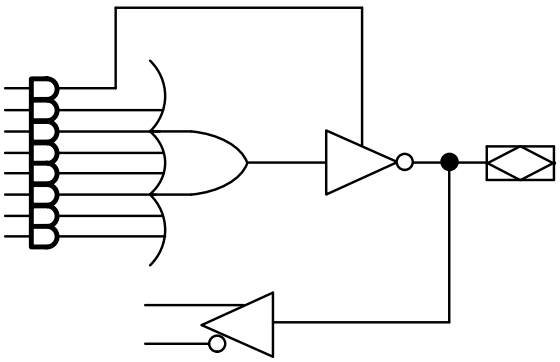
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



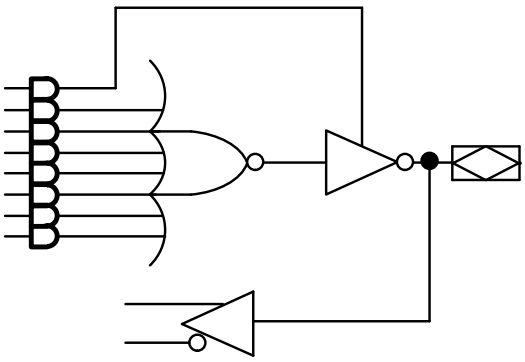
Registered Active Low



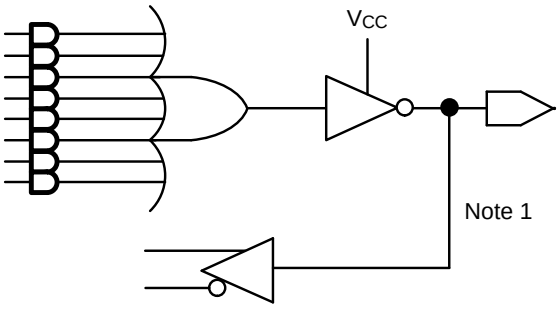
Registered Active High



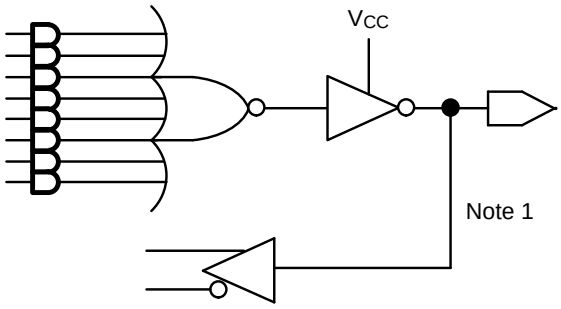
Combinatorial I/O Active Low



Combinatorial I/O Active High



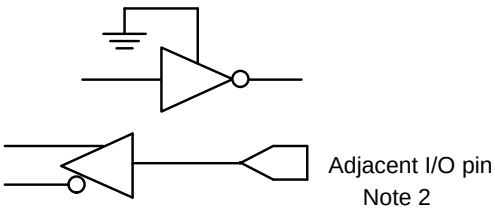
Combinatorial Output Active Low



Combinatorial Output Active High

Notes:

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *The dedicated-input configuration is not available on pins 15 and 16.*



Dedicated Input

13061E-5

Figure 2. Macrocell Configurations

Zero-Standby Power Mode

The PALCE16V8Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE16V8Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero (I_{CC} < 15 μA). The outputs will maintain the states held before the device went into the standby mode. There is no speed penalty associated with coming out of standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the I_{CC} vs. frequency graph.

Product-Term Disable

On a programmed PALCE16V8Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs frequency graph, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note, “Minimizing Power Consumption with Zero-Power PLDs”.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8Z will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function is not disabled by the security bit. This allows functional testing after the security bit is programmed.

Security Bit

A security bit is provided on the PALCE16V8Z as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8Z device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

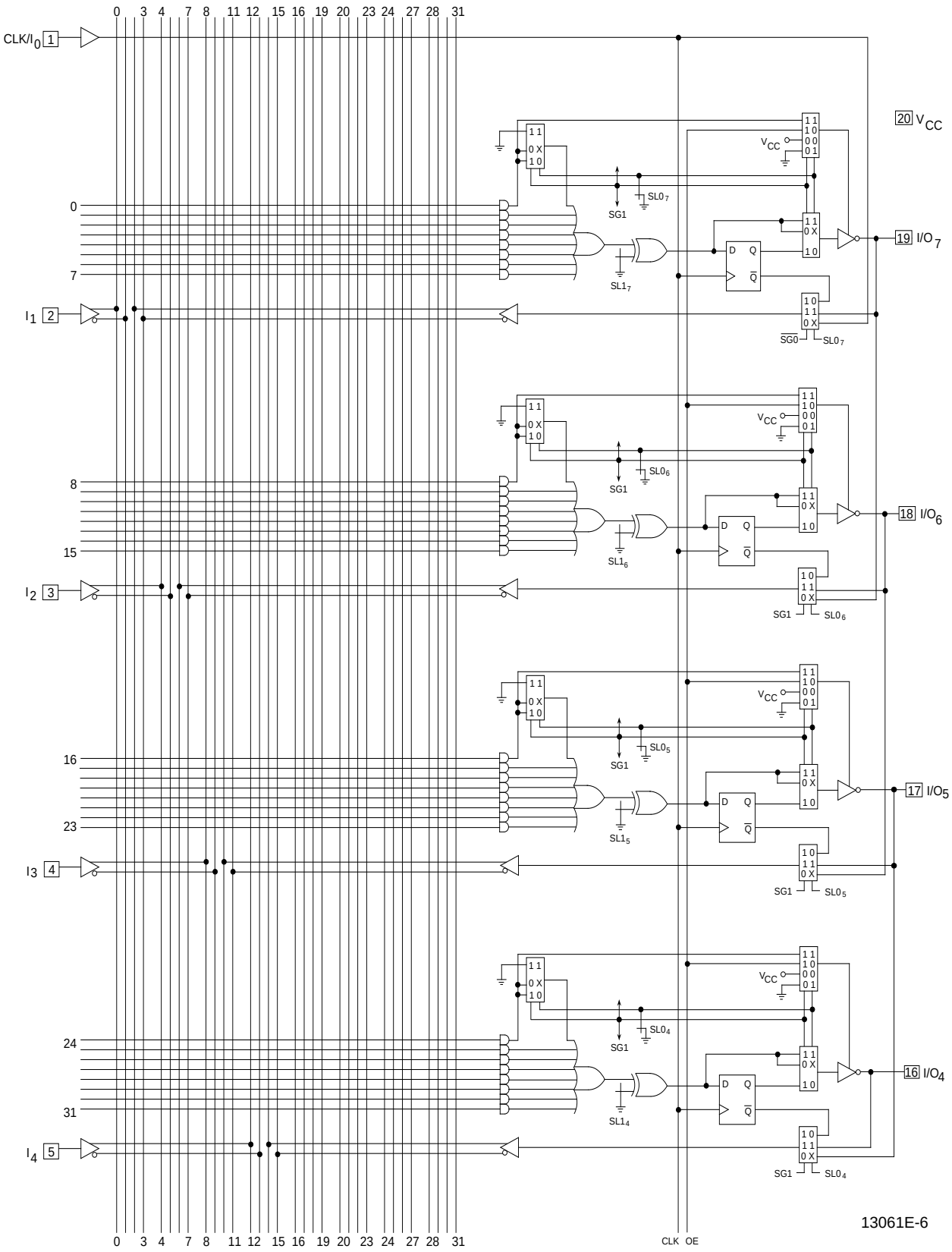
Quality and Testability

The PALCE16V8Z offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

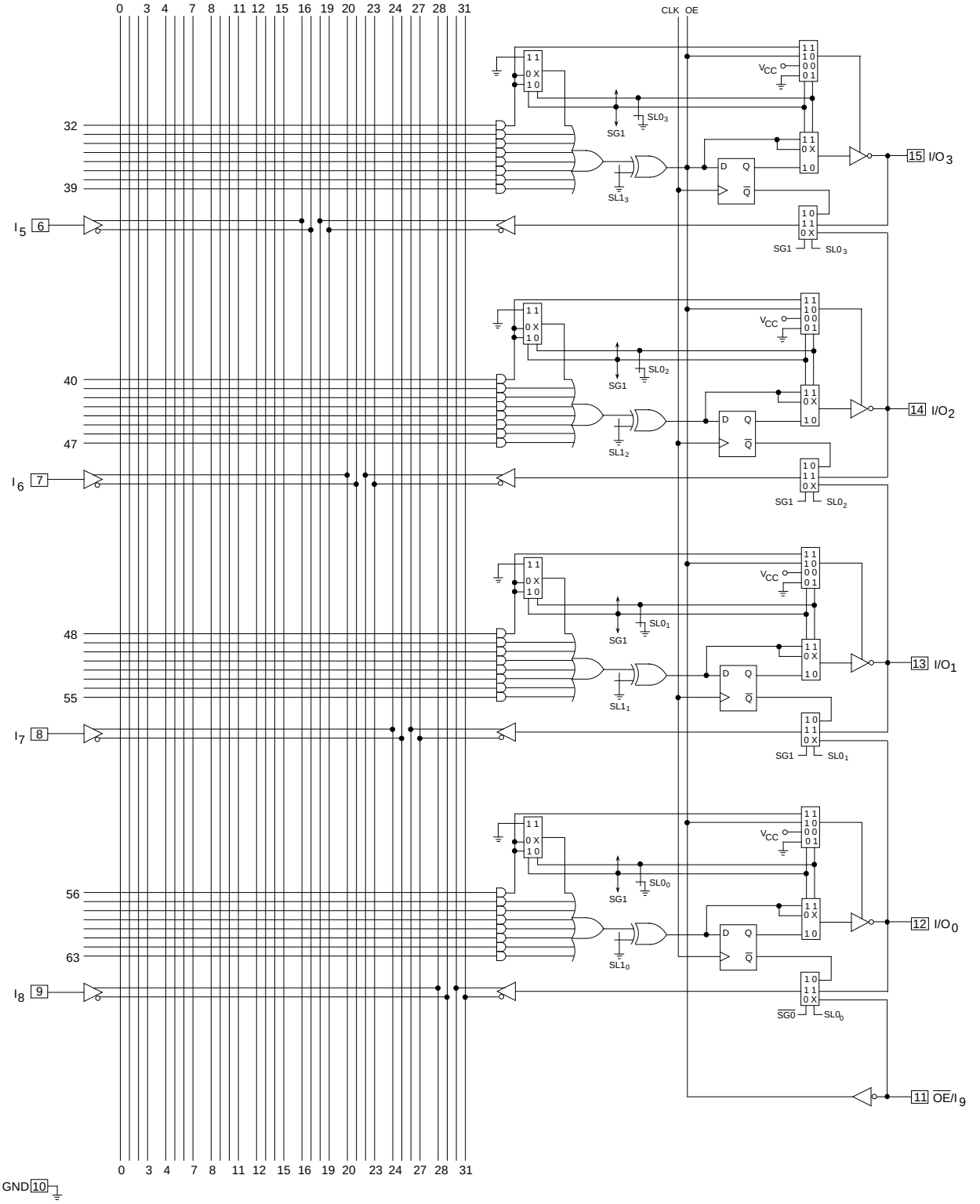
Technology

The high-speed PALCE16V8Z is fabricated with AMD’s advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



13061E-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Ambient Temperature
with Power Applied . . . . . –55°C to +125°C
Supply Voltage with
Respect to Ground . . . . . –0.5 V to + 7.0 V
DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V
DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage . . . . . 2001 V
Latchup Current
(T_A = –40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case
Temperature (T_C) . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current (Static)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	f = 0 MHz		30	µA
	Supply Current (Dynamic)		f = 15 MHz		75	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			(Note 5) Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				12	ns
t_S	Setup Time from Input or Feedback to Clock			8		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				8	ns
t_{WL}	Clock Width	LOW		5		ns
t_{WH}		HIGH		5		ns
f_{MAX}	Maximum Frequency (Notes 4 and 6)	External Feedback	$1/(t_S + t_{CO})$	62.5		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	77		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				8	ns
t_{EA}	Input to Output Enable Using Product Term Control				13	ns
t_{ER}	Input to Output Disable Using Product Term Control				13	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *This parameter is tested in standby mode.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *Output delay minimum for t_{PD}, t_{CO}, t_{PZD}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
6. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Ambient Temperature
with Power Applied . . . . . –55°C to +125°C
Supply Voltage with
Respect to Ground . . . . . –0.5 V to + 7.0 V
DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V
DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage . . . . . 2001 V
Latchup Current
(T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Operating Case
Temperature (T_C) . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current (Static)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	f = 0 MHz		15	µA
	Supply Current (Dynamic)		f = 25 MHz		75	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input or Feedback to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15	ns
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Ambient Temperature
with Power Applied . . . . . –55°C to +125°C
Supply Voltage with
Respect to Ground . . . . . –0.5 V to + 7.0 V
DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V
DC Output or I/O
Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage . . . . . 2001 V
Latchup Current
(T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Operating Case
Temperature (T_C) . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	V_{CC} – 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	I_{OL} = 24 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max (Note 4)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max	f = 0 MHz		15	µA
			f = 25 MHz		90	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

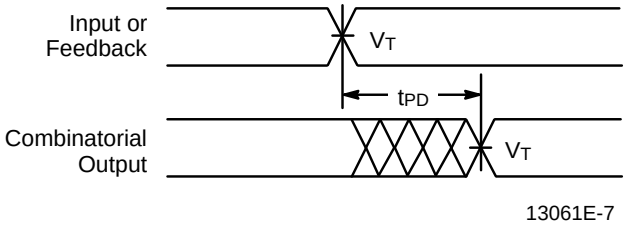
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input or Feedback to Clock			20		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Notes 4 and 5)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	50		MHz
		No Feedback	$1/(t_S + t_H)$	50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				25	ns
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

Notes:

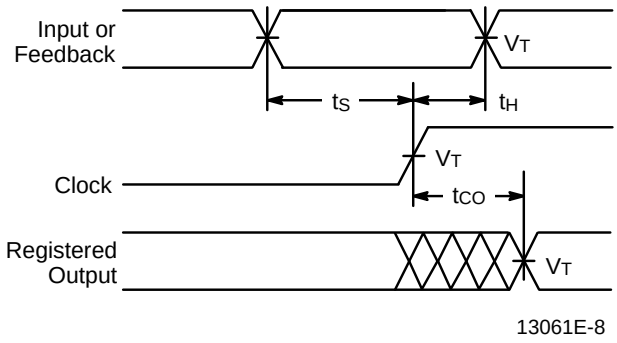
2. *See Switching Test Circuit for test conditions.*
3. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 2 ns faster.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

SWITCHING WAVEFORMS



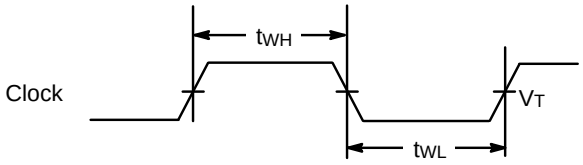
13061E-7

Combinatorial Output



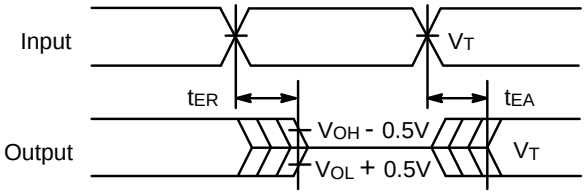
13061E-8

Registered Output



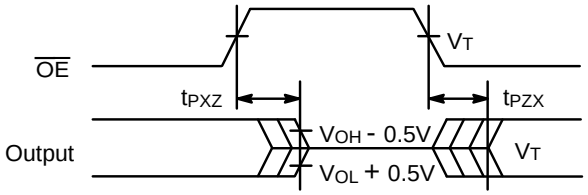
13061E-9

Clock Width



13061E-10

Input to Output Disable/Enable



13061E-11

$\overline{OE}$ to Output Disable/Enable

Notes:

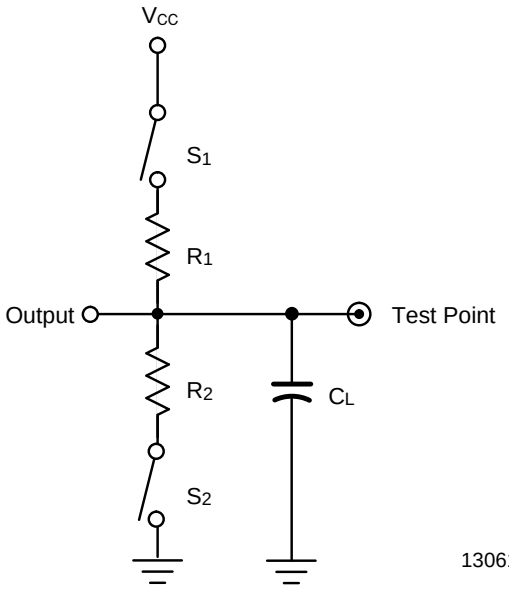
1. *V_T = 1.5 V for input signals and $V_{CC}/2$ for output signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

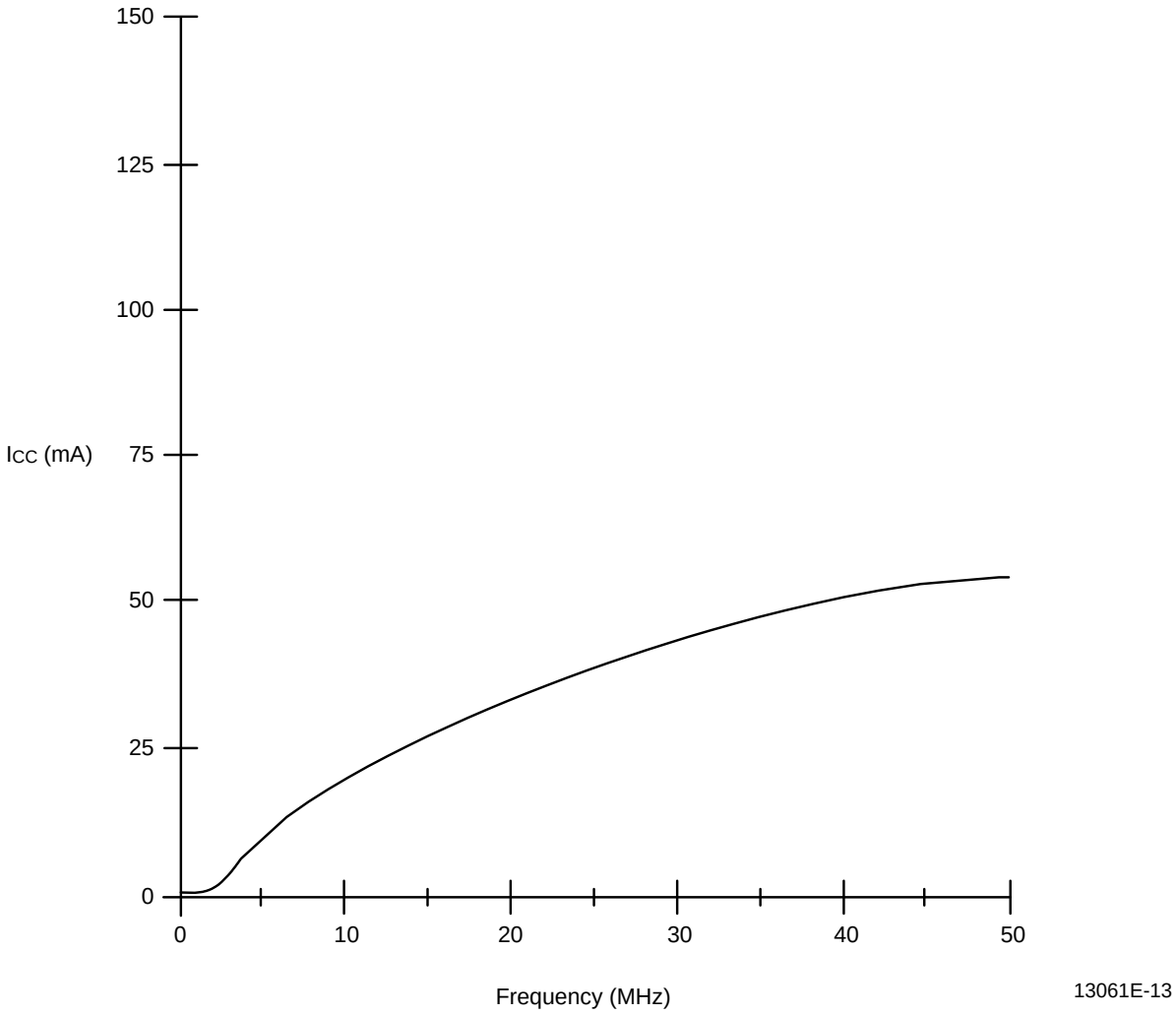


13061E-12

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	820 Ω	820 Ω	$V_{CC}/2$
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				$V_{CC}/2$
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE16V8Z-12/15

V_{CC} = 5.0 V, T_A = 25°C



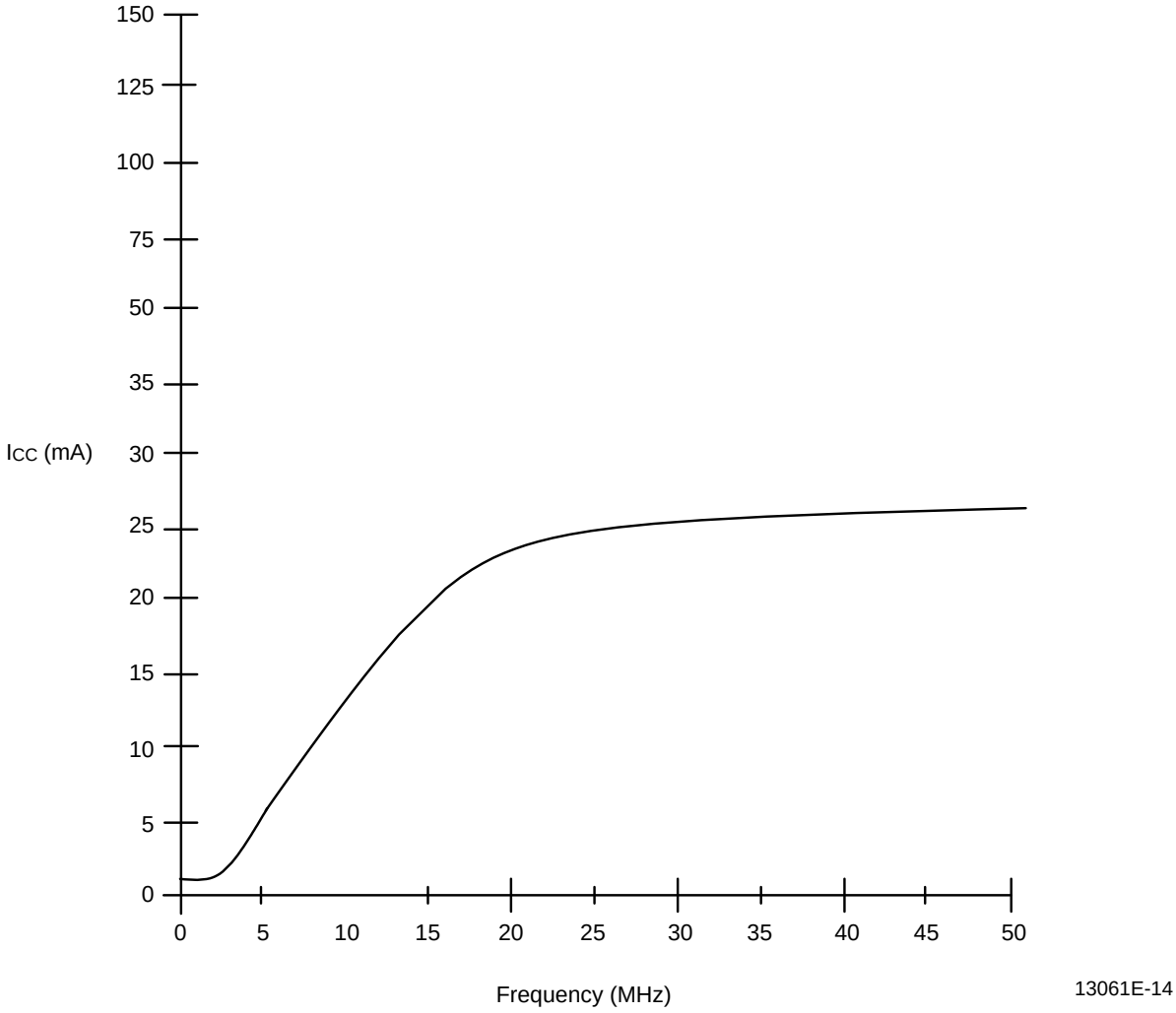
I_{CC} vs. Frequency
Graph for the PALCE16V8Z-12/15

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE16V8Z-25

V_{CC} = 5.0 V, T_A = 25°C



I_{CC} vs. Frequency
Graph for the PALCE16V8Z-25

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

The PALCE16V8Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

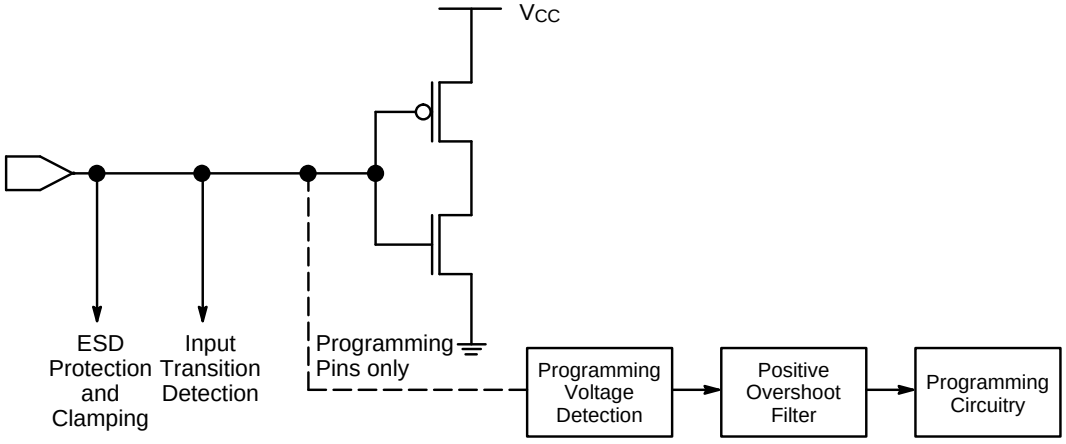
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

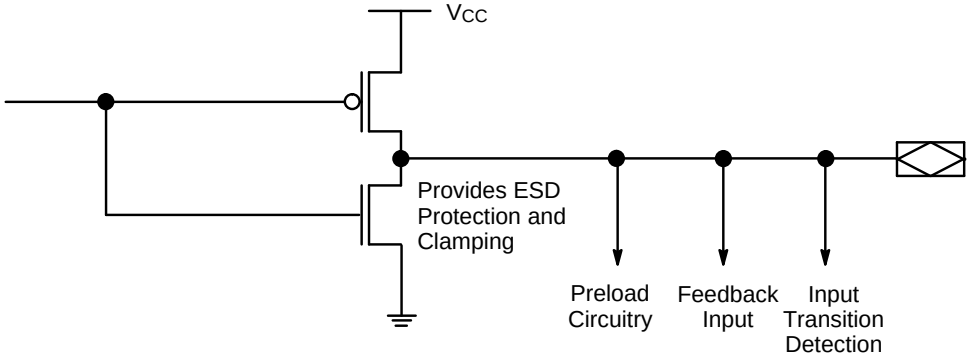
ROBUSTNESS FEATURES

The PALCE16V8Z has some unique features that make it extremely robust, especially when operating in high-speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

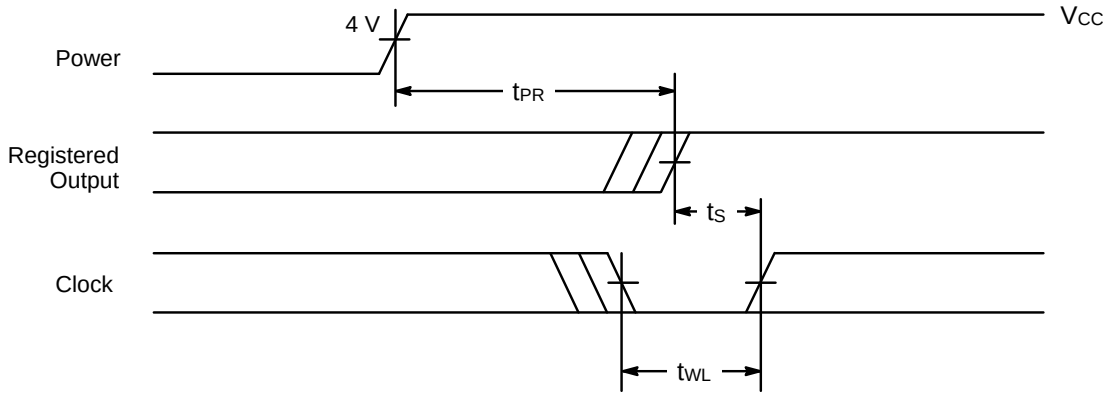
13061E-16

POWER-UP RESET

The PALCE16V8Z has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



13061E-17

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

PALCE16V8Z-25

Parameter Symbol	Parameter Description		Typ PDIP	Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		20	19	°C/W
θ_{ja}	Thermal impedance, junction to ambient		65	57	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	58	41	°C/W
		400 lfpm air	51	37	°C/W
		600 lfpm air	47	35	°C/W
		800 lfpm air	44	33	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

PALCE20V8 Family

EE CMOS 24-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Pin and function compatible with all GAL 20V8/As**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - — 5-ns propagation delay for "-5" version
  - — 7.5-ns propagation delay for "-7" version
- **Direct plug-in replacement for a wide range of 24-pin PAL devices**
- **Programmable enable/disable control**
- **Outputs individually programmable as registered or combinatorial**
- **Peripheral Component Interconnect (PCI) compliant**
- **Preloadable output registers for testability**
- **Automatic register reset on power-up**
- **Cost-effective 24-pin plastic SKINNYDIP and 28-pin PLCC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**
- **Programmable output polarity**
- **5-ns version utilizes a split leadframe for improved performance**

GENERAL DESCRIPTION

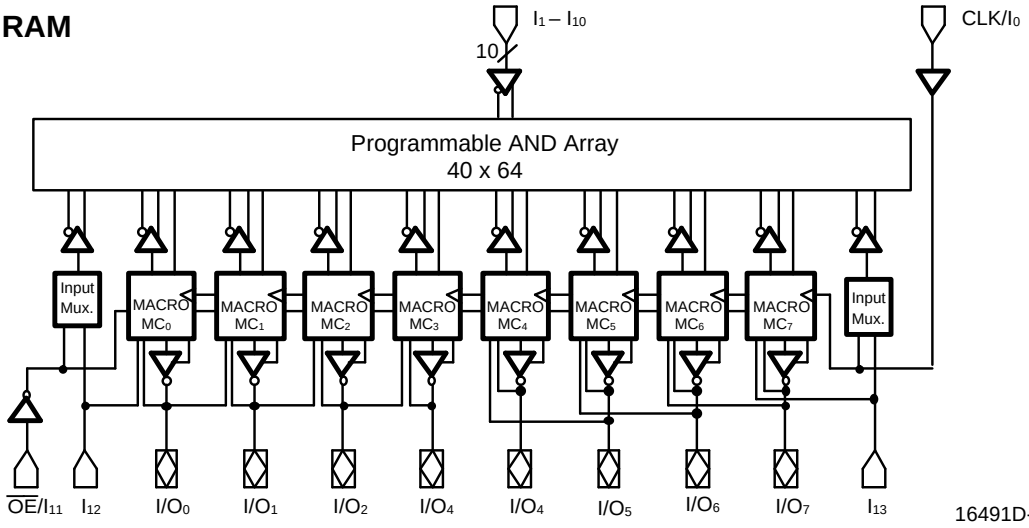
The PALCE20V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture. The PALCE20V8 is fully compatible with the GAL20V8 and can directly replace PAL20R8 series devices and most 24-pin combinatorial PAL devices.

Device logic is automatically configured according to the user's design specification. A design is implemented using any of a number of popular design software packages, allowing automatic creation of a programming file based on Boolean or state equations. Design software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE20V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

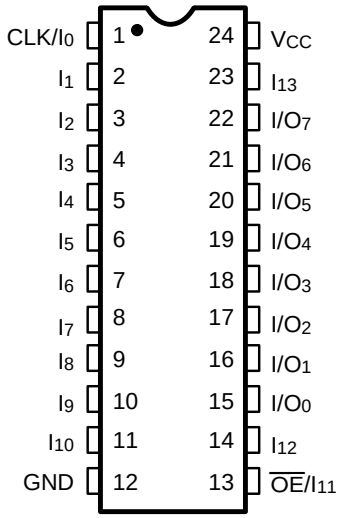
BLOCK DIAGRAM



16491D-1

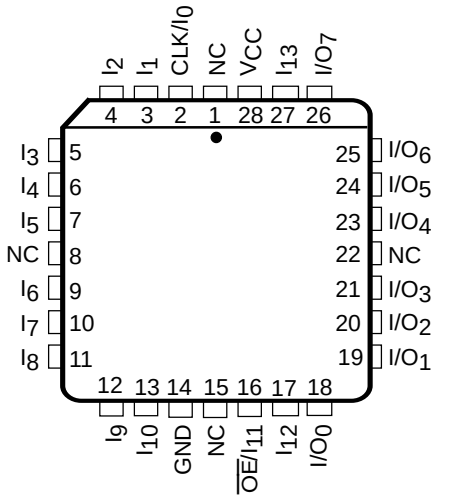
CONNECTION DIAGRAMS
(Top View)

SKINNYDIP



16491D-2

PLCC/LCC



16491D-3

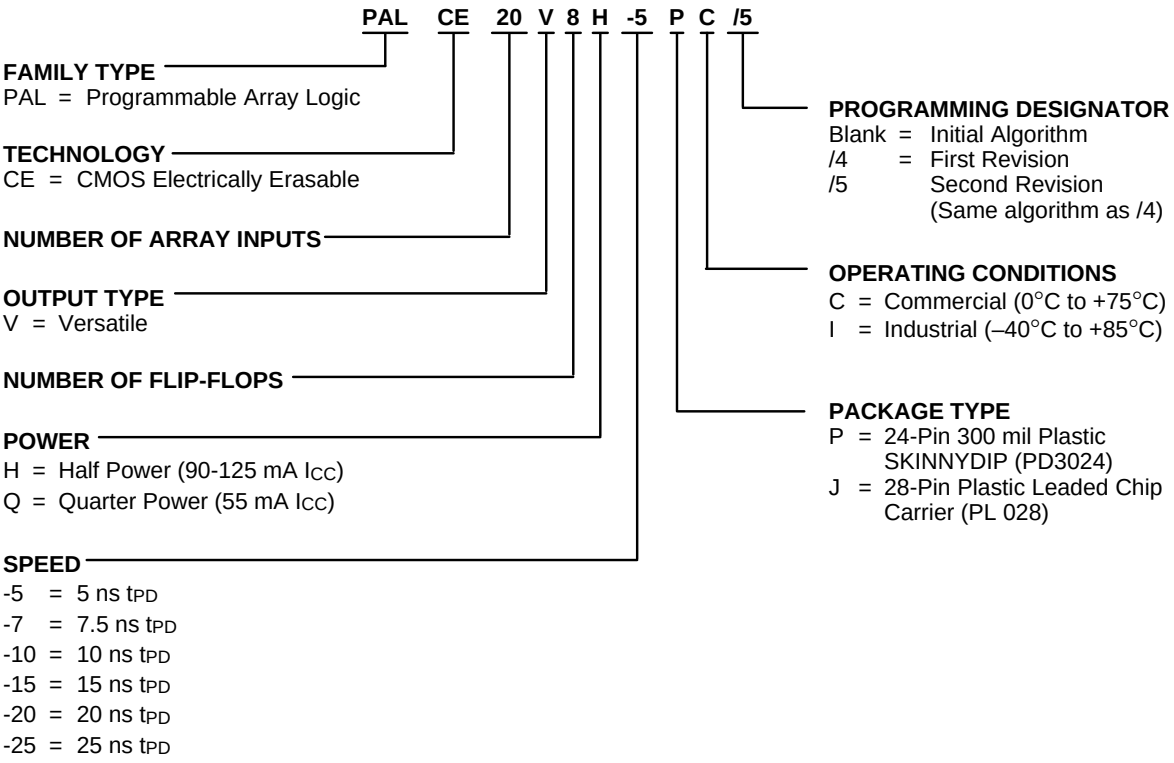
***Note**:*
Pin 1 is marked for orientation.

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
$\overline{OE}$ = Output Enable
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE20V8H-5	JC	/5
PALCE20V8H-7	PC, JC	
PALCE20V8H-10		Blank, /4
PALCE20V8Q-10		/5
PALCE20V8H-15	PC, JC, PI, JI	Blank, /4
PALCE20V8Q-15	PC, JC	
PALCE20V8Q-20	PI, JI	
PALCE20V8H-25	PC, JC, PI, JI	
PALCE20V8Q-25		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

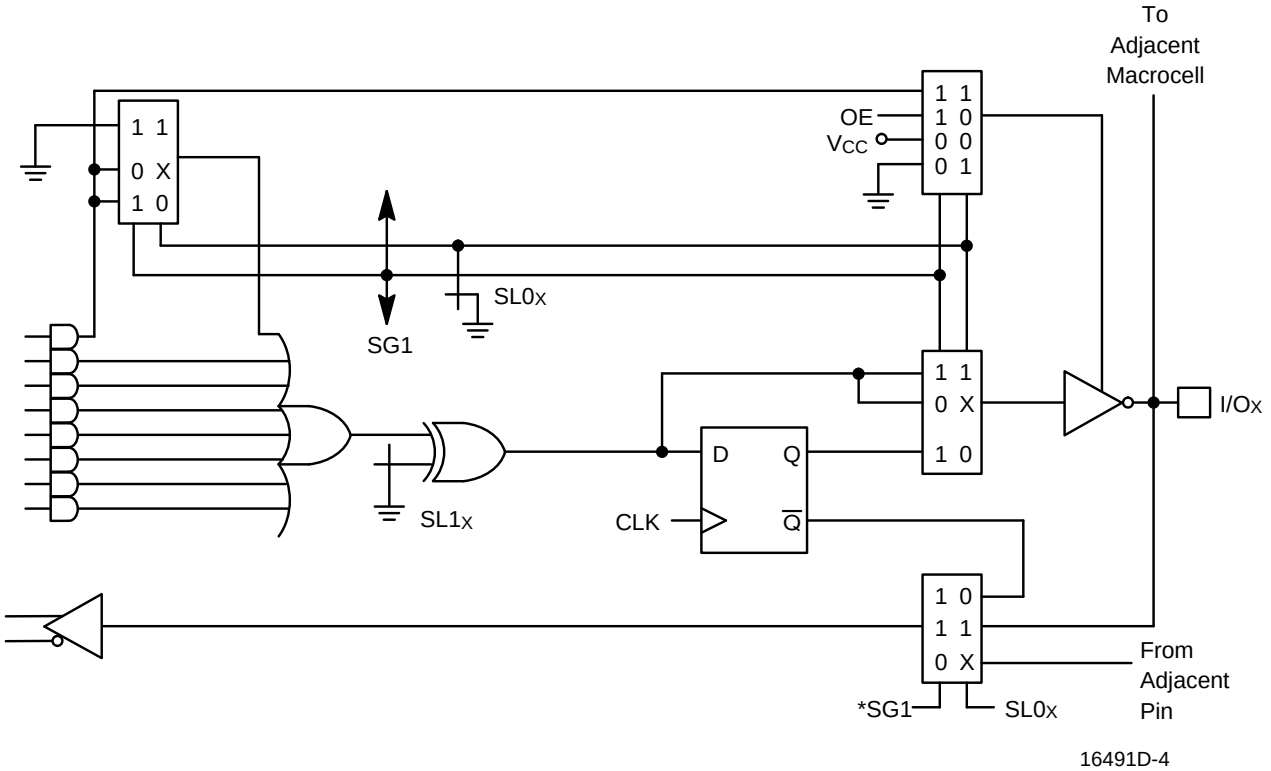
FUNCTIONAL DESCRIPTION

The PALCE20V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0..MC_7). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 13 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE20V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE20V8. First, it can be programmed as an emulated PAL device. This includes the PAL20R8 series and most 24-pin combinatorial PAL devices. The PAL device programmer manufacturer will supply device codes for the standard PAL architectures to be used with the PALCE20V8. The programmer will program the PALCE20V8 to the corresponding PAL device architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed directly as a PALCE20V8. Here the user must use the PALCE20V8 device code. This option provides full utilization of the macrocells, allowing non-standard architectures to be built.



** In Macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

Figure 1. PALCE20V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled. A macrocell configured as a dedicated input derives the input signal from an adjacent I/O.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE20V8 will emulate a PAL20R8 family or a combinatorial device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer.

These configurations are summarized in table 1 and illustrated in figure 2.

If the PALCE20V8 is configured as a combinatorial device, the CLK and $\overline{OE}$ pins may be available as inputs to the array. If the device is configured with registers, the CLK and $\overline{OE}$ pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. $SL1_x$ is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE20V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 18(21) and 19(23). Pins 18(21) and 19(23) do not use feedback in this mode.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. The feedback signal is an adjacent I/O pin.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0,SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

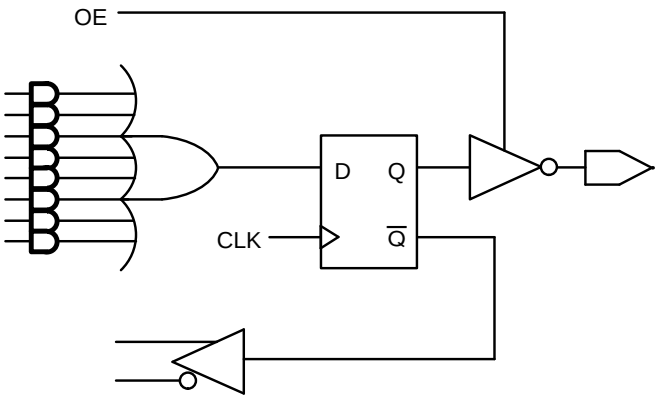
Table 1. Macrocell Configurations

SG0	SG1	$SL0_x$	Cell Configuration	Devices Emulated
Device has registers				
0	1	0	Registered Output	PAL20R8, 20R6, 20R4
0	1	1	Combinatorial I/O	PAL20R6, 20R4
Device has no registers				
1	0	0	Combinatorial Output	PAL20L2, 18L4,16L6,14L8
1	0	1	Dedicated Input	PAL20L2,18L4, 16L6
1	1	1	Combinatorial I/O	PAL20L8

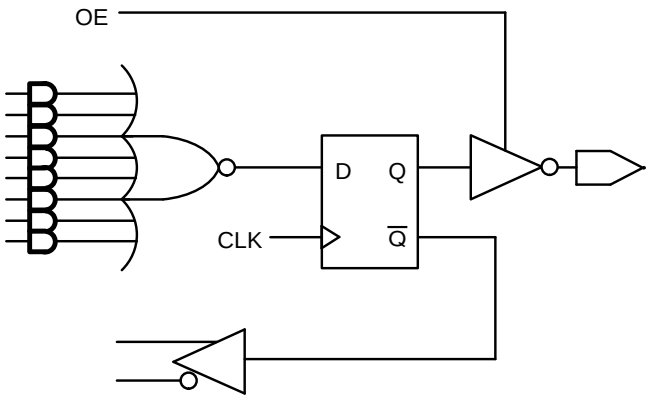
Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save “DeMorganizing” efforts.

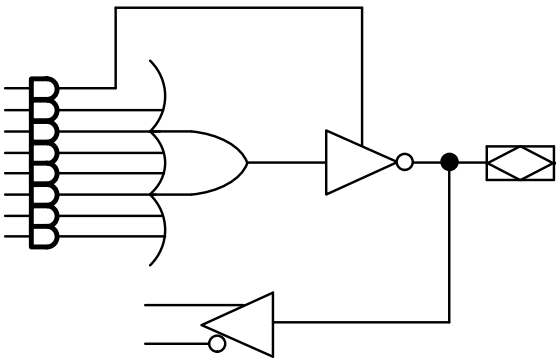
Selection is made through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is a 0 and active low if $SL1_x$ is a 1.



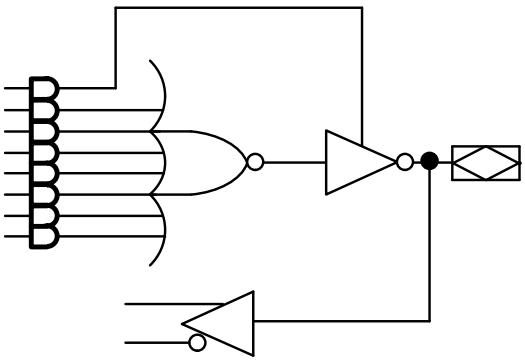
Registered Active Low



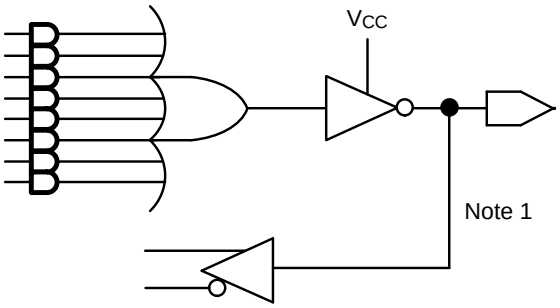
Registered Active High



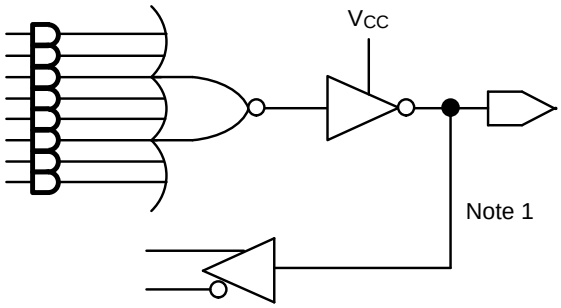
Combinatorial I/O Active Low



Combinatorial I/O Active High



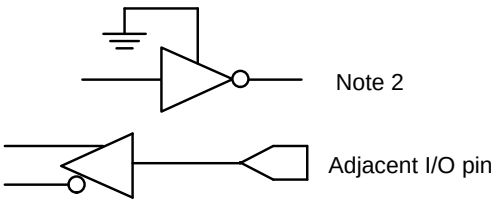
Combinatorial Output Active Low



Combinatorial Output Active High

Notes:

1. *Feedback is not available on pins 18 (21) and 19 (23) in the combinatorial output mode.*
2. *This macrocell configuration is not available on pins 18 (21) and 19 (23).*



Dedicated Input

16491D-5

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE20V8 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE20V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE20V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE20V8. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE20V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALCE20V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming and post-programming functional yields in the industry.

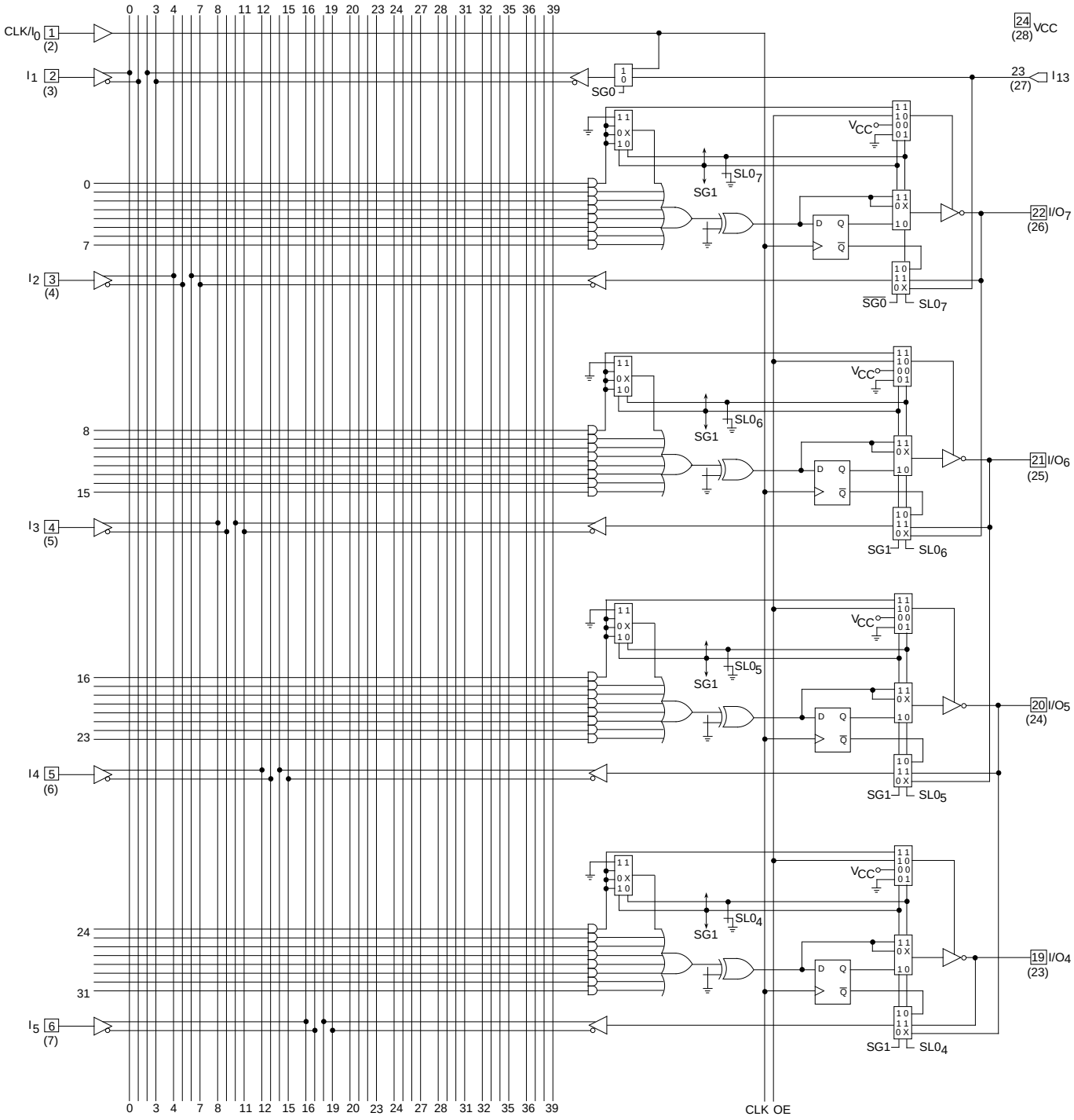
Technology

The high-speed PALCE20V8H is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

PCI Compliance

The PALCE20V8H-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The PALCE20V8H-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.

LOGIC DIAGRAM
SKINNYDIP (PLCC and LCC) Pinouts



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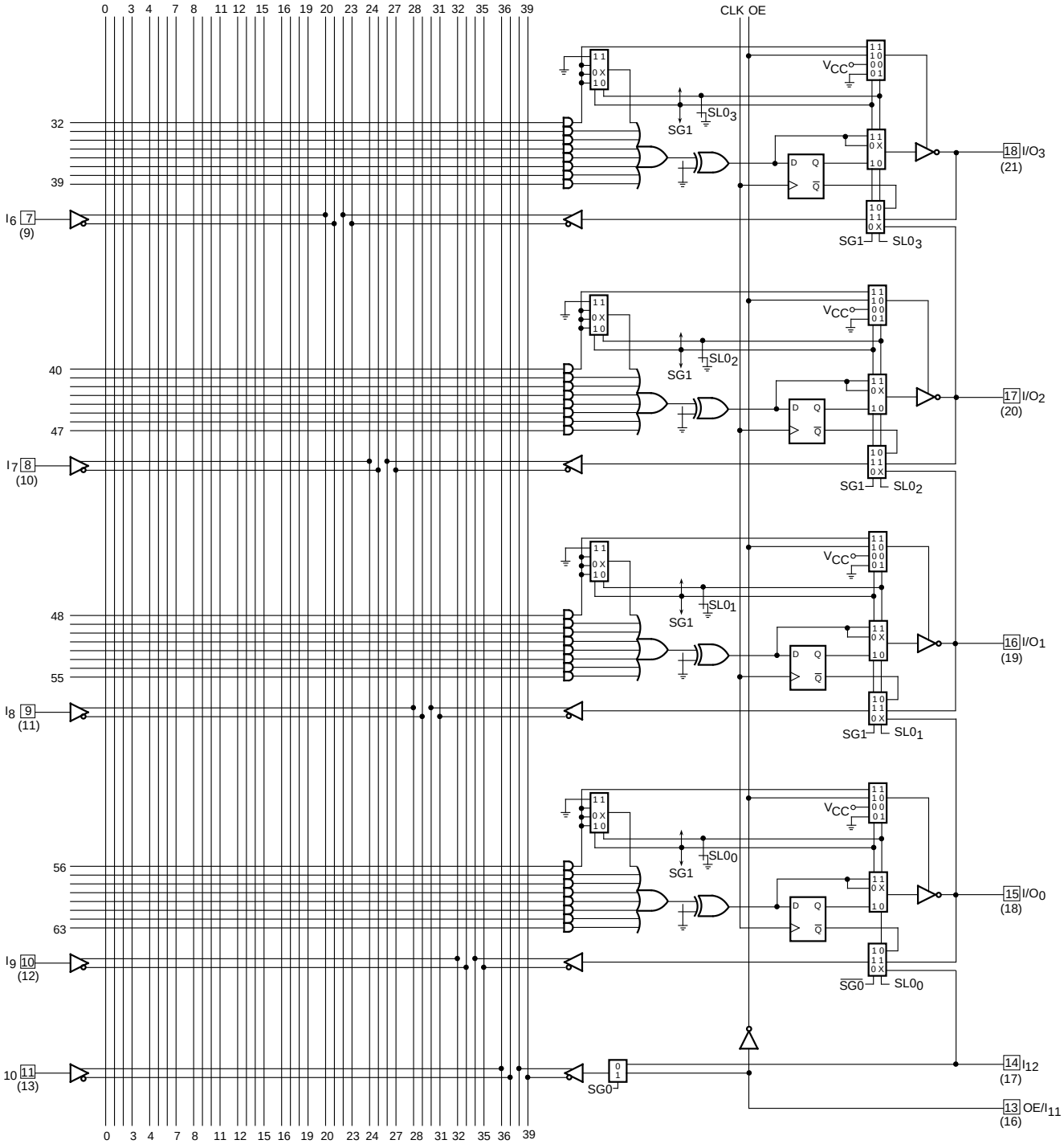
LOGIC DIAGRAM (continued)
SKINNYDIP (PLCC and LCC) Pinouts



16491D-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Static)	Supply Current	Outputs Open (I_{OUT} = 0 mA), V_{IN} = 0 V V_{CC} = Max		125	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 5)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	5	ns
t_S	Setup Time from Input or Feedback to Clock			3		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)				1	ns
t_{WL}	Clock Width	LOW		3		ns
t_{WH}		HIGH		3		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	142.8		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 6)	166		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	166		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			2	6	ns
t_{ER}	Input to Output Disable Using Product Term Control			2	5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
6. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

***Note*:**

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output		8 Outputs Switching	3	7.5	ns
			1 Output Switching	3	7	ns
t_S	Setup Time from Input or Feedback to Clock			5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)				1	ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	100		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 6)	125		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			1	6	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			1	6	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	9	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
6. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 25 MHz		115	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 4)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	71.4		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to 75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–150	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz (Note 4)		55	mA

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case under test conditions. Refer to the I_{CC} vs. frequency graph for typical measurements.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min (Note 4)	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			3	7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	71.4		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable			2	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable			2	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			3	10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or
I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
(T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	45.5		37		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	50		40		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or
I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
(T_A = –40°C to +85°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Temperature (T_A) Operating
in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max, f = 15 MHz	H		130	mA
			Q		65	

Notes:

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

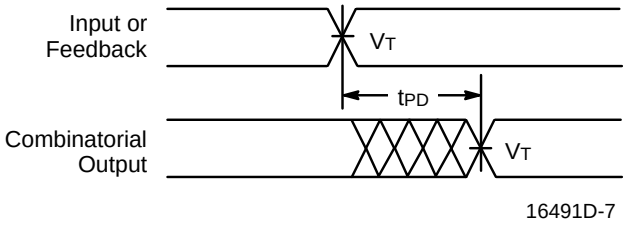
SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-20		-25		Unit
				Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		20		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		13		15		ns
t_H	Hold Time			0		0		0		ns
t_{CO}	Clock to Output				10		11		12	ns
t_{WL}	Clock Width	LOW		8		10		12		ns
t_{WH}		HIGH		8		10		12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	45.5		41.6		37		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	50		45.4		40		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		50.0		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		18		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		18		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		18		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		18		20	ns

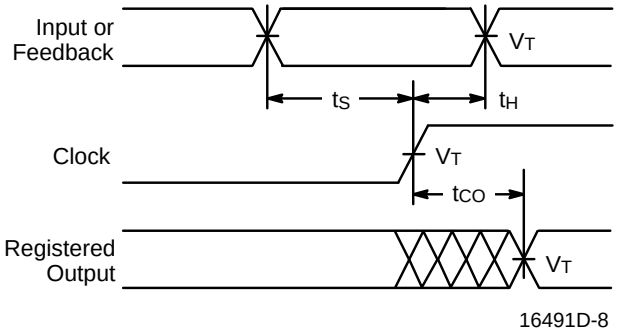
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

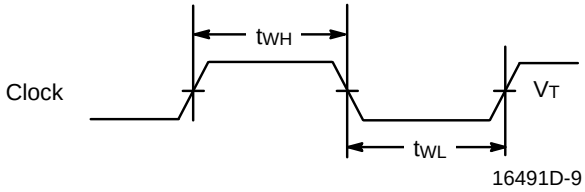
SWITCHING WAVEFORMS



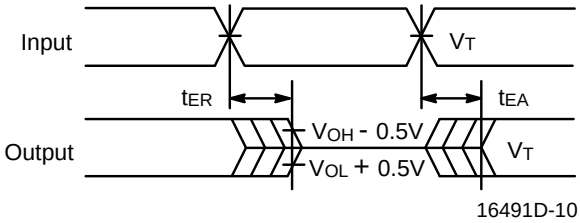
Combinatorial Output



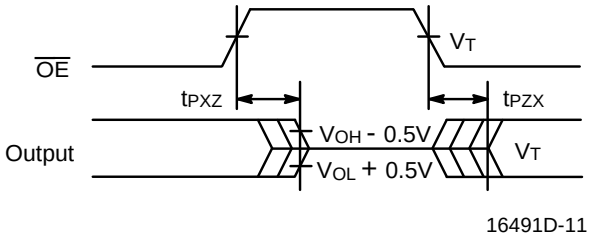
Registered Output



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

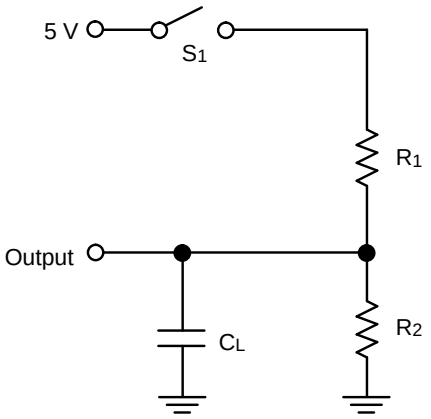
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



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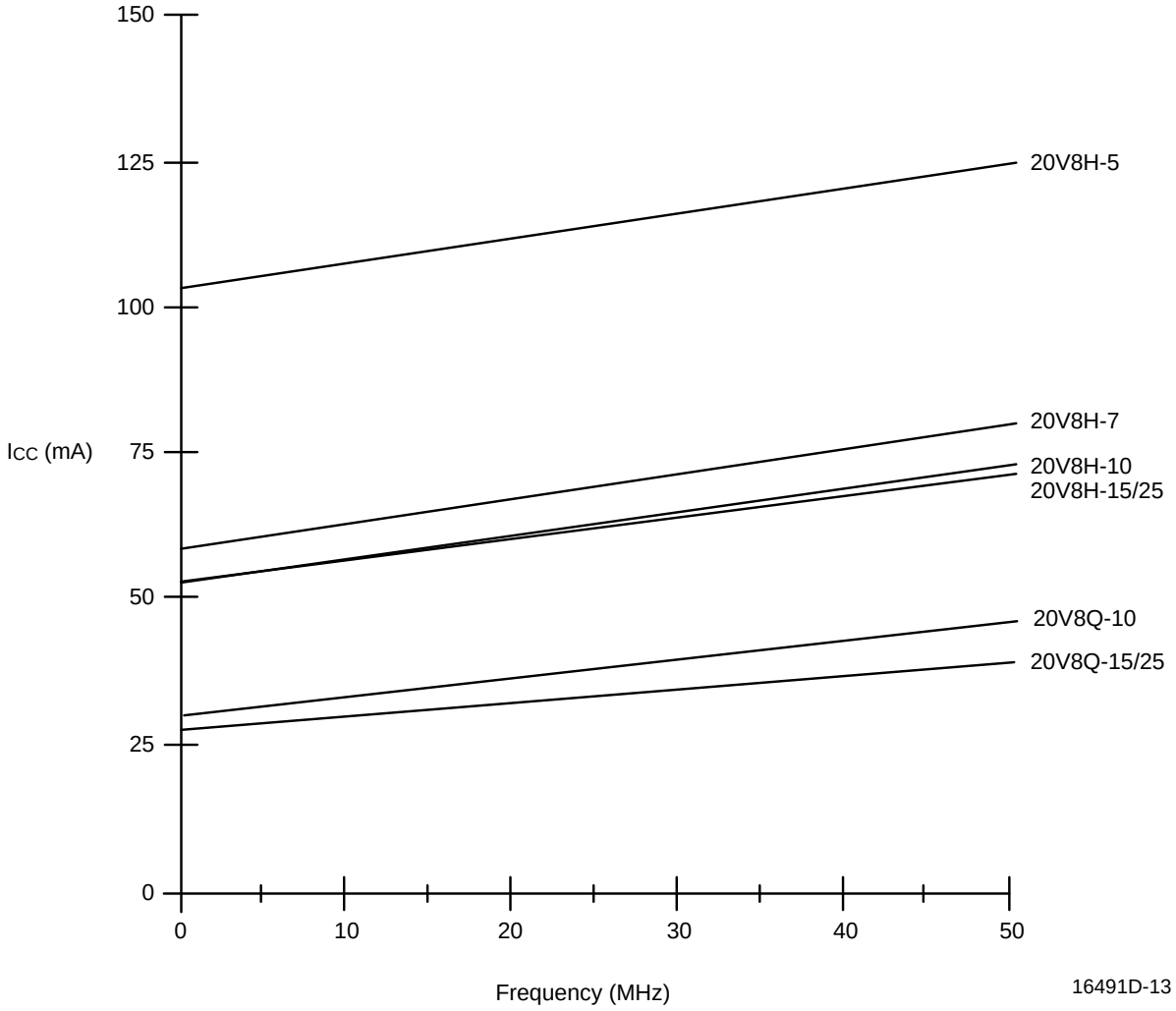
Switching Test Circuit

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF		H-5: 200 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5.0 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

The PALCE20V8 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Endurance Characteristics

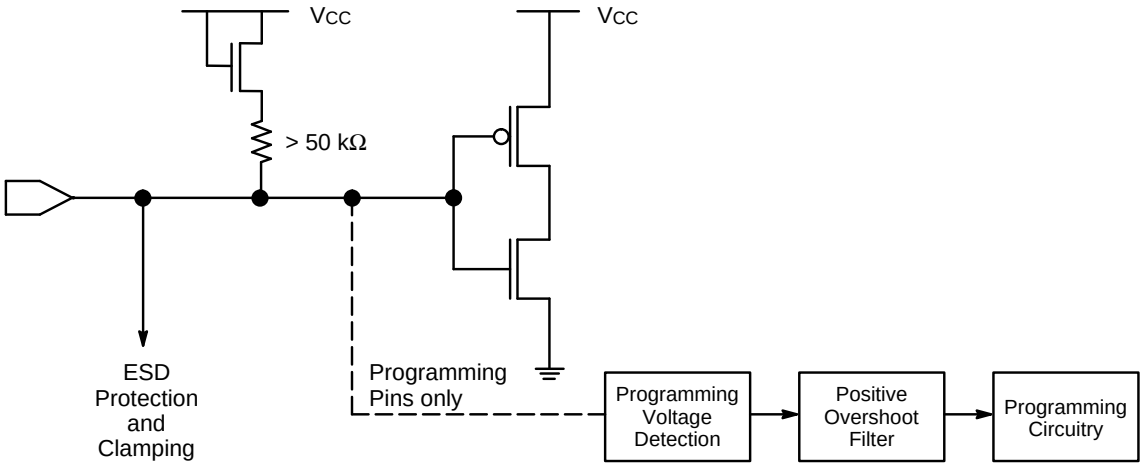
Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

ROBUSTNESS FEATURES

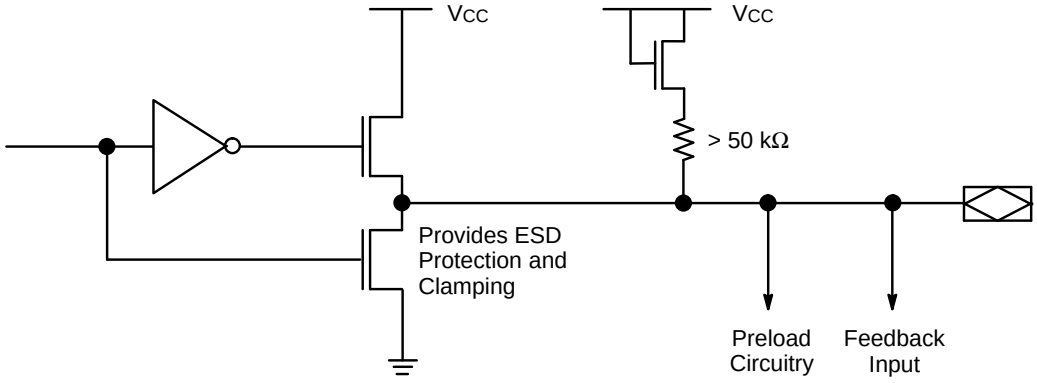
The PALCE20V8X-X/5 have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 versions.

Selected /4 devices are also being retrofitted with these robustness features. See the chart below for device listings.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR SELECTED /5 VERSION AND SELECTED /4 VERSIONS*



Typical Input



Typical Output

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*

Device	Rev Letter
PALCE20V8H-10	K
PALCE20V8H-15	K, J
PALCE20V8Q-15	J
PALCE20V8H-25	J
PALCE20V8Q-25	J

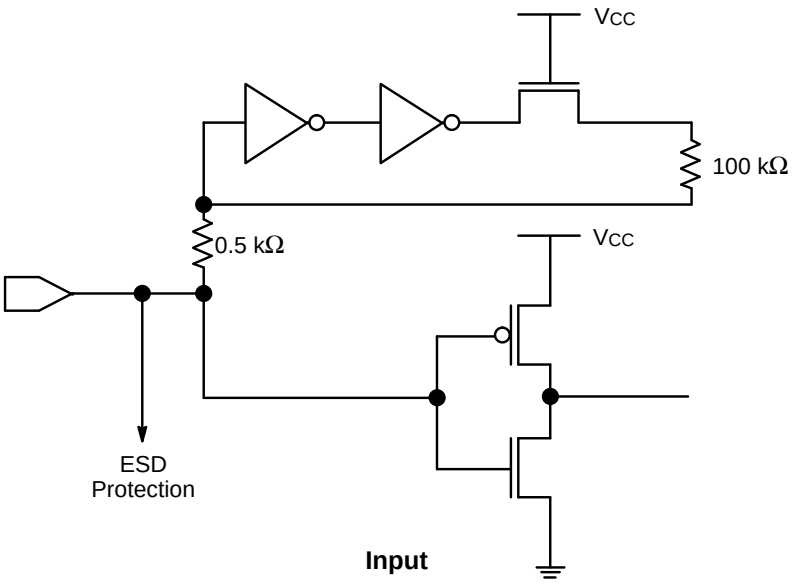
Topside Marking:

AMD CMOS PLDs are marked on top of the package in the following manner:

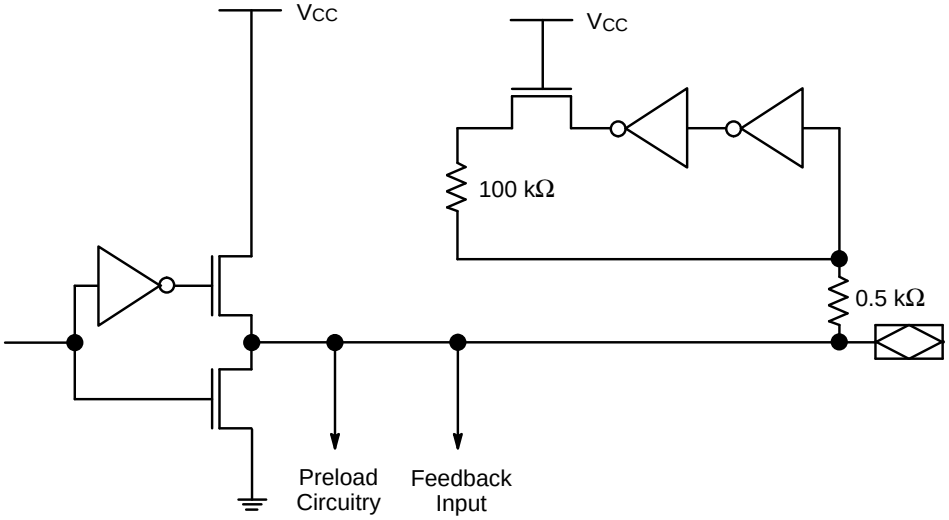
PALCEXXXX
Datecode (3 numbers) Lot ID (4 characters)– –(Rev Letter)

The Lot ID and Rev Letter are separated by two spaces.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR SELECTED /5 VERSIONS*



Input



I/O

16491D-15

*

Device	Rev Letter
PALCE20V8H-10	L
PALCE20V8H-15	L, M
PALCE20V8Q-15	M
PALCE20V8H-25	M
PALCE20V8Q-25	M

Topside Marking:

AMD CMOS PLDs are marked on top of the package in the following manner:

PALCEXXX
Datecode (3 numbers) Lot ID (4 characters)– –(Rev Letter)

The Lot ID and Rev Letter are separated by two spaces.

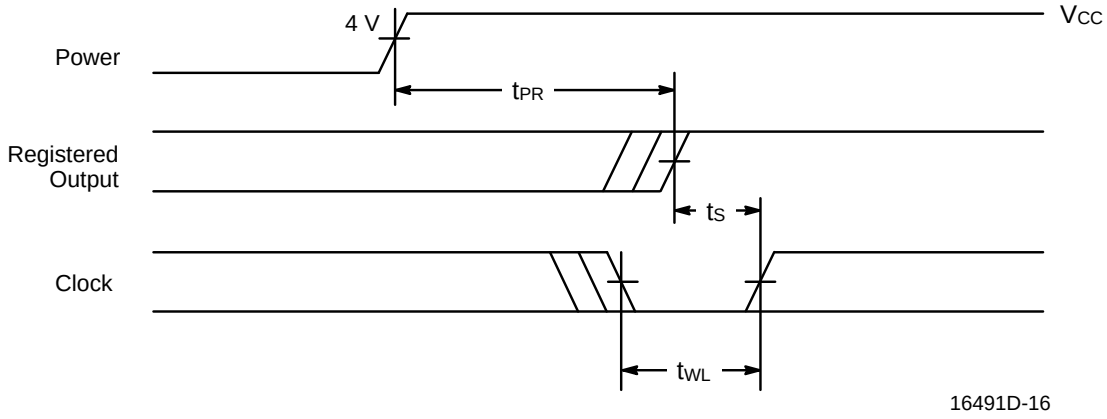
POWER-UP RESET

The PALCE20V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below.

Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min	Max	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveforms

TYPICAL THERMAL CHARACTERISTICS

/4 Devices (PALCE20V8H-10/4)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		19	19	°C/W
θ_{ja}	Thermal impedance, junction to ambient		73	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	61	45	°C/W
		400 lfpm air	53	41	°C/W
		600 lfpm air	50	38	°C/W
		800 lfpm air	47	36	°C/W

/5 Devices (PALCE20V8H-7/5)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		18	16	°C/W
θ_{ja}	Thermal impedance, junction to ambient		69	51	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	60	42	°C/W
		400 lfpm air	54	37	°C/W
		600 lfpm air	50	36	°C/W
		800 lfpm air	X	X	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

PALCE22V10Z Family

Zero-Power 24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero-power CMOS technology**
  - 30 μA standby current
  - As fast as 15 ns first-access propagation delay and 50 MHz f_{MAX} (external)
- **Unused product term disable for reduced power consumption**
- **Available in Industrial operating range at 15 ns t_{PD}**
  - T_A = –40°C to +85°C
  - V_{CC} = +4.5 V to +5.5 V
- **HC- and HCT-compatible inputs and outputs**
- **Electrically-erasable technology provides reconfigurable logic and full testability**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP, 28-pin PLCC, and 24-pin SOIC packages save space**

GENERAL DESCRIPTION

The PALCE22V10Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It provides user-programmable logic for replacing conventional zero-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

The PALCE22V10Z provides zero standby power and high speed. At 30 μA maximum standby current, the PALCE22V10Z allows battery powered operation for an extended period.

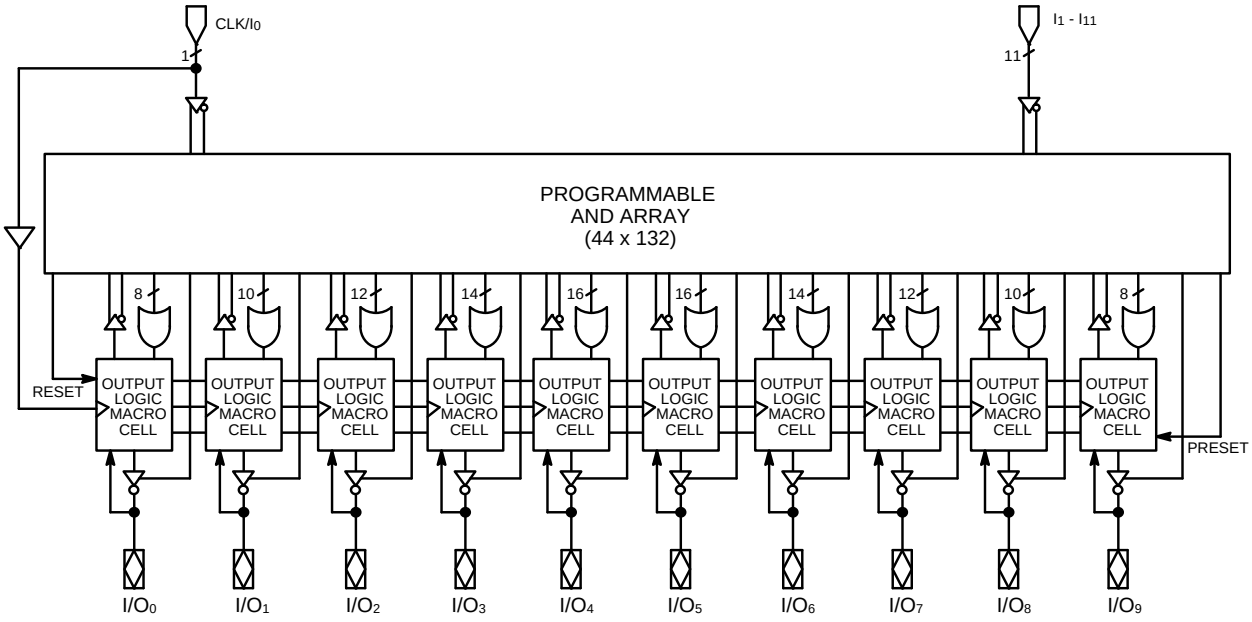
The ZPAL™ device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the Software Reference Guide to PLD Compliers for certified development systems, and the Programmer Reference Guide for approved programmers.

Publication# **15700** Rev. **E** Amendment **/0**
Issue Date: **February 1996**

BLOCK DIAGRAM

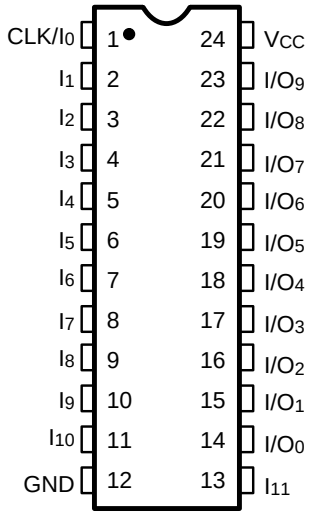


15700E-1

CONNECTION DIAGRAMS

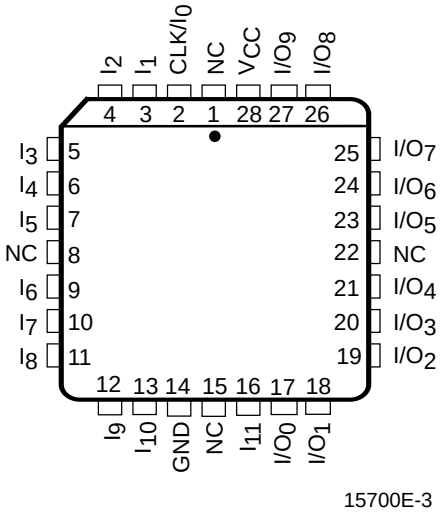
Top View

SKINNYDIP/SOIC



15700E-2

PLCC



15700E-3

Note:

Pin 1 is marked for orientation.

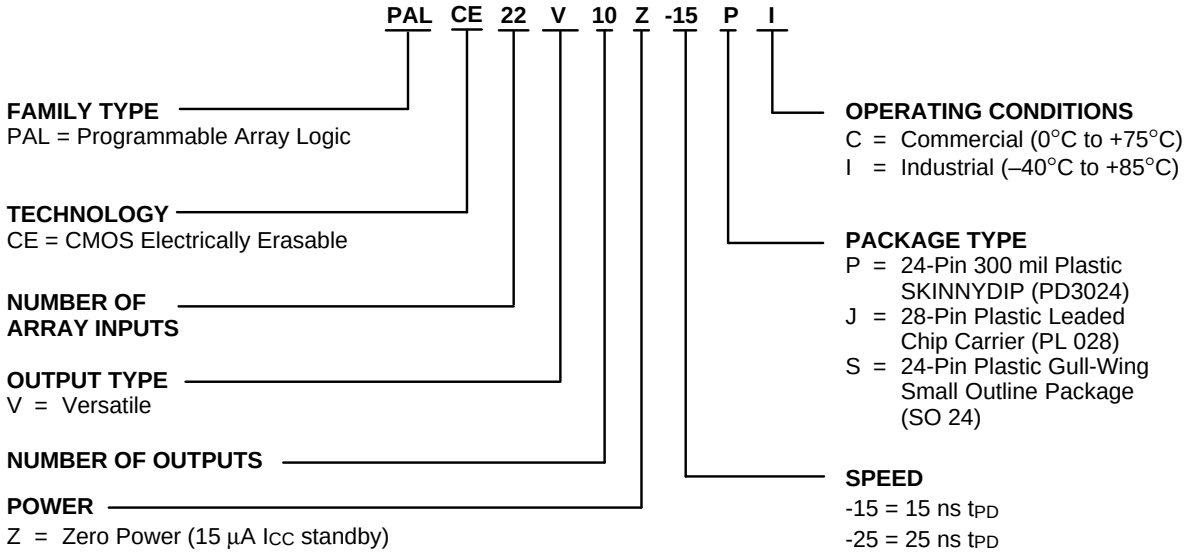
PIN DESCRIPTION

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
PALCE22V10Z-15	PI, JI
PALCE22V10Z-25	PC, JC, SC, PI, JI, SI

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE22V10Z is the zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALCE22V10Z has zero standby power and unused product term disable.

The PALCE22V10Z allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10Z has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

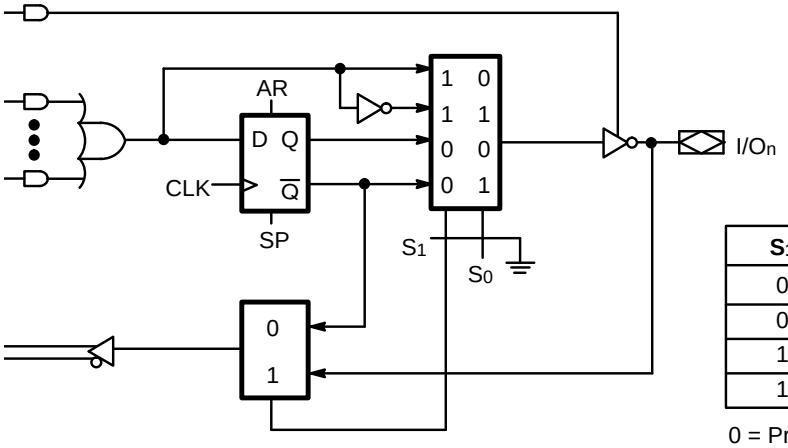
The PALCE22V10Z has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PALCE22V10Z includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

15700E-4

Figure 1. Output Logic Macrocell

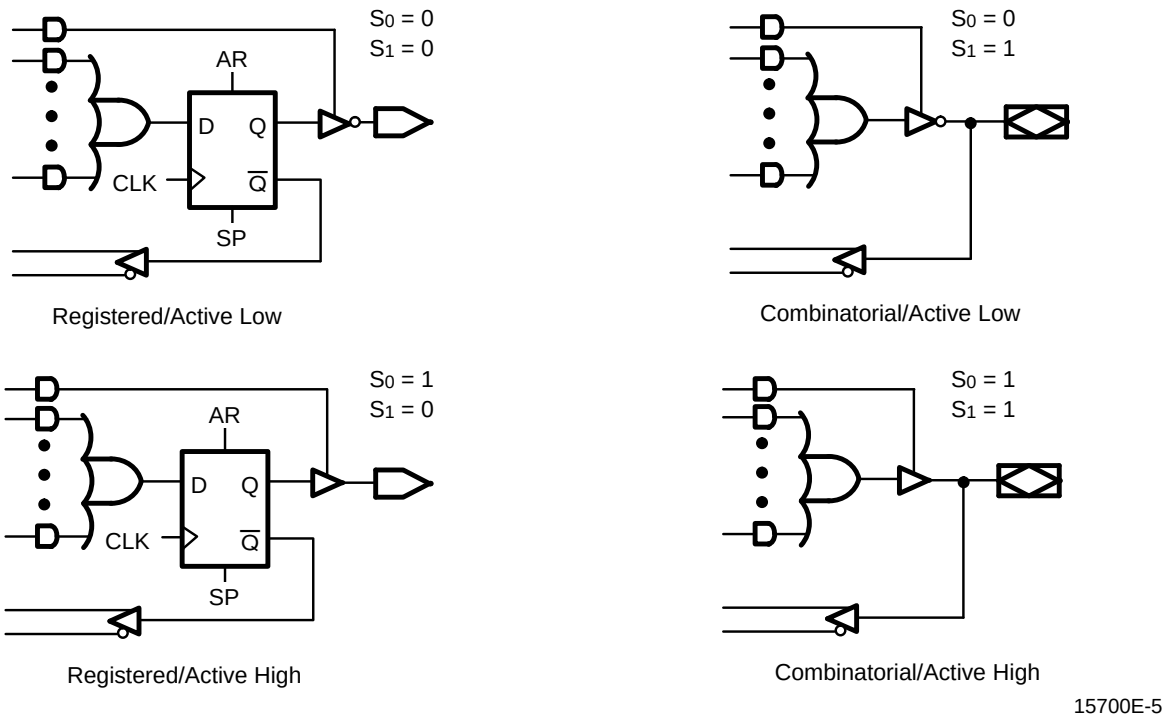


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10Z has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Zero-Standby Power Mode

The PALCE22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE22V10Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero (I_{CC} < 30 μA). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the I_{CC} vs. frequency graph.

Product-Term Disable

On a programmed PALCE22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs. frequency graph, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note “Minimizing Power Consumption with Zero-Power PLDs.”

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10Z will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The registers on the PALCE22V10Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10Z design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

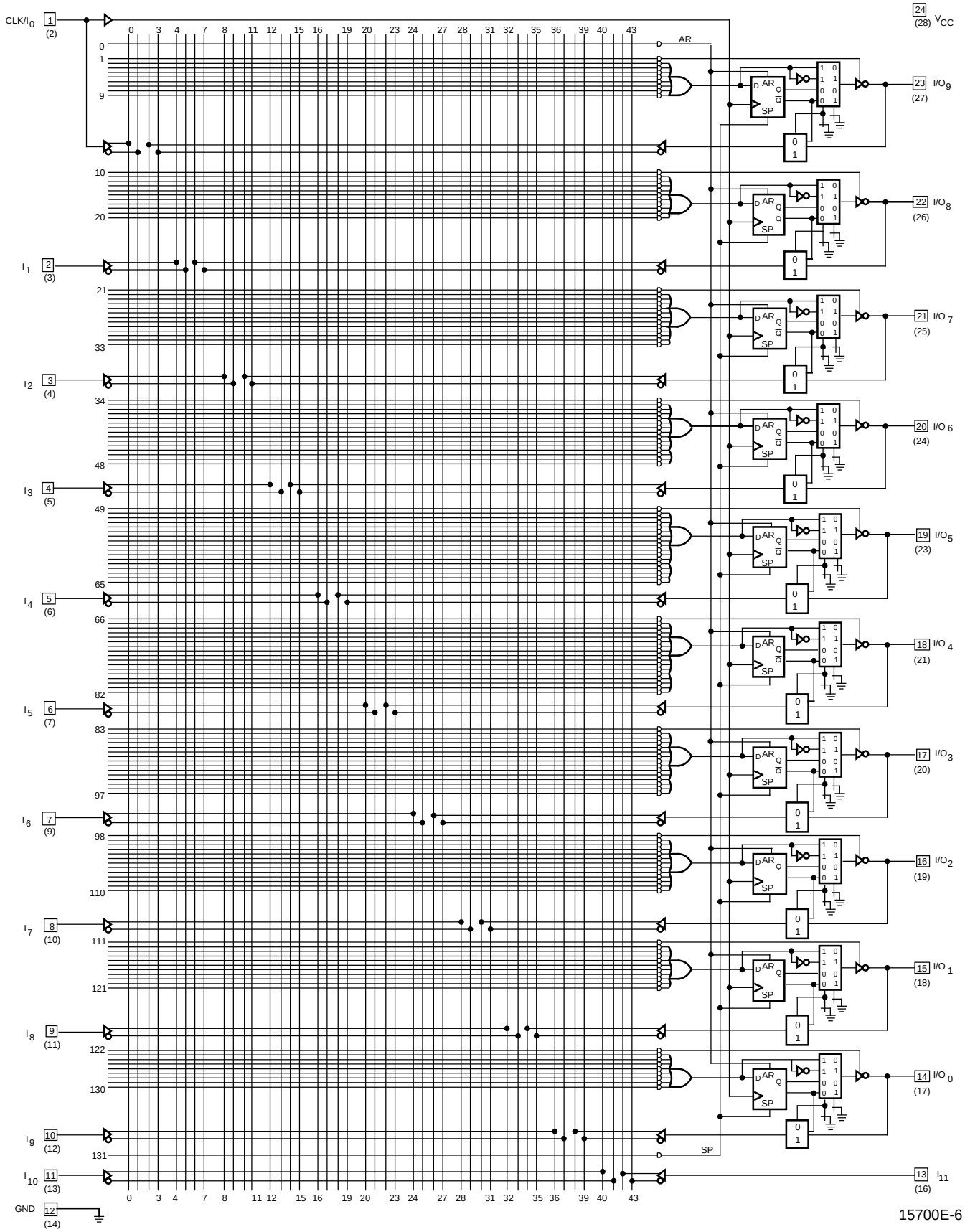
The PALCE22V10Z offers a very high level of built-in quality.

The erasability of the CMOS PALCE22V10Z allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALCE22V10Z is fabricated with AMD’s advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts



15700E-6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_C = –40°C to +85°C) . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case Temperature (T_C) . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min	I_{OH} = 20 µA	V_{CC}–0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
		V_{CC} = Min	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–5	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		30	µA
		V_{CC} = Max	f = 15 MHz		100	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width			15		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		ns
t_{SPR}	Synchronous Preset Recovery Time			10		ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_C = –40°C to +85°C) . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Operating Case Temperature (T_C) . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min	I_{OH} = 20 µA	V_{CC}– 0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
		V_{CC} = Min	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–5	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		30	µA
		V_{CC} = Max	f = 15 MHz		120	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *Represents the worst case of HC and HCT standards, allowing compatibility with either.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

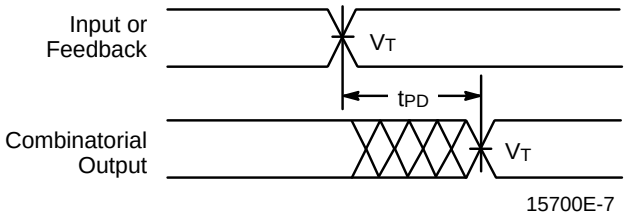
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Notes 4 and 5)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

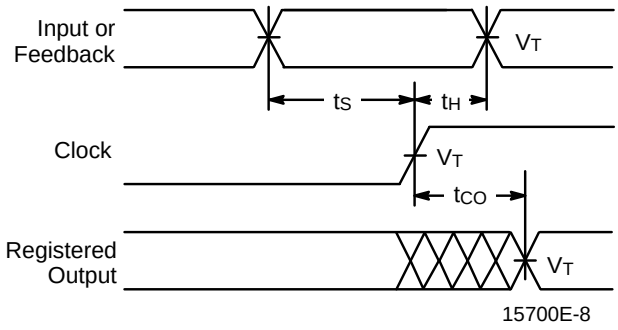
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 5 ns faster.*
4. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

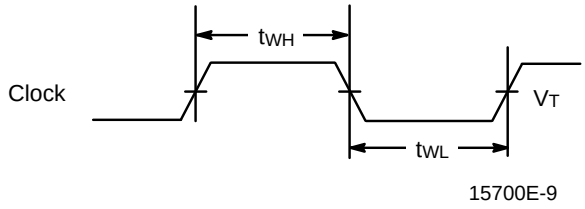
SWITCHING WAVEFORMS



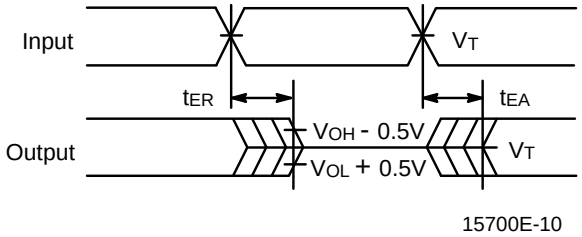
Combinatorial Output



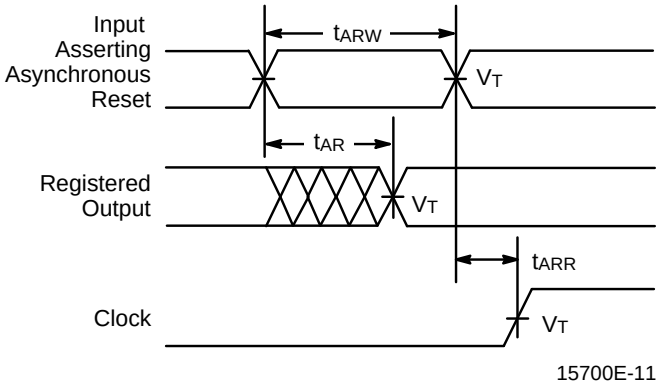
Registered Output



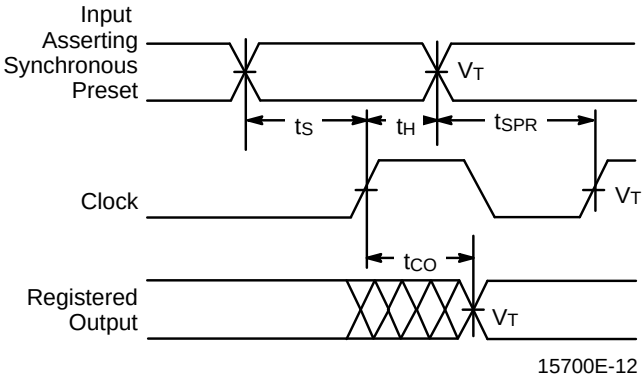
Clock Width



Input to Output Disable/Enable



Asynchronous Reset

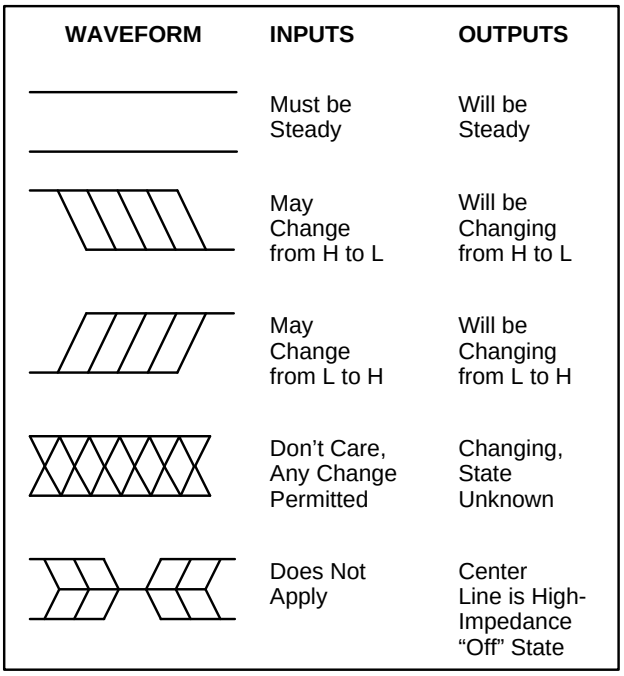


Synchronous Preset

Notes:

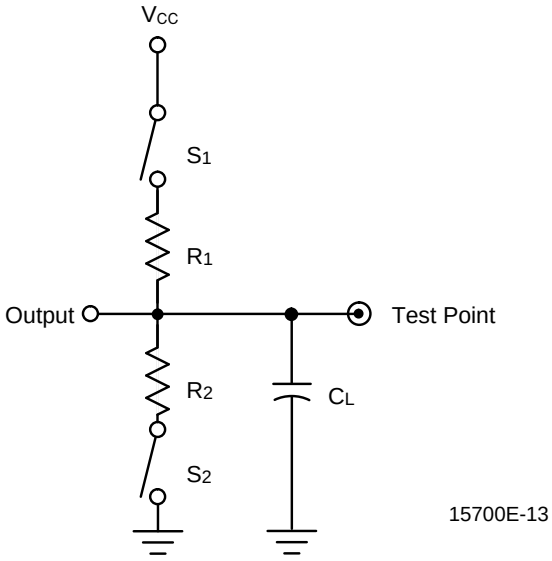
1. *V_T = 1.5 V for input signals and V_{CC}/2 for output signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–5 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

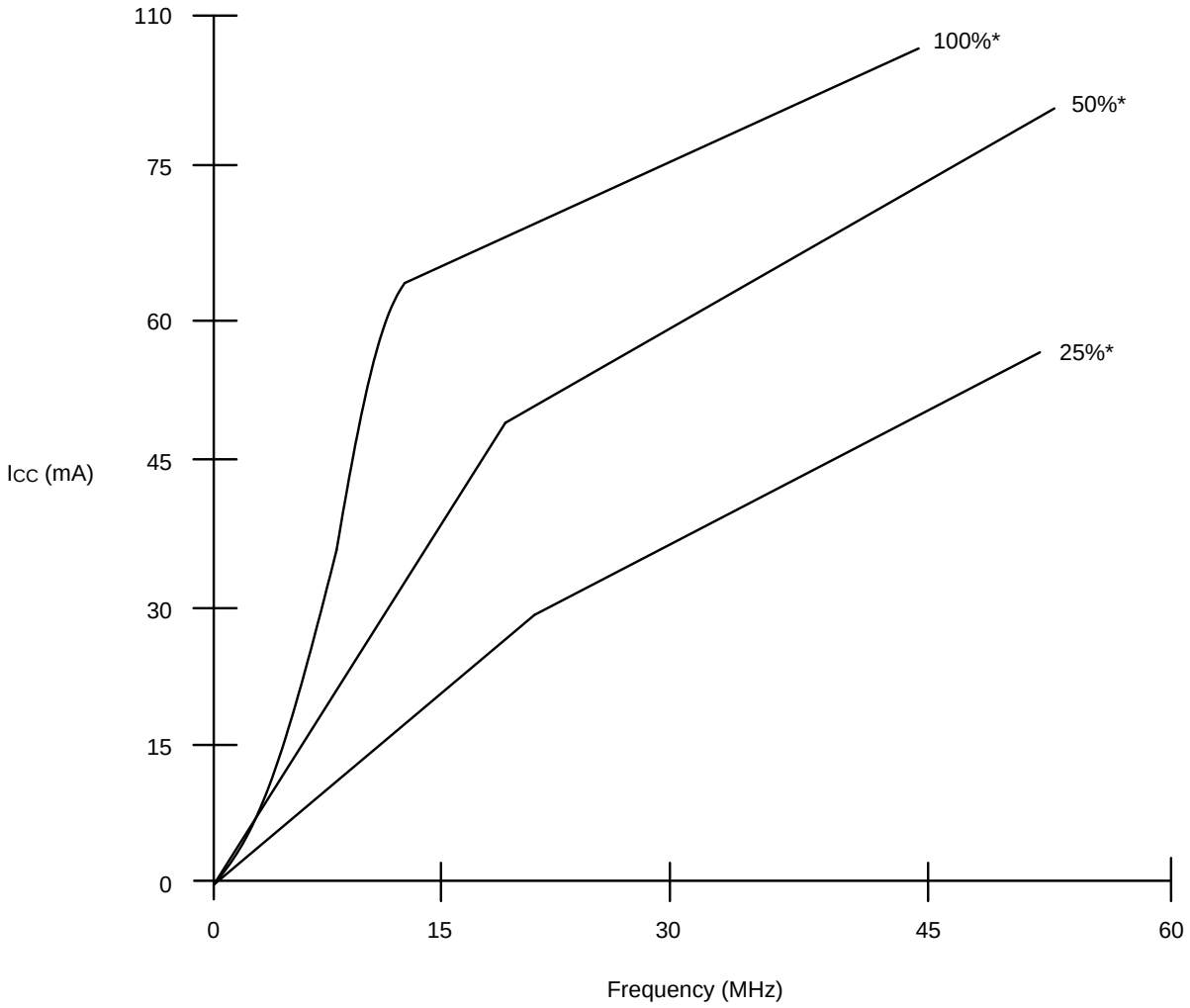
SWITCHING TEST CIRCUIT



15700E-13

Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	820 Ω	820 Ω	$V_{CC}/2$
t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				$V_{CC}/2$
t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE22V10Z-15
V_{CC} = 5.0 V, T_A = 25°C

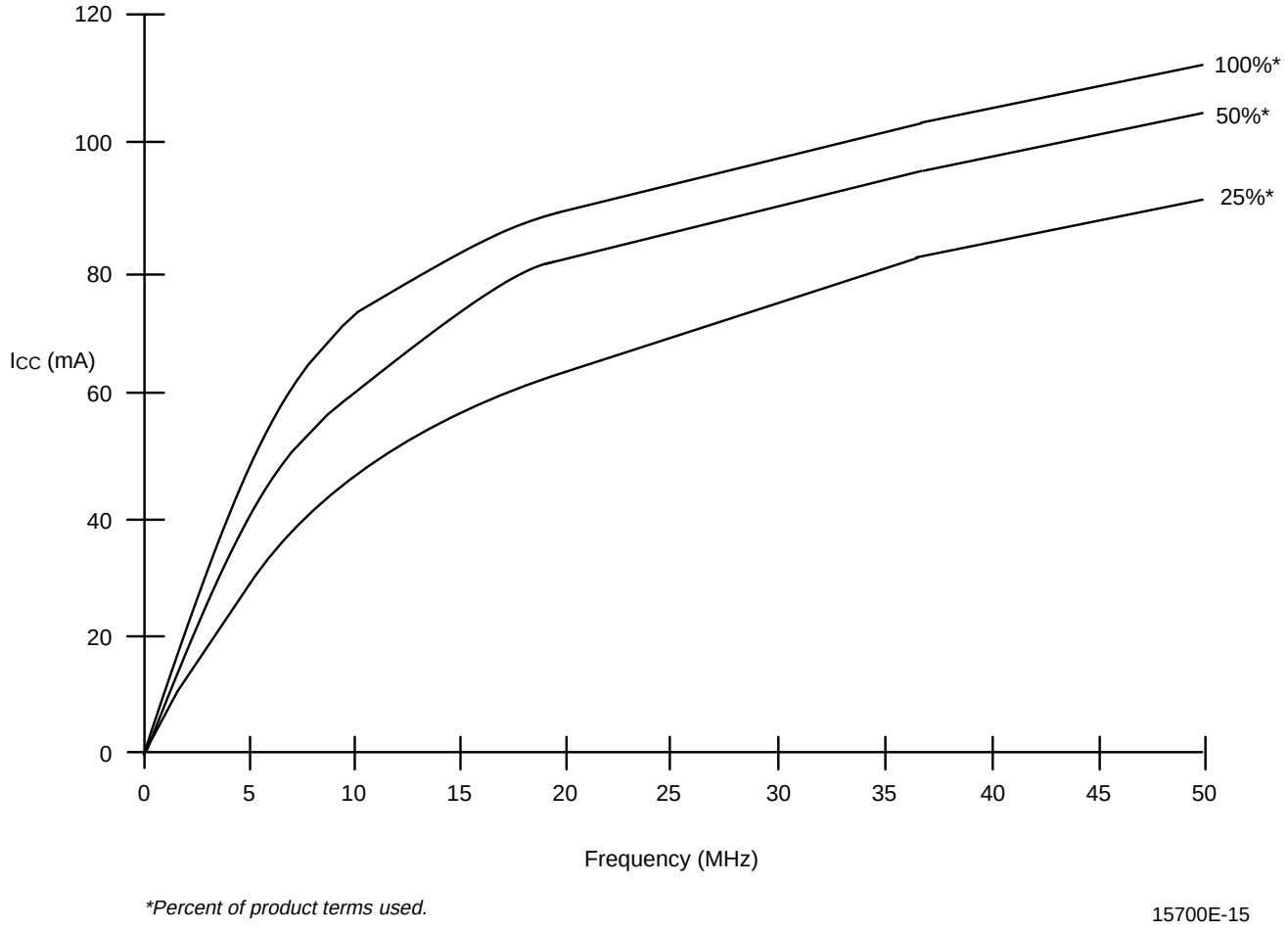


**Percent of product terms used.*

15700E-14

I_{CC} vs. Frequency
Graph for the PALCE22V10Z-15

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE22V10Z-25
V_{CC} = 5.0 V, T_A = 25°C



**Percent of product terms used.*

15700E-15

I_{CC} vs. Frequency Graph for the PALCE22V10Z-25

ENDURANCE CHARACTERISTICS

The PALCE22V10Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

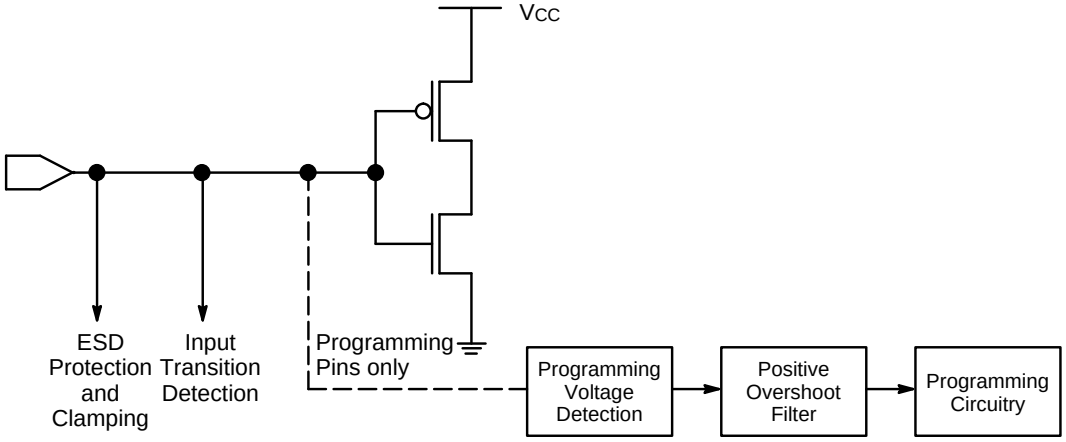
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

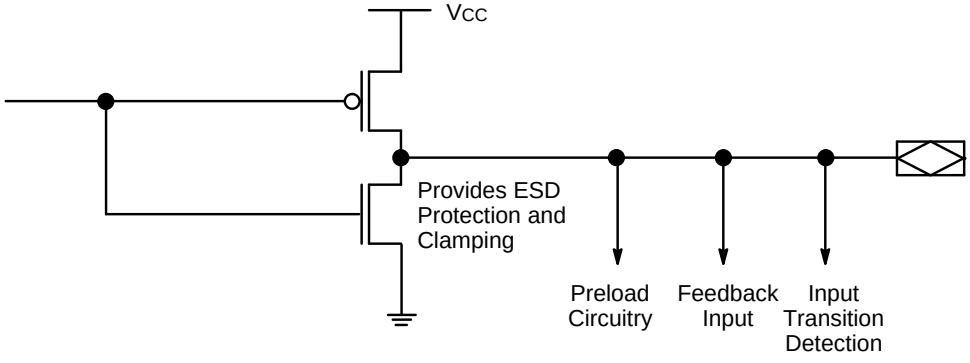
ROBUSTNESS FEATURES

The PALCE22V10Z has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

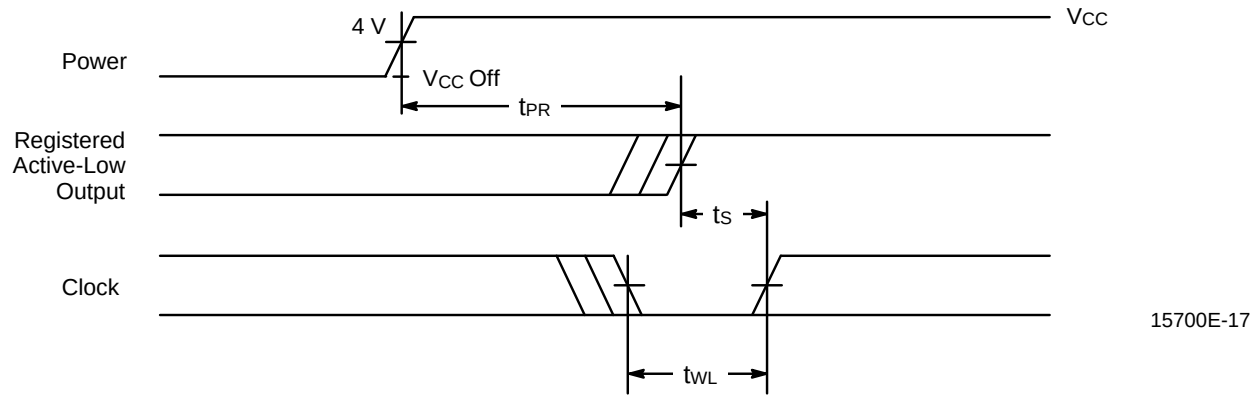
15700E-16

POWER-UP RESET FOR THE PALCE22V10Z FAMILY

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, four conditions are required to ensure a valid power-up reset. These conditions are:

- The supply voltage prior to the V_{CC} rise must not exceed V_{CC} off.
- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.
- If inputs are not switching at the time of power-up, an input transition must take place to assure proper data is set-up in registers or to outputs.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		
V_{CC} Off	Supply Voltage Prior to Power-Up	100	mV



Power-Up Reset Waveform

PALCE26V12 Family

28-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **28-pin versatile PAL programmable logic device architecture**
- **Electrically erasable CMOS technology provides half power (only 115 mA) at high speed (7.5 ns propagation delay)**
- **14 dedicated inputs and 12 input/output macrocells for architectural flexibility**
- **Macrocells can be registered or combinatorial, and active high or active low**
- **Varied product term distribution allows up to 16 product terms per output**
- **Two clock inputs for independent functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Register preload for testability and built-in register reset on power-up**
- **Space-efficient 28-pin SKINNYDIP and PLCC packages**
- **Center V_{CC} and GND pins to improve signal characteristics**
- **Extensive third-party software and programmer support through FusionPLD partners**

GENERAL DESCRIPTION

The PALCE26V12 is a 28-pin version of the popular PAL22V10 architecture. Built with low-power, high-speed, electrically-erasable CMOS technology, the PALCE26V12 offers many unique advantages.

Device logic is automatically configured according to the user's design specification. Design is simplified by design software, allowing automatic creation of a programming file based on Boolean or state equations. The software can also be used to verify the design and can provide test vectors for the programmed device.

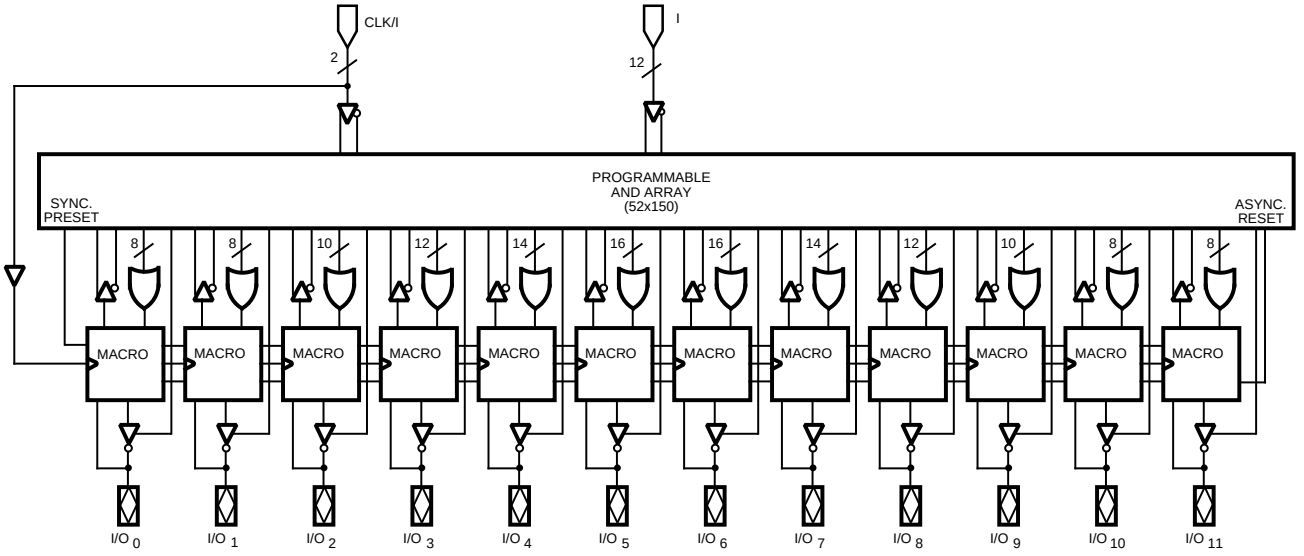
The PALCE26V12 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The functions are programmed into the device through electrically-erasable floating-gate cells in the AND logic array and the macrocells. In the unprogrammed state, all AND product terms float HIGH. If both true and complement of any input are connected, the term will be permanently LOW.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, active high or active low, with registered I/O possible. The flip-flop can be clocked by one of two clock inputs. The output configuration is determined by four bits controlling three multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE26V12 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# **16072** Rev. **E** Amendment **/0**
Issue Date: **February 1996**

BLOCK DIAGRAM

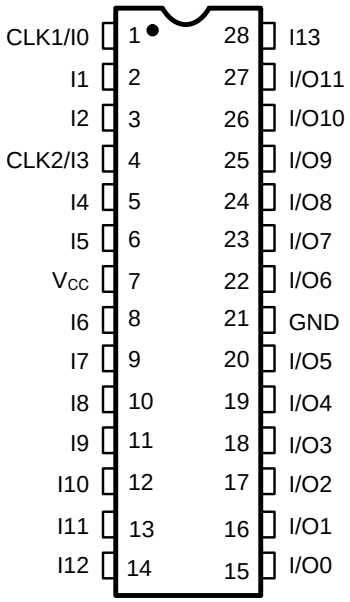


16072E-1

CONNECTION DIAGRAMS

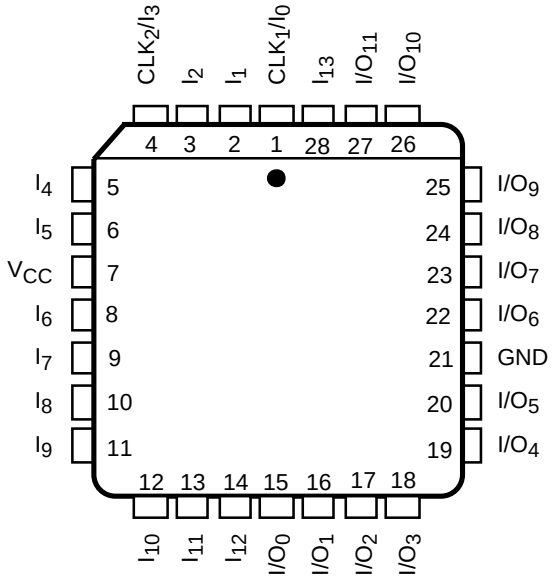
Top View

DIP



16072E-2

PLCC



16072E-3

Note:
Pin 1 is marked for orientation.

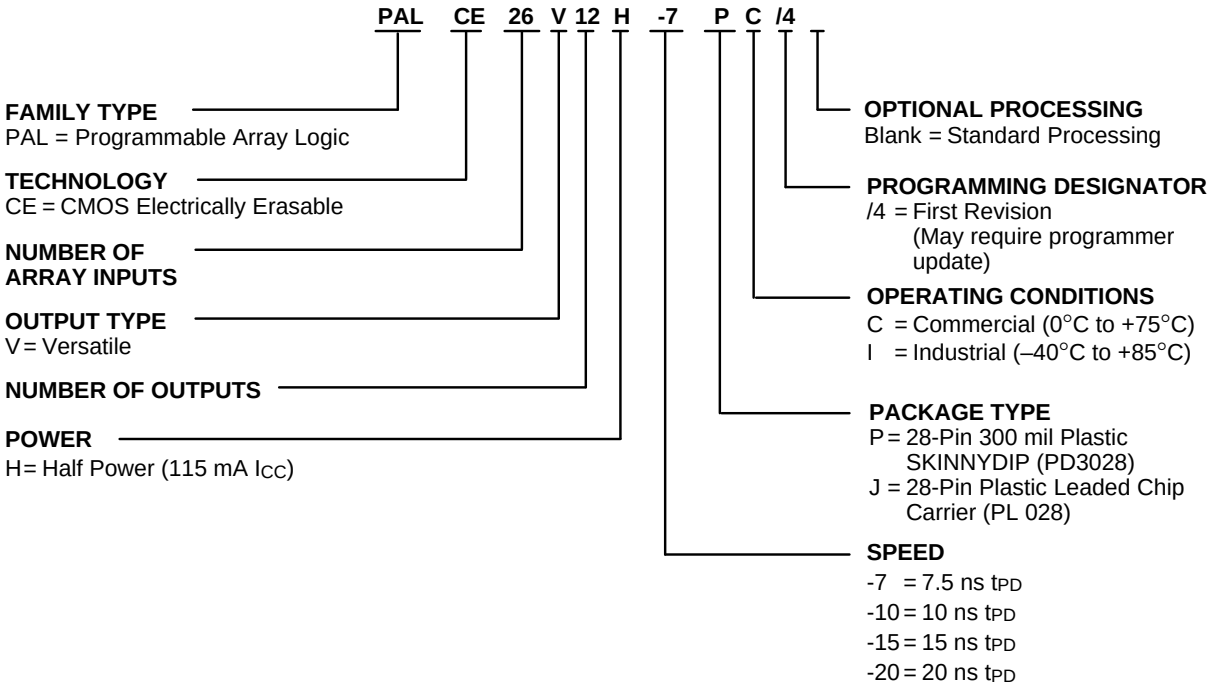
PIN DESCRIPTION

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
V_{CC}	=	Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD commercial and industrial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE26V12H-7	JC	/4
PALCE26V12H-10	PC, JC, PI, JI	
PALCE26V12H-15		
PALCE26V12H-20		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE26V12 has fourteen dedicated input lines, two of which can be used as clock inputs. Unused inputs should be tied directly to ground or V_{CC}. Buffers for device inputs and feedbacks have both true and complementary outputs to provide user-selectable signal polarity. The inputs drive a programmable AND logic array, which feeds a fixed OR logic array.

The OR gates feed the twelve I/O macrocells (see Figure 1). The macrocell allows one of eight potential output configurations; registered or combinatorial, active high or active low, with register or I/O pin feedback (see Figure 2). In addition, registered configurations can be clocked by either of the two clock inputs.

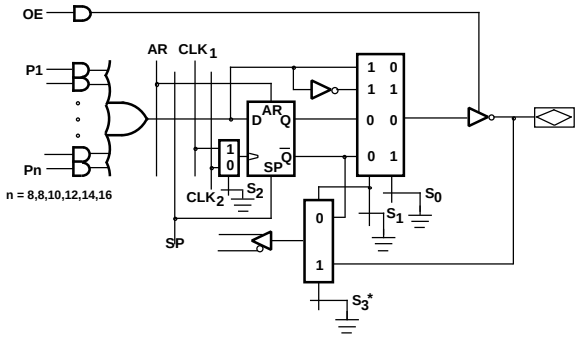
The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S0–S3 (see Table 1). Multiplexer controls initially float to V_{CC} (1) through a programmable cell, selecting the "1" path through the multiplexer. Programming the cell connects the control line to GND (0), selecting the "0" path.

Table 1. Macrocell Configuration Table

S3	S1	S0	Output Configuration
1	0	0	Registered Output and Feedback, Active Low
1	0	1	Registered Output and Feedback, Active High
1	1	0	Combinatorial I/O, Active Low
1	1	1	Combinatorial I/O, Active High
0	0	0	Registered I/O, Active Low
0	0	1	Registered I/O, Active High
0	1	0	Combinatorial Output, Registered Feedback, Active Low
0	1	1	Combinatorial Output, Registered Feedback, Active High

1 = Unprogrammed EE bit
0 = Programmed EE bit

S2	Clock Input
1	CLK_1/I_0
0	CLK_2/I_3



**When S_3 = 1 (unprogrammed) the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.*

16072E-4

Figure 1. PALCE26V12 Macrocell

Registered or Combinatorial

Each macrocell of the PALCE26V12 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH edge of the selected clock input. Any macrocell can be configured as combinatorial by selecting a multiplexer path that bypasses the flip-flop. Bypass is controlled by bit S1.

Programmable Clock

The clock input for any flip-flop can be selected to be from either pin 1 or pin 4. A 2:1 multiplexer controlled by bit S2 determines the clock input.

Programmable Feedback

A 2:1 multiplexer allows the user to determine whether the macrocell feedback comes from the flip-flop or from the I/O pin, independent of whether the output is registered or combinatorial. Thus, registered outputs may have internal register feedback for higher speed (f_{MAX} internal), or I/O feedback for use of the pin as a direct input (f_{MAX} external). Combinatorial outputs may have I/O feedback, either for use of the signal in other equations or for use as another direct input, or register feedback.

The feedback multiplexer is controlled by the same bit (S1) that controls whether the output is registered or combinatorial, as on the 22V10, with an additional control bit (S3) that allows the alternative feedback path to be selected. When S3 = 1, S1 selects register feedback for registered outputs (S1 = 0) and I/O feedback for combinatorial outputs (S1 = 1). When S3 = 0, the opposite is selected: I/O feedback for registered outputs and register feedback for combinatorial outputs.

Programmable Enable and I/O

Each macrocell has a three-state output buffer controlled by an individual product term. Enable and disable can be a function of any combination of device inputs or feedback. The macrocell provides a bidirectional I/O pin if I/O feedback is selected, and may be configured as a dedicated input if the buffer is always disabled. This is accomplished by connecting all inputs to the enable term, forcing the AND of the complemented inputs to be always LOW. To permanently enable the outputs, all inputs are left disconnected from the term (the unprogrammed state).

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save “DeMorganizing” efforts.

Selection is controlled by programmable bit S0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high.

Preset/Reset

For initialization, the PALCE26V12 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH or the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE26V12 will be HIGH or LOW depending on whether the output is active low or active high, respectively. The V_{CC} rise must be monotonic, and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE26V12 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE26V12 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. Programming the security bit disables preload, and the array will read as if every bit is disconnected. The security bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

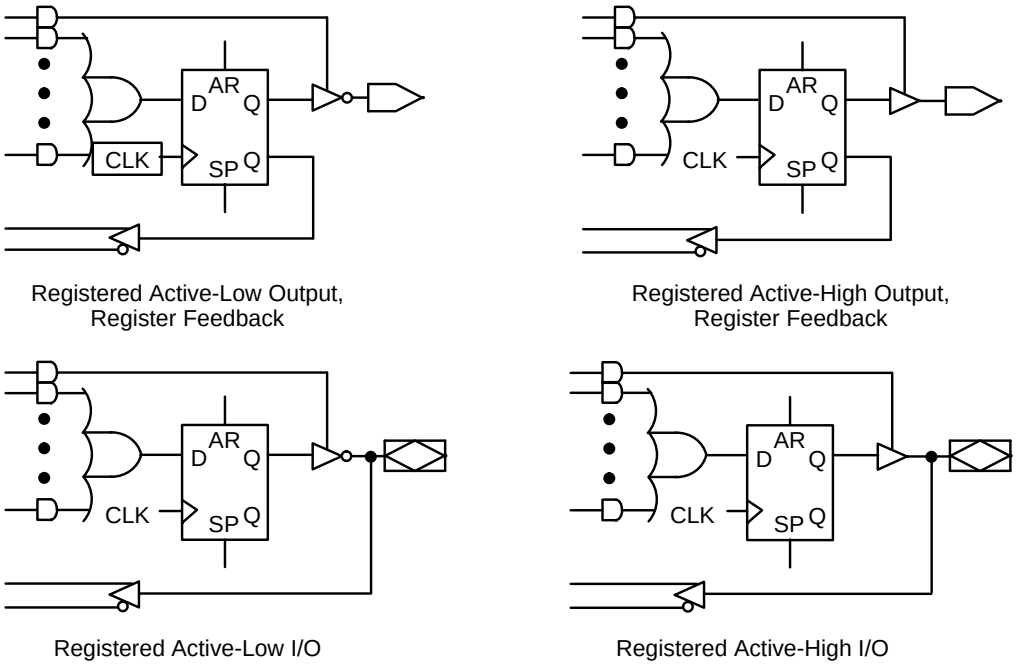
The PALCE26V12 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALCE26V12 offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE26V12 is fabricated with AMD’s advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.



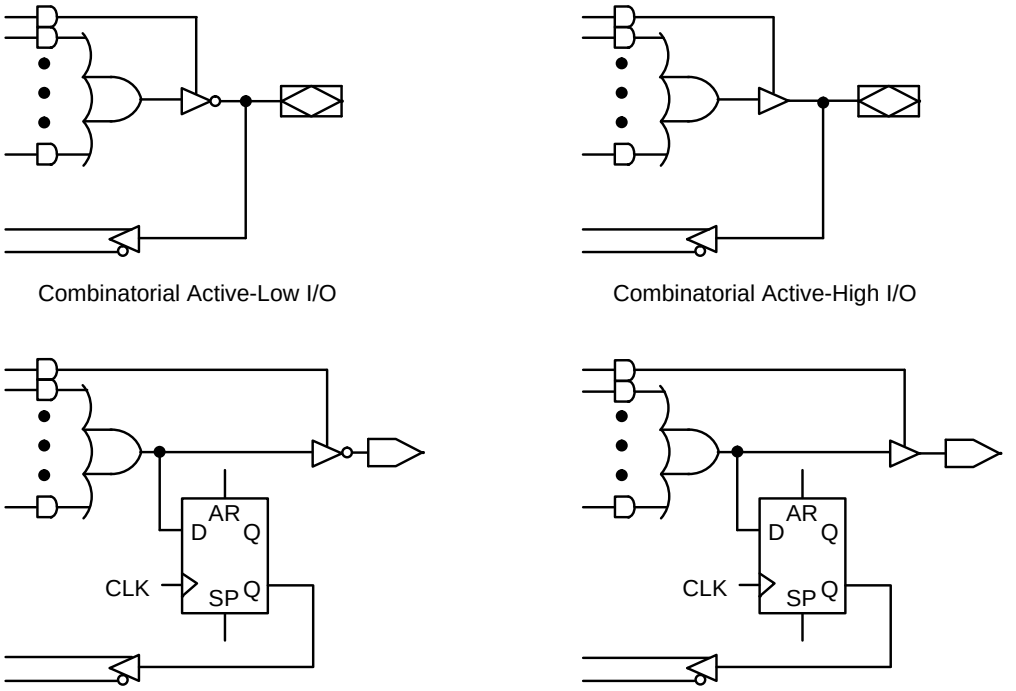
Registered Active-Low Output, Register Feedback

Registered Active-High Output, Register Feedback

Registered Active-Low I/O

Registered Active-High I/O

Registered Outputs



Combinatorial Active-Low I/O

Combinatorial Active-High I/O

Combinatorial Active-Low Output, Register Feedback

Combinatorial Active-High Output, Register Feedback

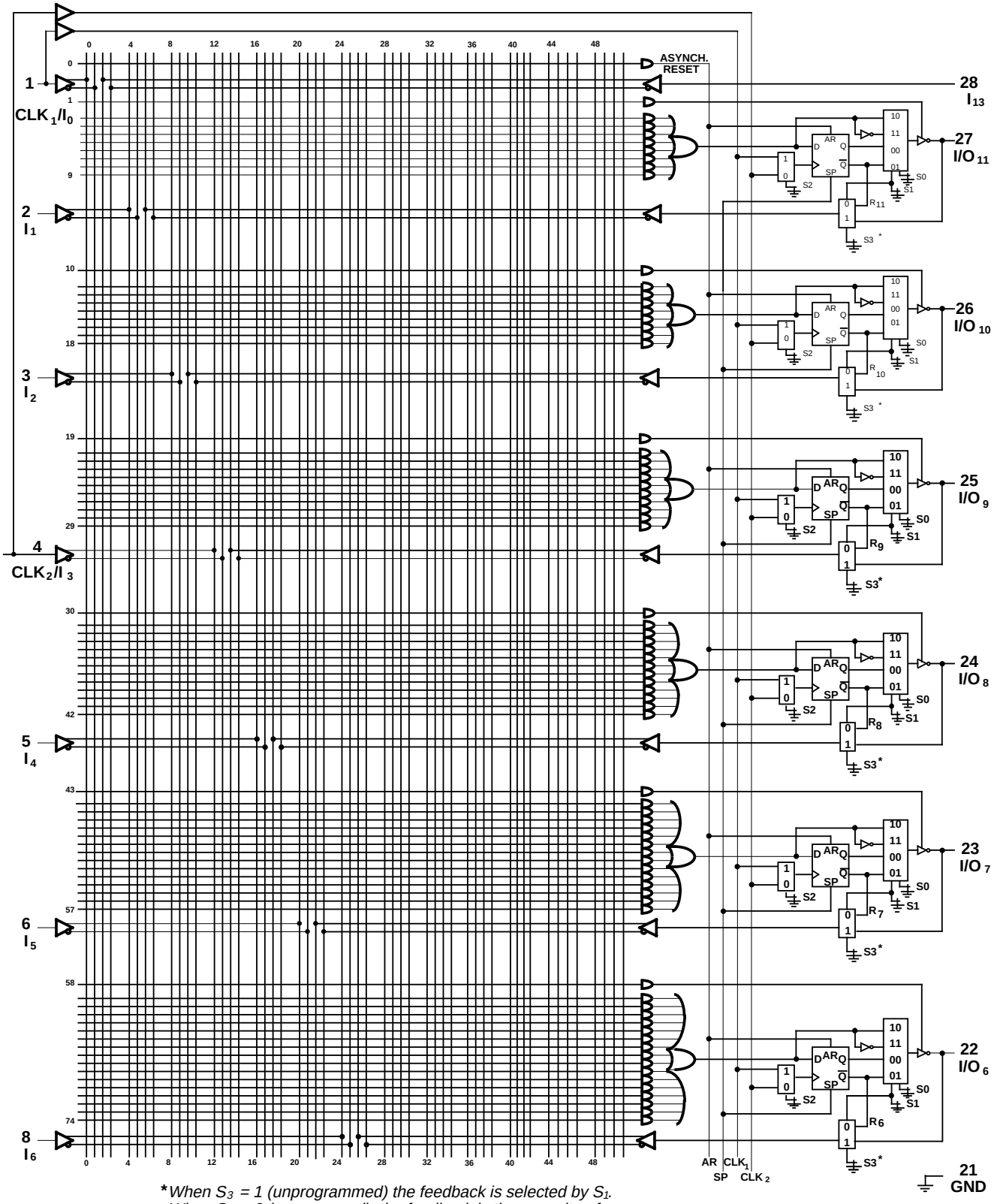
Combinatorial Outputs

16072E-5

Figure 2. PALCE26V12 Macrocell Configuration Options

LOGIC DIAGRAM

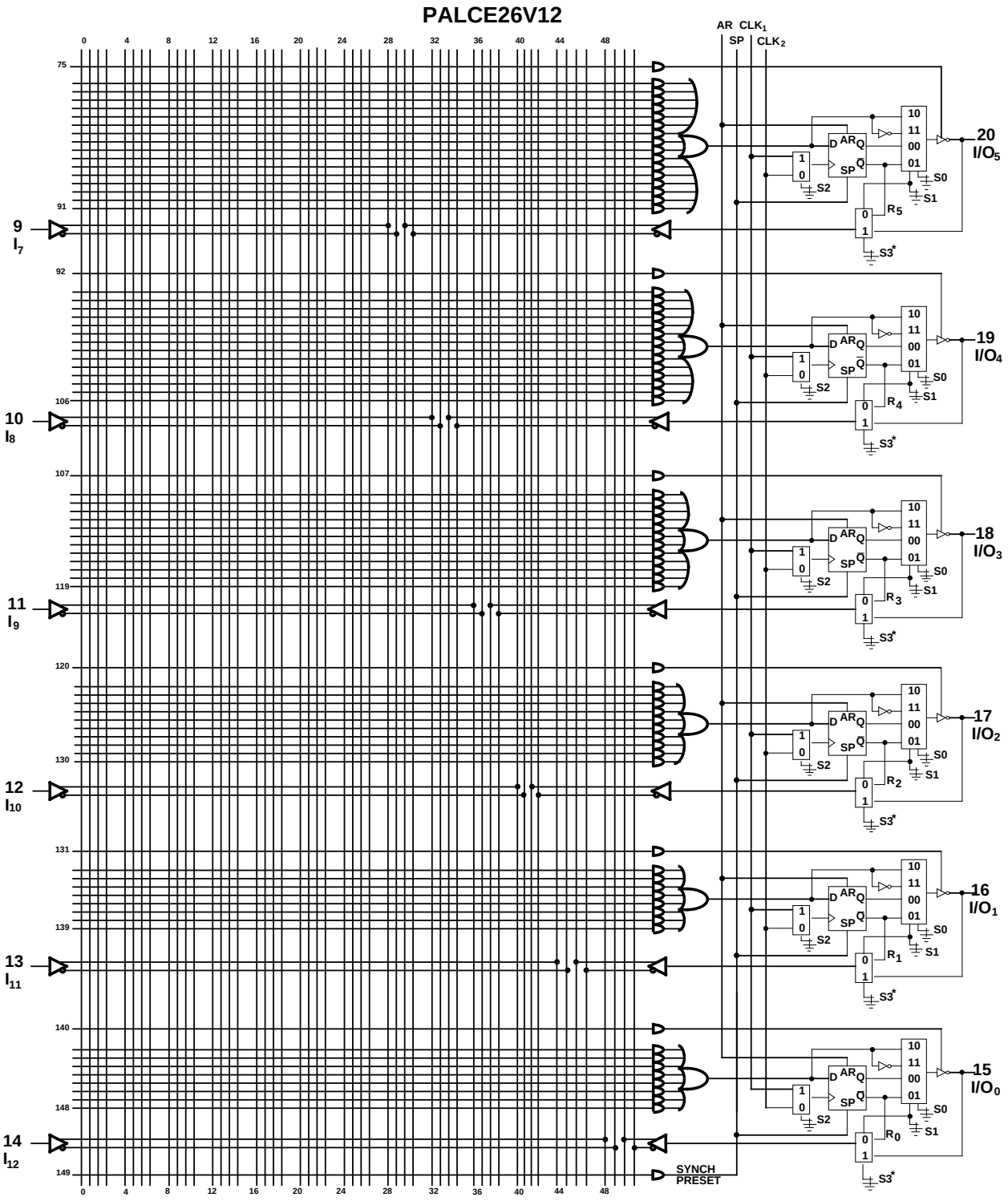
PALCE26V12



***** *When S_3 = 1 (unprogrammed) the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.*

16072E-6

LOGIC DIAGRAM (continued)



When S_3 = 1 (unprogrammed) the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

16072E-6
(concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.6 V to +7.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–170	mA
I_{CC} (Static)	Commercial Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 0 MHz	H-7/10		115	mA
I_{CC} (Dynamic)	Commercial Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz	H-7/10		140	mA
I_{CC} (Dynamic)	Industrial Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz	H-10		150	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V T_A = +25°C	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	f = 1 MHz	8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-7		-10		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				7.5		10	ns
t_{S1}	Setup Time from Input or Feedback			3.5		5		ns
t_{S2}	Setup Time from SP to Clock			4.5		5		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				6		9	ns
t_{AR}	Asynchronous Reset to Registered Output				11		13	ns
t_{ARW}	Asynchronous Reset Width			6		8		ns
t_{ARR}	Asynchronous Reset Recovery Time			5		8		ns
t_{SPR}	Synchronous Preset Recovery Time			5		8		ns
t_{WL}	Clock Width	LOW		3.5		4		ns
t_{WH}		HIGH		3.5		4		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S + t_{CO})$	105.3		71.4		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	125		105		MHz
t_{EA}	Input to Output Enable Using Product Term Control				8		10	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5		10	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.6 V to +7.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–160	mA
I_{CC} (Static)	Commerical Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 0 MHz	H-15/20		105	mA
I_{CC} (Dynamic)	Industrial Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz	H-15		150	mA
I_{CC} (Static)		V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	H-20		130	mA
I_{CC} (Dynamic)		V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz	H-20		150	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V T_A = +25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-20		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		20	ns
t_S	Setup Time from Input, Feedback, or SP to Clock			10		13		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time			15		20		ns
t_{SPR}	Synchronous Preset Recovery Time			10		13		ns
t_{WL}	Clock Width	LOW		8		10		ns
t_{WH}		HIGH		8		10		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S + t_{CO})$	50		40		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	58.8		43		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		20	ns

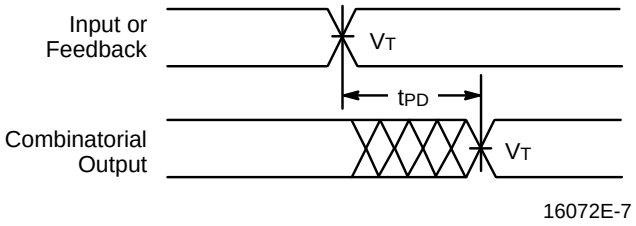
Notes:

2. See Switching Test Circuit for test conditions.

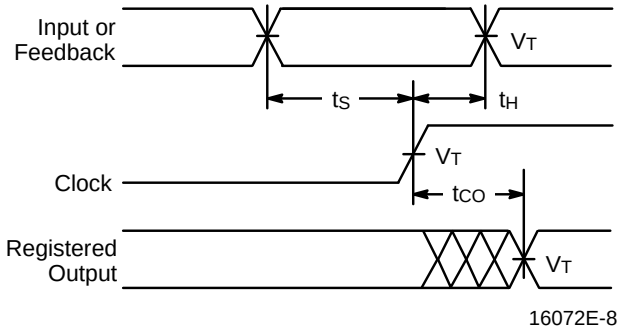
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

6. t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.

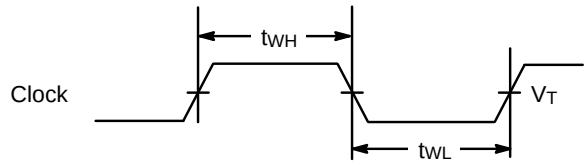
SWITCHING WAVEFORMS



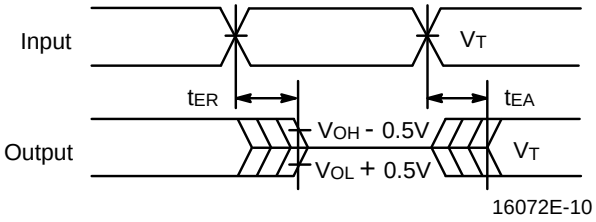
Combinatorial Output



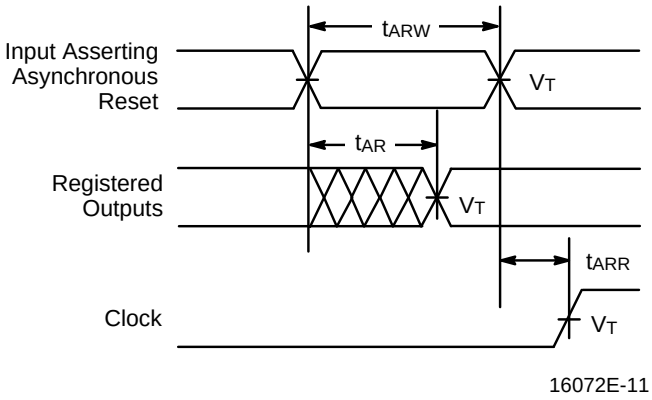
Registered Output



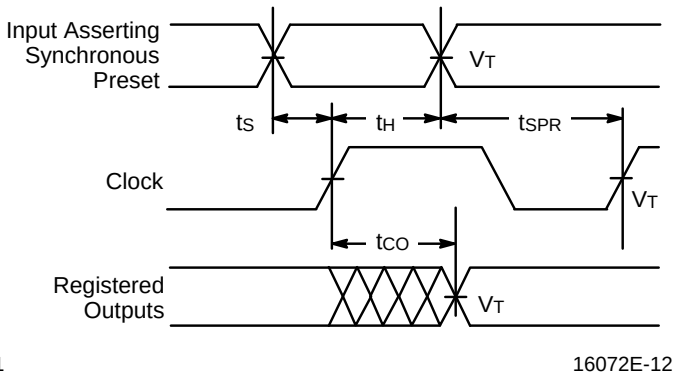
Clock Width



Input to Output Disable/Enable



Asynchronous Reset

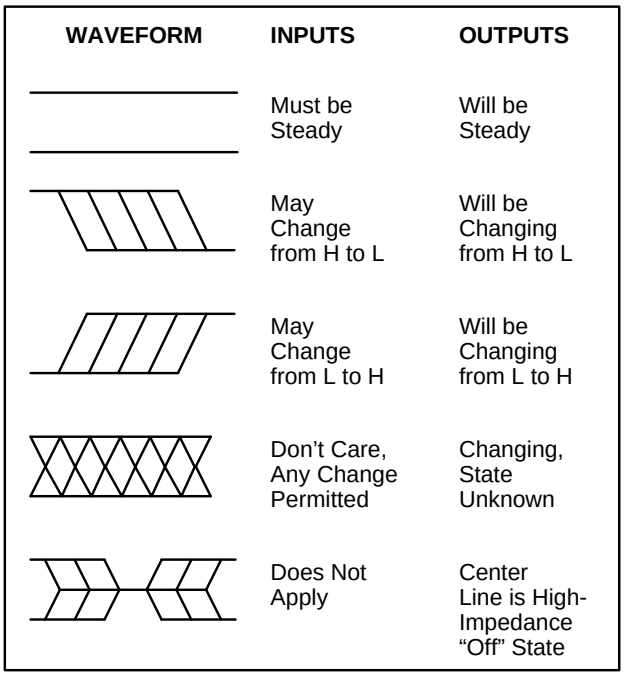


Synchronous Preset

Notes:

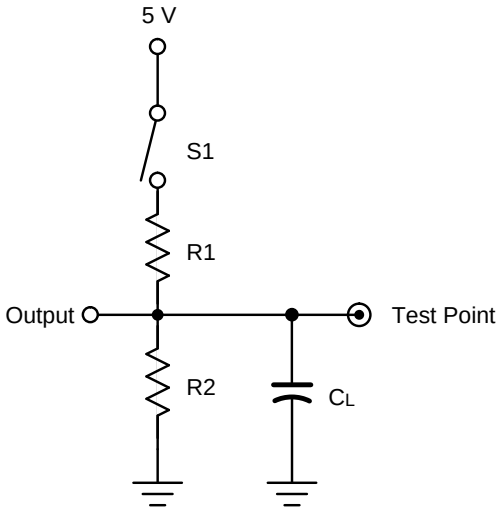
1. *V_T = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–5 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT

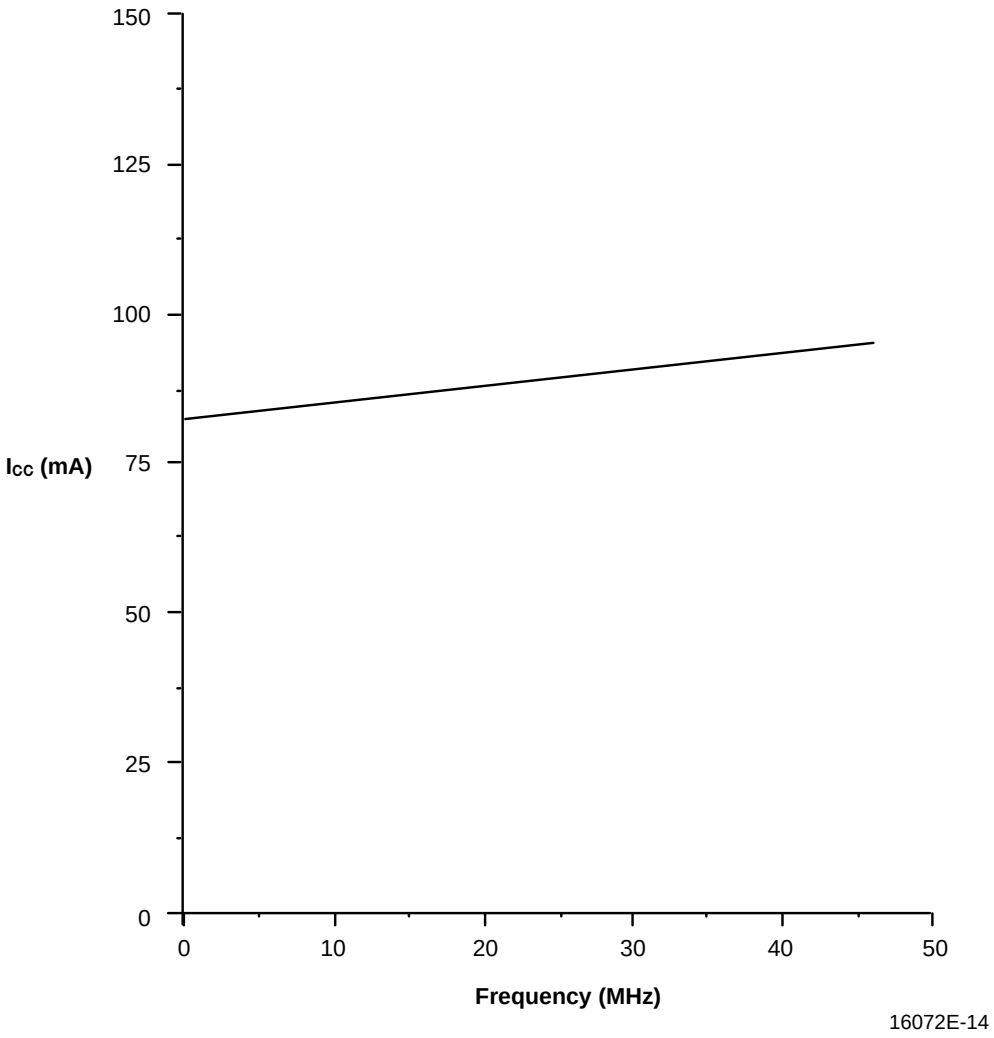


16072E-13

Specification	S1	C_L	R1	R2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	Com'l: H-15/20 Ind: H-20 390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF		Com'l: H-7/10 Ind: H-10/15 300 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS FOR THE PALCE26V12H-7/10

V_{CC} = 5.0 V, T_A = 25°C



The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

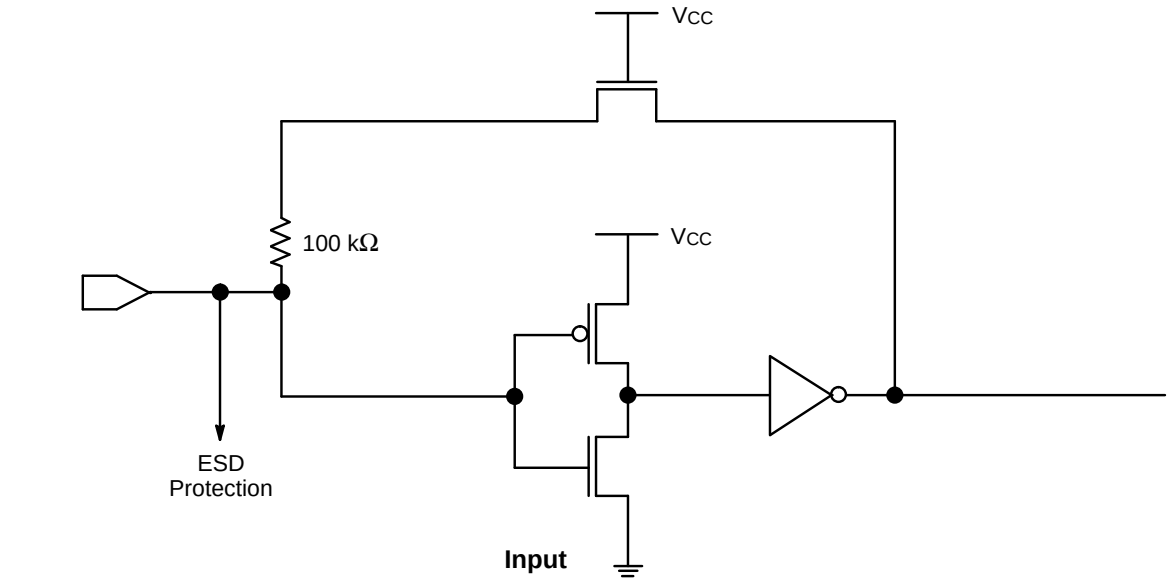
The PALCE26V12 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

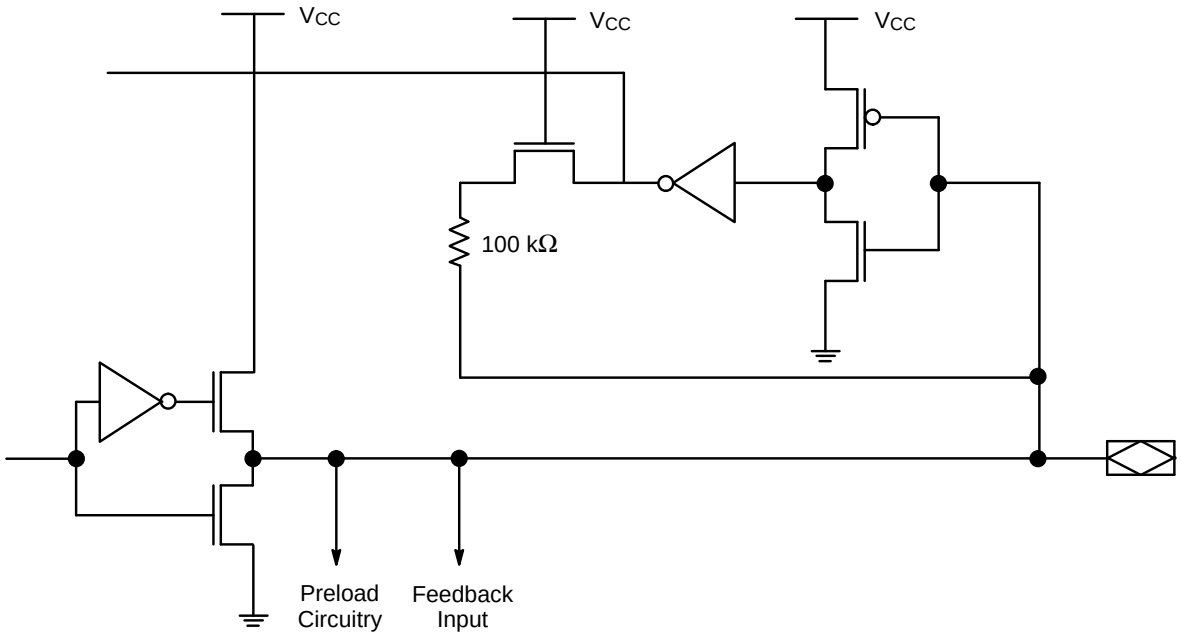
Bus-Friendly Inputs

The PALCE26V12H-7/10 (Com'l) and H-10/15 (Ind) inputs and I/O loop back to the input after the second stage of the input buffer. This configuration reinforces the state of the input and pulls the voltage away from the input threshold voltage where noise can cause oscillations. For an illustration of this configuration, see below.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR REV. C VERSION*



Input



16072E-15

Output

*

Device	Rev. Letter
PALCE26V12H-7	C
PALCE26V12H-10	
PALCE26V12H-15	

Topside Marking:

AMD CMOS PLD's are marked on top of the package in the following manner:

PALCE xxxx

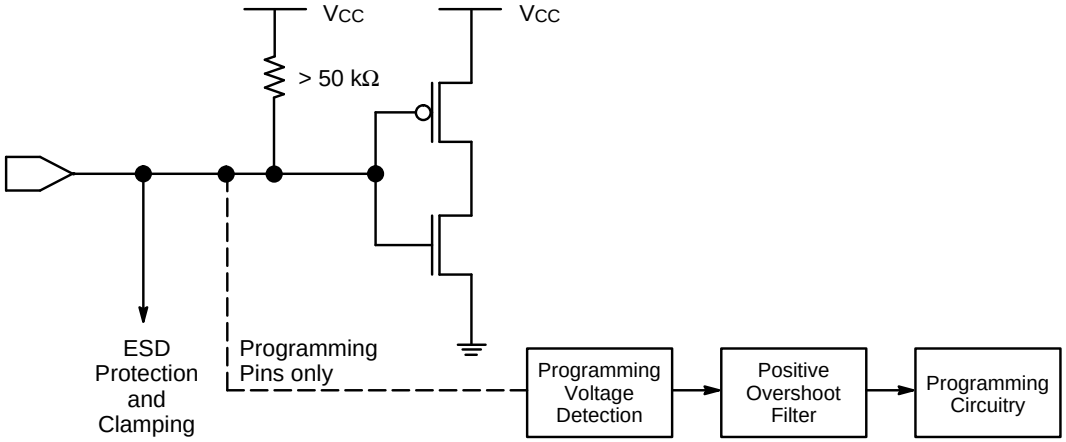
Datecode (4 numbers) LOT ID (3 characters) – – (Rev. Letter)

The Lot ID and Rev. letter are separated by two spaces.

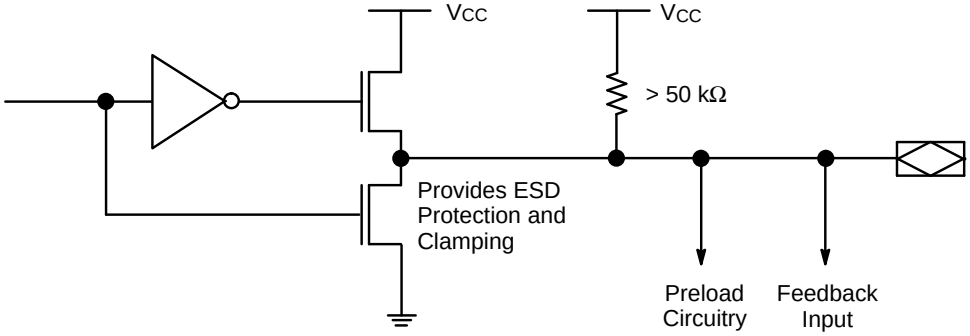
ROBUSTNESS FEATURES

The PALCE26V12 has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR REV. B VERSION*



Typical Input



Typical Output

16072E-16

*

Device	Rev. Letter
PALCE26V12-15	B
PALCE26V12-20	

Topside Marking:

AMD CMOS PLD's are marked on top of the package in the following manner:

PALCE xxxx

Datecode (4 numbers) LOT ID (3 characters) – – (Rev. Letter)

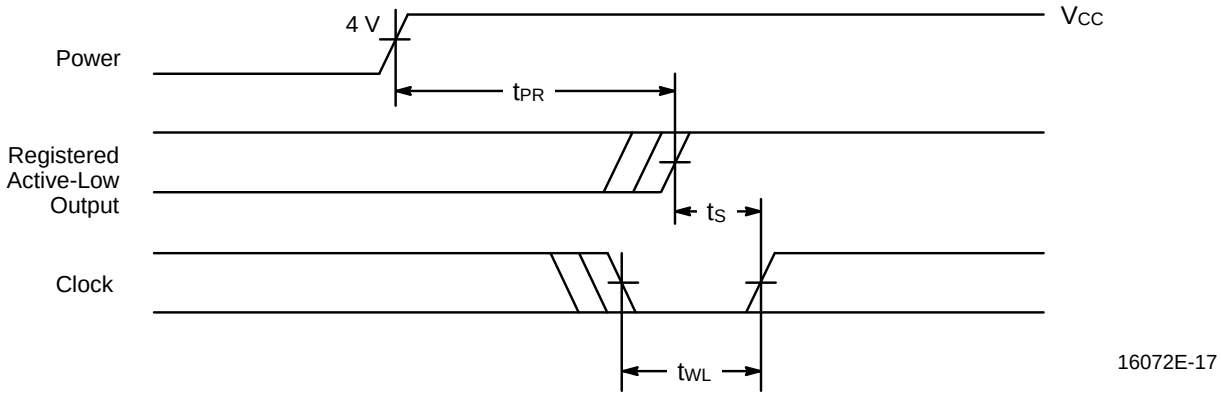
The Lot ID and Rev. letter are separated by two spaces.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

PALCE26V12

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		19	18	°C/W
θ_{ja}	Thermal impedance, junction to ambient		65	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	59	48	°C/W
		400 lfpm air	54	44	°C/W
		600 lfpm air	50	39	°C/W
		800 lfpm air	50	37	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

f_{MAX} Parameters

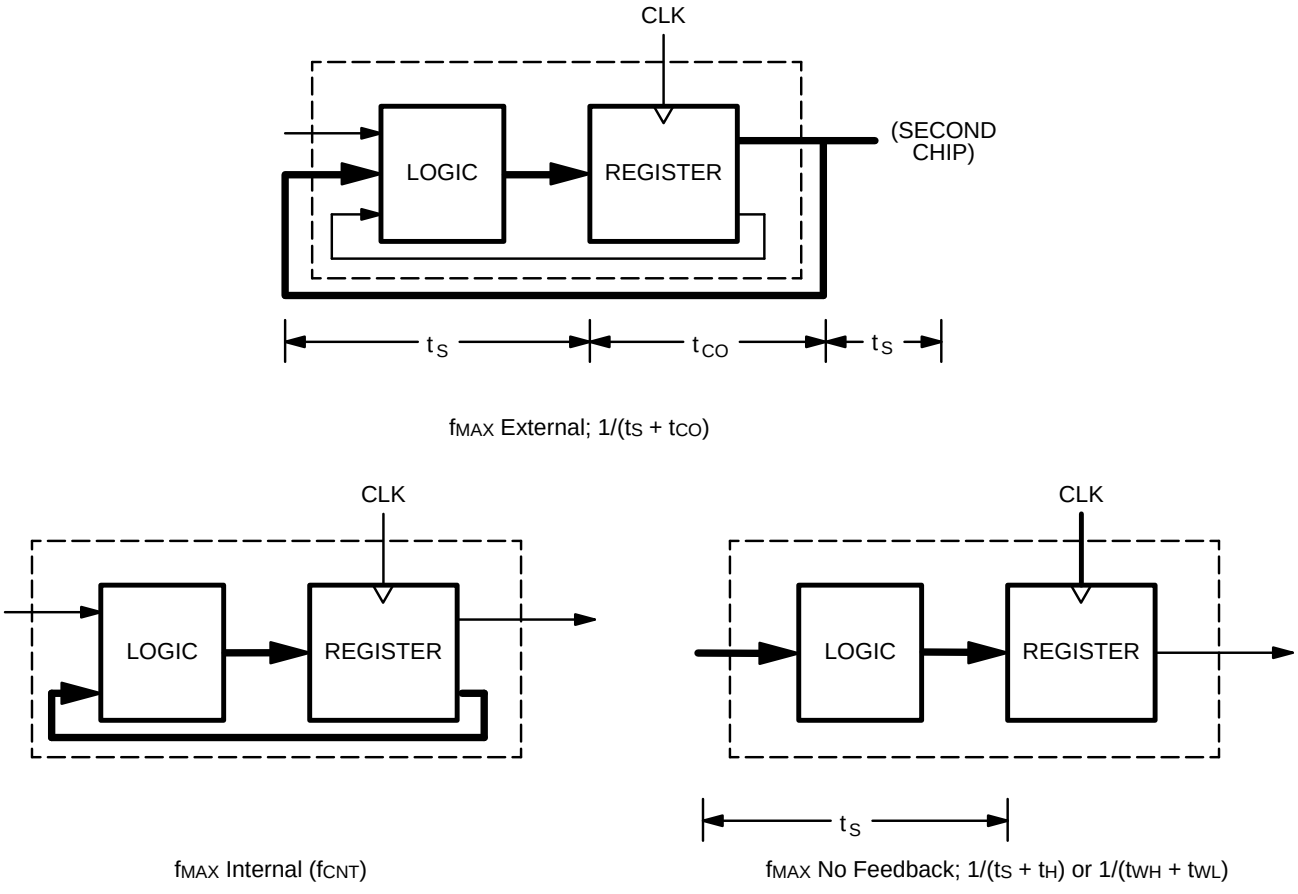
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design, therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

f_{MAX} external and f_{MAX} no feedback are calculated parameters. f_{MAX} external is calculated from t_S and t_{CO}, and f_{MAX} no feedback is calculated from t_{WL} and t_{WH}. f_{MAX} internal is measured.



f_{MAX} External; $1/(t_S + t_{CO})$

f_{MAX} Internal (f_{CNT})

f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

16072E-18

PALCE22V10 Family

24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As fast as 5-ns propagation delay and 142.8 MHz f_{MAX} (external)**
- **Low-power EE CMOS**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Peripheral Component Interconnect (PCI) compliant (-5/-7/-10)**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP, 24-pin SOIC, 24-pin Flat-pack and 28-pin PLCC and LCC packages save space**
- **5-ns and 7.5-ns versions utilize split lead-frames for improved performance**

GENERAL DESCRIPTION

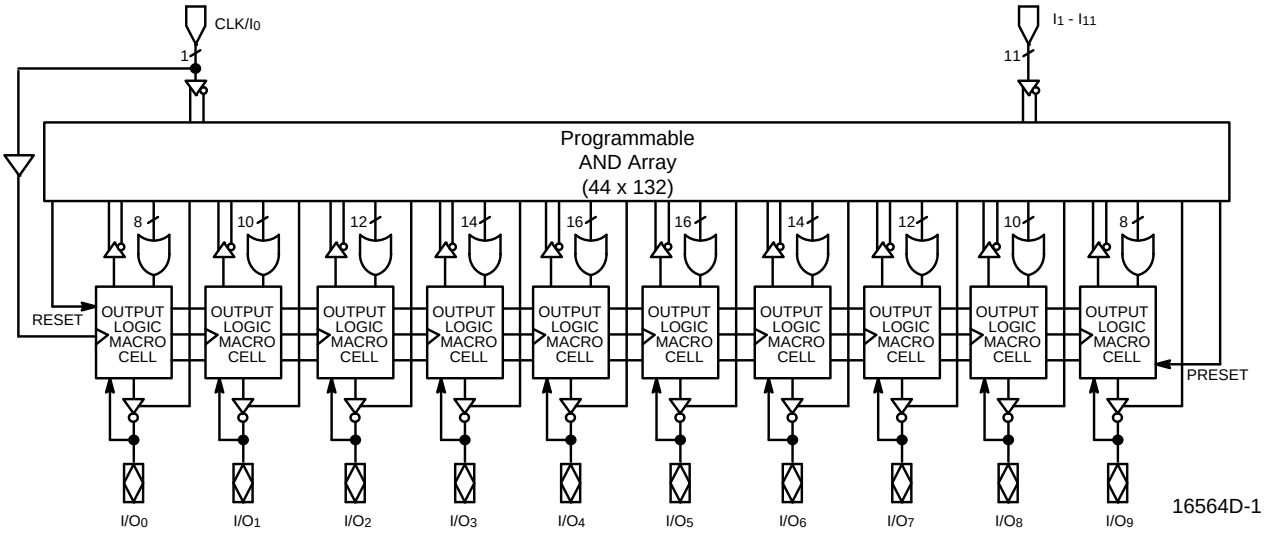
The PALCE22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar.

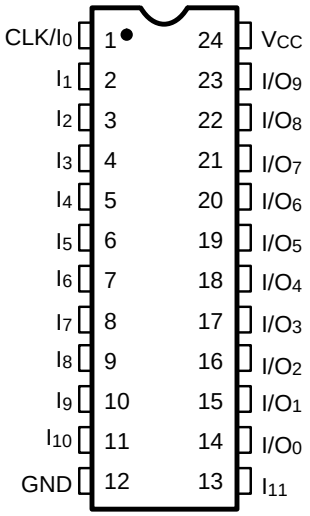
BLOCK DIAGRAM



CONNECTION DIAGRAMS

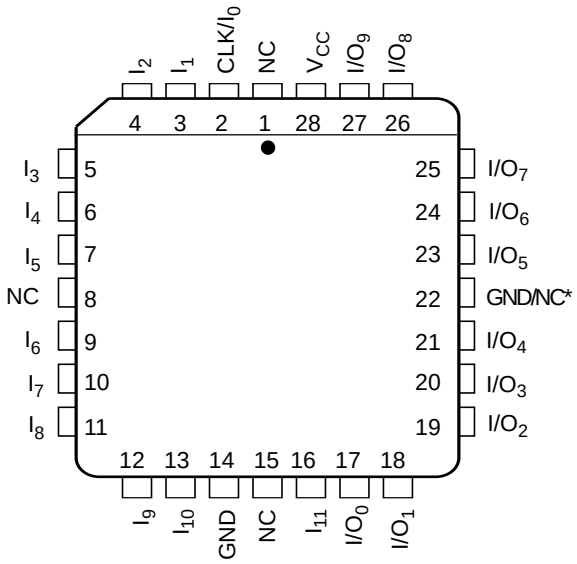
Top View

SKINNYDIP/SOIC/FLATPACK



16564D-2

PLCC/LCC



16564D-3

** For -5, this pin must be grounded for guaranteed data sheet performance. If not grounded, AC timing may degrade by about 10%.*

Note:

Pin 1 is marked for orientation.

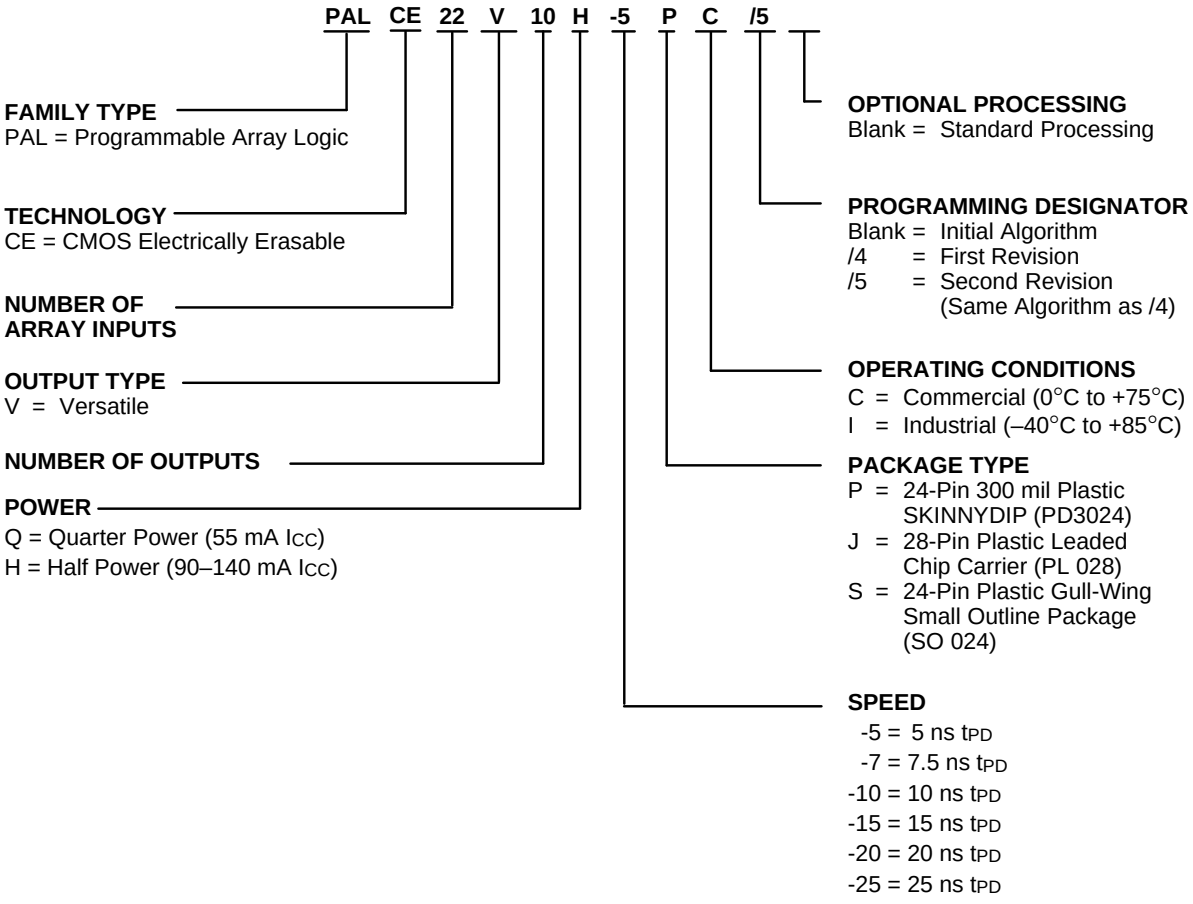
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE22V10-5	JC	/5
PALCE22V10H-7	PC, JC	
PALCE22V10H-10	PC, JC, SC, PI, JI, ZC	
PALCE22V10Q-10	PC, JC	
PALCE22V10H-15	PC, JC, PI, JI, ZC	Blank, /5, /4
PALCE22V10Q-15	PC, JC	/5
PALCE22V10H-20	PI, JI	/4
PALCE22V10H-25	PC, JC, SC, PI, JI	Blank, /4
PALCE22V10Q-25	PC, JC	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE22V10 allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

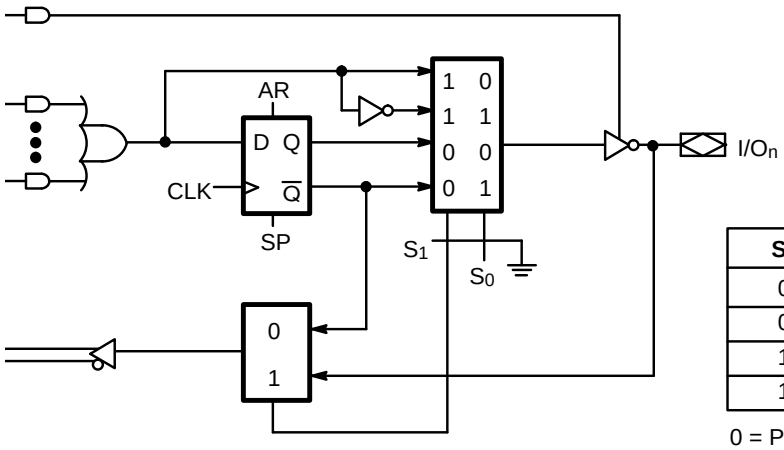
Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 1). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 – S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

The PALCE22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

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Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

Each macrocell of the PALCE22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

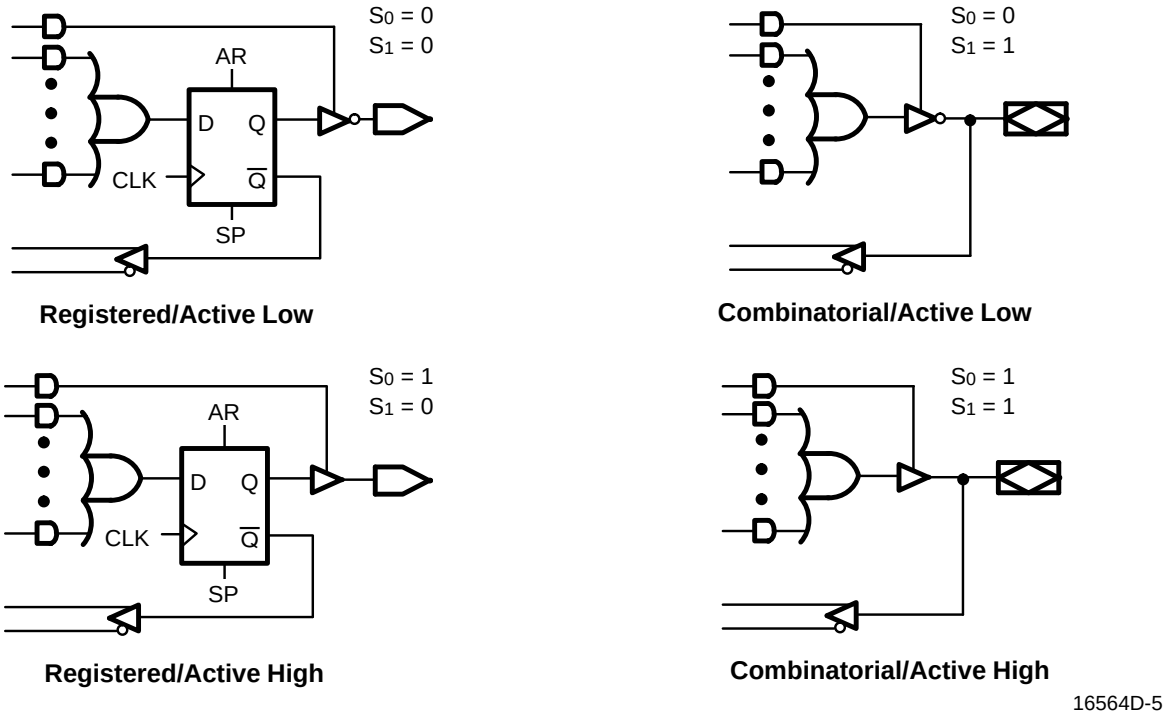


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10 design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALCE22V10 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

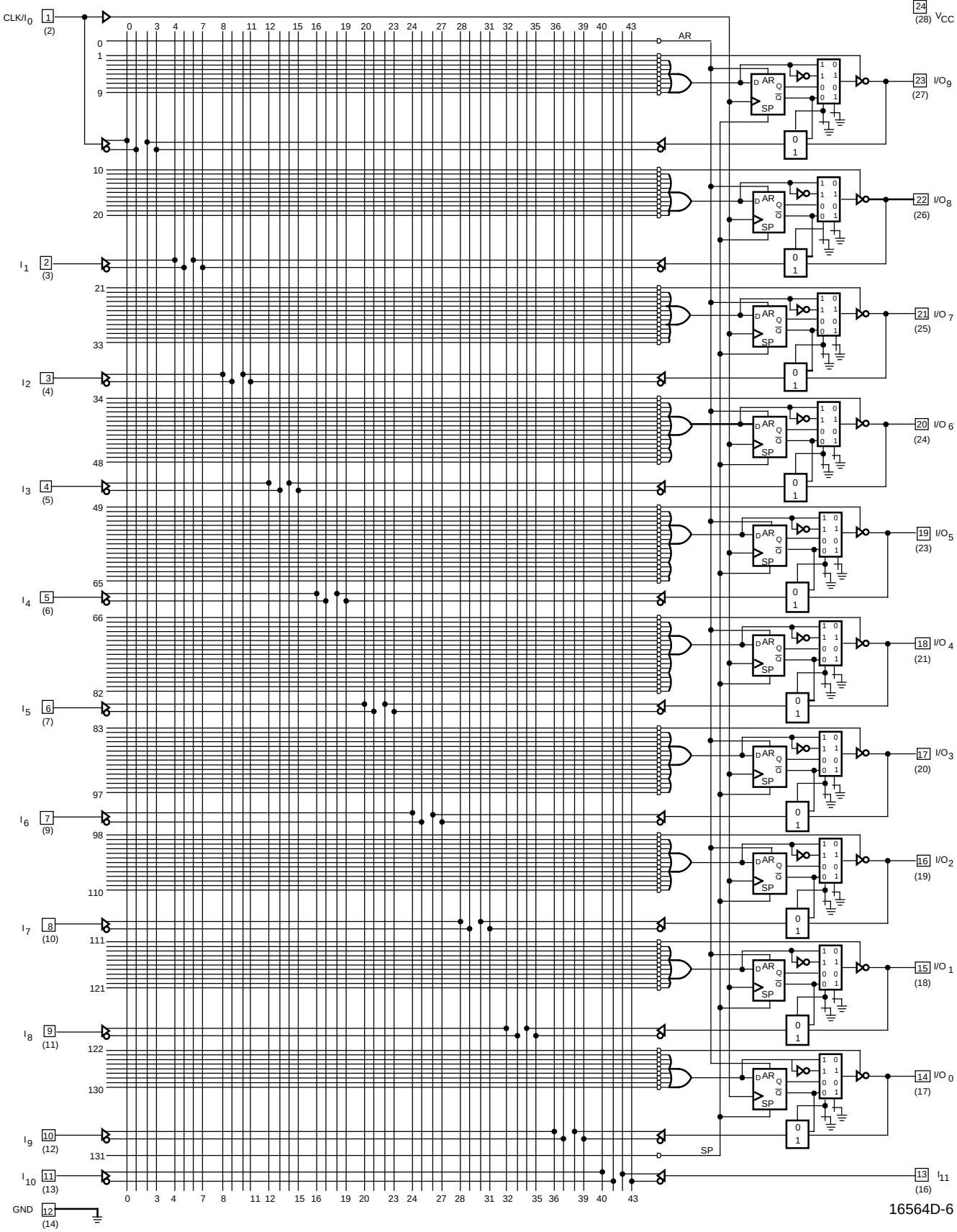
The high-speed PALCE22V10 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

PCI Compliance

The PALCE22V10H-5/7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The PALCE22V10H-5/7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design.

LOGIC DIAGRAM

SKINNYDIP/SOIC/FLATPACK (PLCC/LCC) Pinouts



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30	–130	mA
I_{CC} (Static)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		125	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-5		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				5	ns
t_{S1}	Setup Time from Input or Feedback			3		ns
t_{S2}	Setup Time from SP to Clock			4		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 3)				0.5	ns
t_{AR}	Asynchronous Reset to Registered Output				7.5	ns
t_{ARW}	Asynchronous Reset Width			4.5		ns
t_{ARR}	Asynchronous Reset Recovery Time			4.5		ns
t_{SPR}	Synchronous Preset Recovery Time			4.5		ns
t_{WL}	Clock Width	LOW		2.5		ns
t_{WH}		HIGH		2.5		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	142.8		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	150		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	200		MHz
t_{EA}	Input to Output Enable Using Product Term Control				6	ns
t_{ER}	Input to Output Disable Using Product Term Control				5.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Skew is measured with all outputs switching in the same direction.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max T_A = 25°C (Note 3)	–30	–130	mA
I_{CC} (Static)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		115	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-7 PDIP Min	-7 PDIP Max	-7 PLCC Min	-7 PLCC Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			3	7.5	3	7.5	ns
t_{S1}	Setup Time from Input or Feedback			5		4.5		ns
t_{S2}	Setup Time from SP to Clock			6		6		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output			2	5	2	4.5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 3)				1		1	ns
t_{AR}	Asynchronous Reset to Registered Output				10		10	ns
t_{ARW}	Asynchronous Reset Width			7		7		ns
t_{ARR}	Asynchronous Reset Recovery Time			7		7		ns
t_{SPR}	Synchronous Preset Recovery Time			7		7		ns
t_{WL}	Clock Width	LOW		3.5		3.0		ns
t_{WH}		HIGH		3.5		3.0		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	100		111		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	125		133		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	142.8		166		MHz
t_{EA}	Input to Output Enable Using Product Term Control				7.5		7.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5		7.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Skew is measured with all outputs switching in the same direction.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max T_A = 25° C (Note 3)	–30	–130	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		120	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_{S1}	Setup Time from Input or Feedback			6		ns
t_{S2}	Setup Time from SP to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	83.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V, T_A = 25°C (Note 3)	–30	–130	mA
I_{CC} (Static)	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max (Note 4)		55	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is guaranteed worst case under test condition. Refer to the I_{CC} vs. frequency graph for typical I_{CC} characteristics.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10		Unit
				Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input, Feedback or SP to Clock			6		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	83		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CO})$ (Note 4)	110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground (H/Q-15) . . . . +4.75 V to +5.25 V

Supply Voltage (V_{CC}) with Respect to Ground (H/Q-25) . . . . . +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V, T_A = 25°C (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min	-15 Max	-25 Min	-25 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		15	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		25		ns
t_{SPR}	Synchronous Preset Recovery Time			10		25		ns
t_{WL}	Clock Width	LOW		8		13		ns
t_{WH}		HIGH		8		13		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	58.8		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C) . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage		I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage		I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage		Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage		Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current		V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current		V_{IN} = 0 V, V_{CC} = Max (Note 2)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH		V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW		V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current		V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)	–30	–130	mA
I_{CC} (Static)	Supply Current	H-20/25	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		100	mA
		H-10/15			110	
I_{CC} (Dynamic)	Supply Current		V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz		130	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

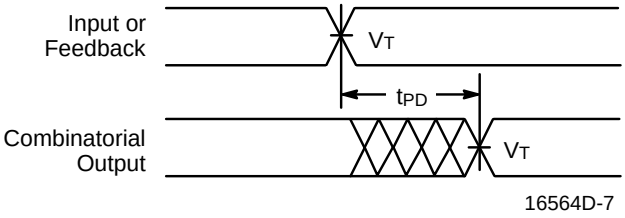
SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10		-15		-20		-25		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				10		15		20		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			7		10		12		15		ns
t_H	Hold Time			0		0		0		0		ns
t_{CO}	Clock to Output				6		10		12		15	ns
t_{AR}	Asynchronous Reset to Registered Output				13		20		25		25	ns
t_{ARW}	Asynchronous Reset Width			8		15		20		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		10		20		25		ns
t_{SPR}	Synchronous Preset Recovery Time			8			10		14	25		ns
t_{WL}	Clock Width	LOW		4		8		10		13		ns
t_{WH}		HIGH		4		8		10		13		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	83.3		50		41.6		33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	110		58.8		45.4		35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		83.3		50		38.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10		15		20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				9		15		20		25	ns

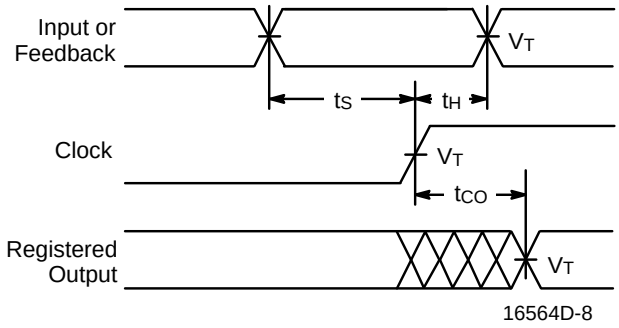
Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – t_S.*

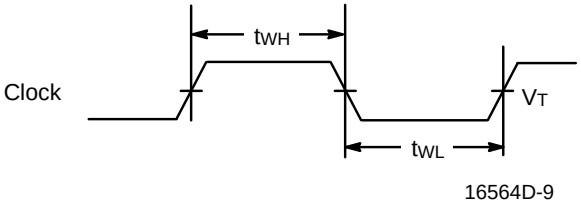
SWITCHING WAVEFORMS



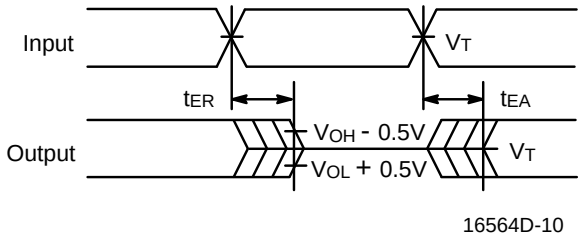
Combinatorial Output



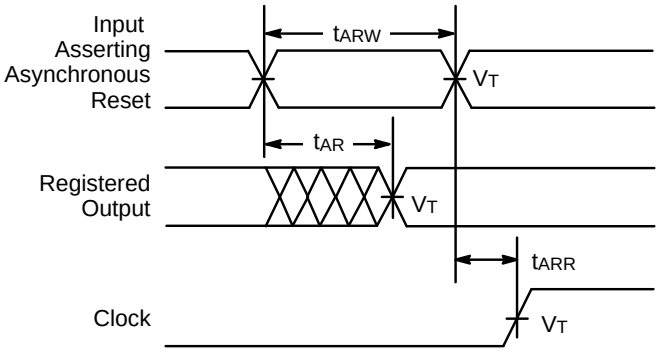
Registered Output



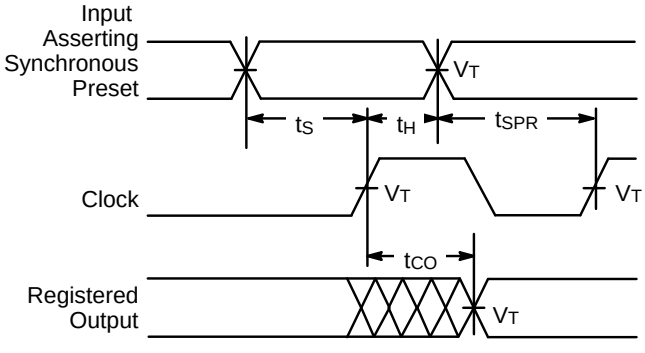
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

Notes:

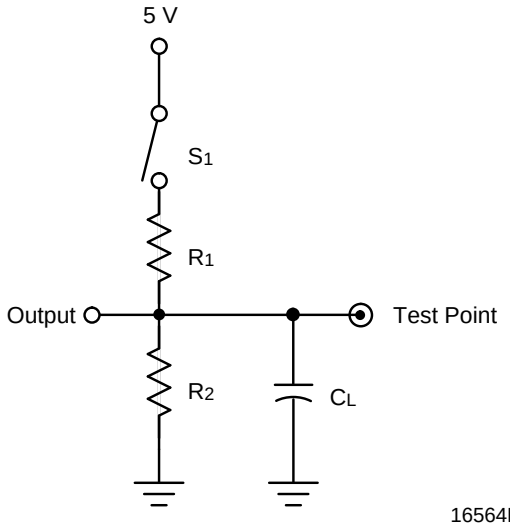
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

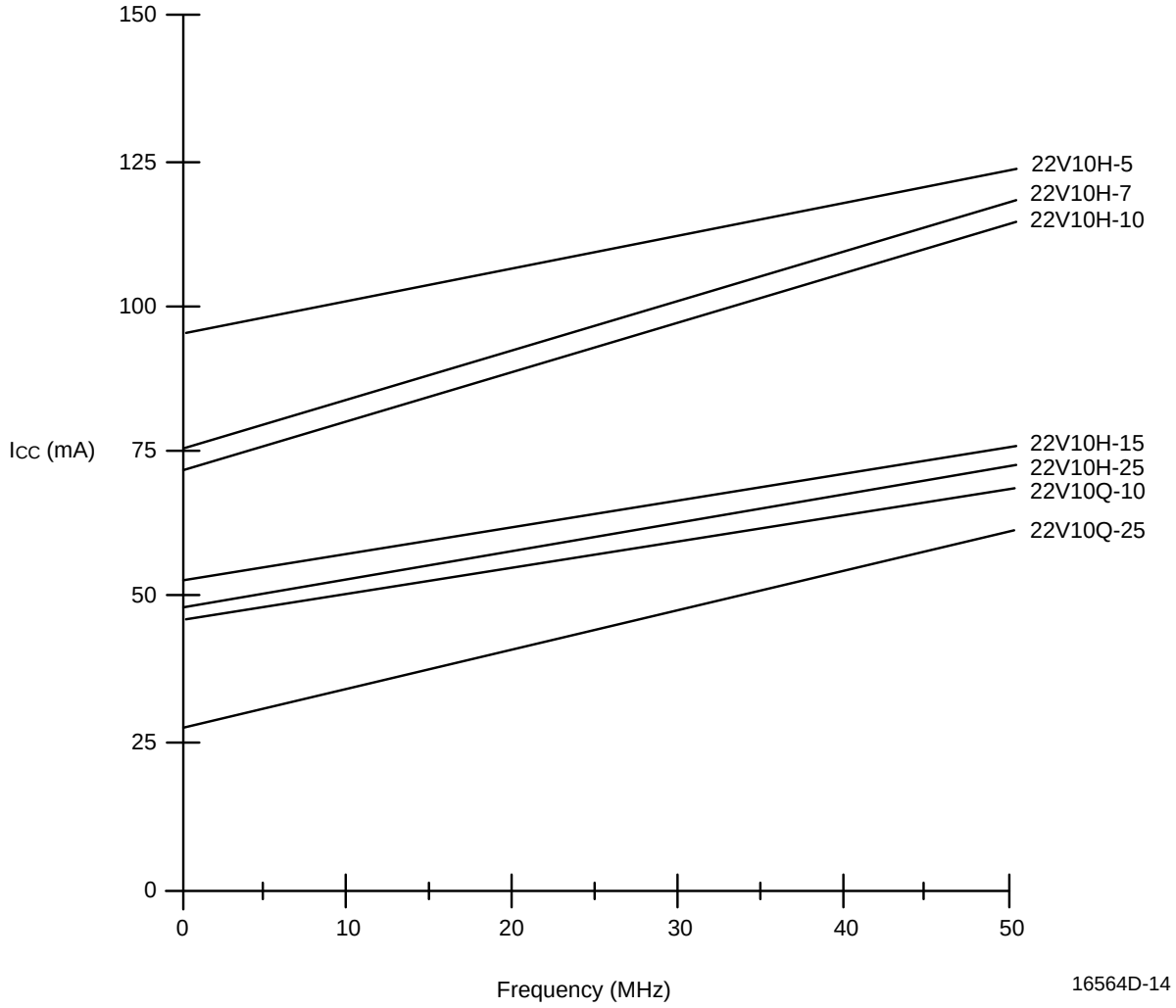


16564D-13

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	All except H-5/7: 390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF		H-5/7: 300 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



I_{CC} vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

ENDURANCE CHARACTERISTICS

The PALCE22V10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

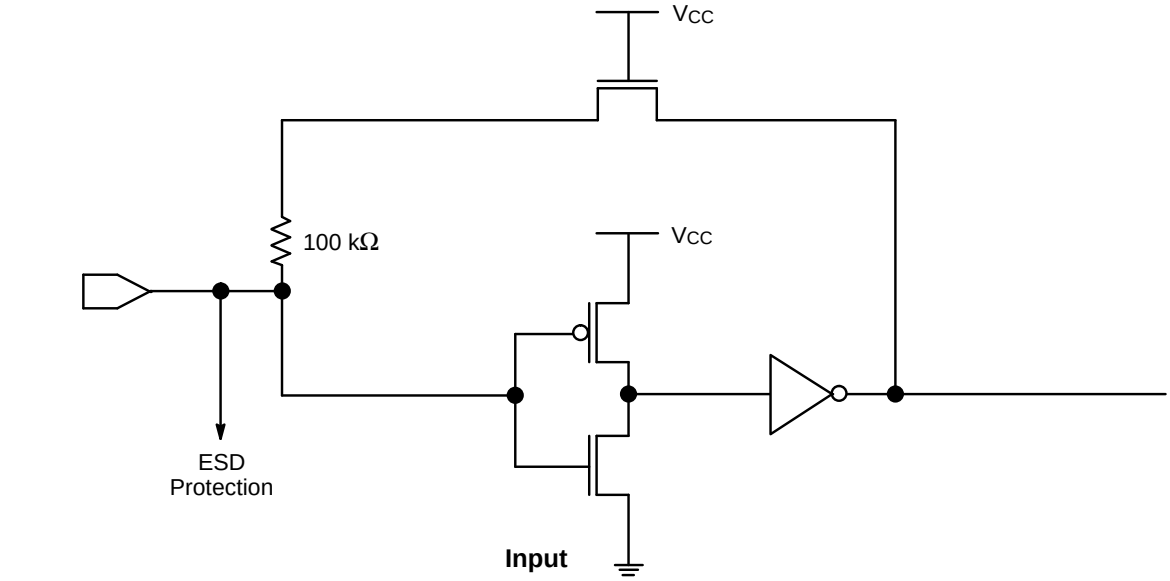
Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

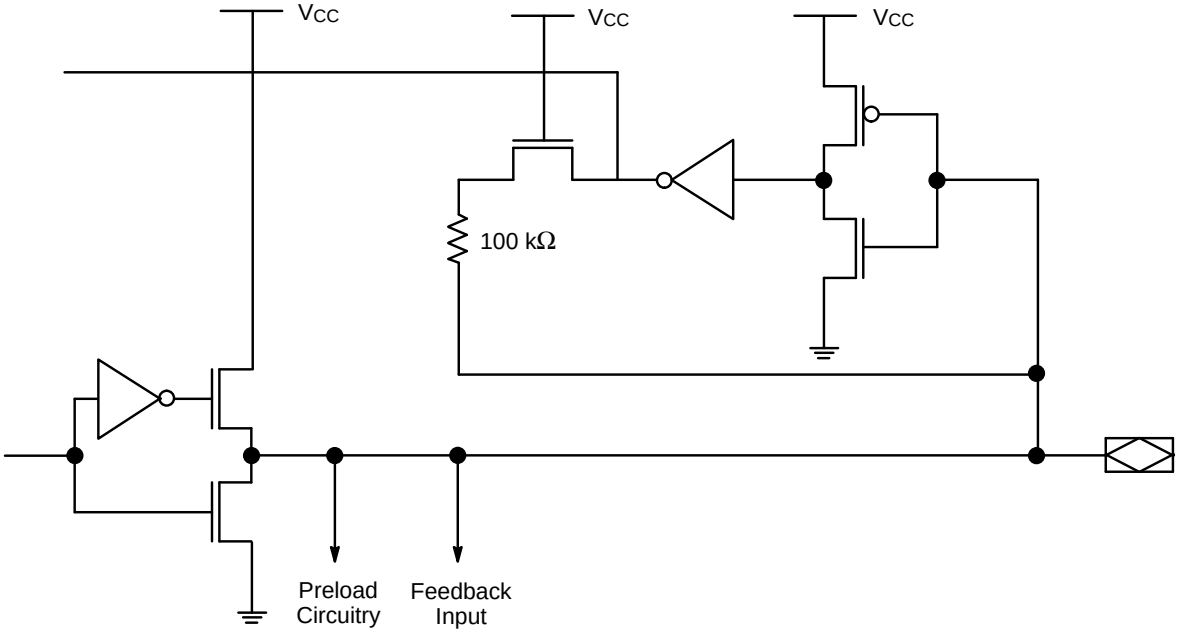
Bus-Friendly Inputs

The PALCE22V10H-15/25, Q-25 (Com'l) and H-20 (Ind) inputs and I/O loop back to the input after the second stage of the input buffer. This configuration reinforces the state of the input and pulls the voltage away from the input threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, see the input/output equivalent schematics.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR SELECTED /4 DEVICES*



Input



16564D-15

Output

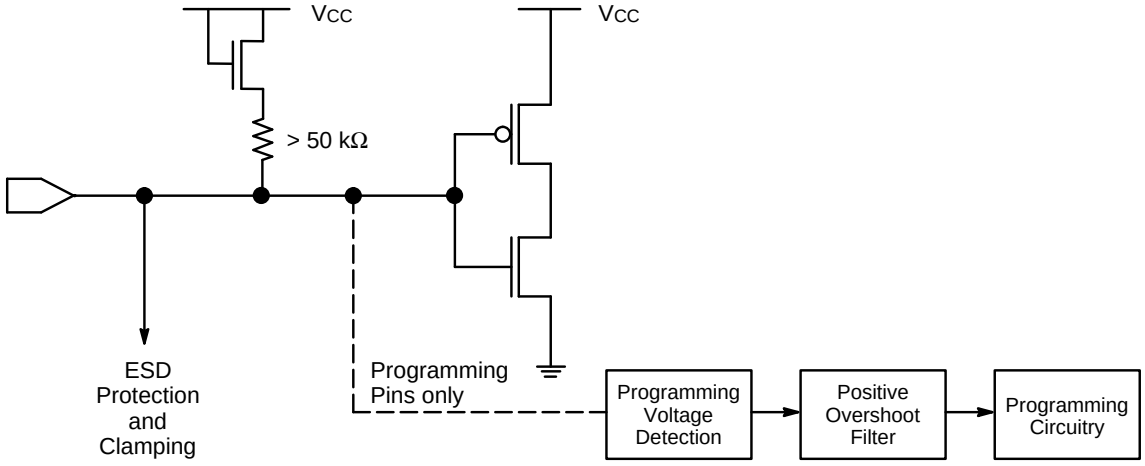
*

Device	Rev Letter
PALCE22V10H-15	H
PALCE22V10H-20	
PALCE22V10H-25	
PALCE22V10Q-25	I

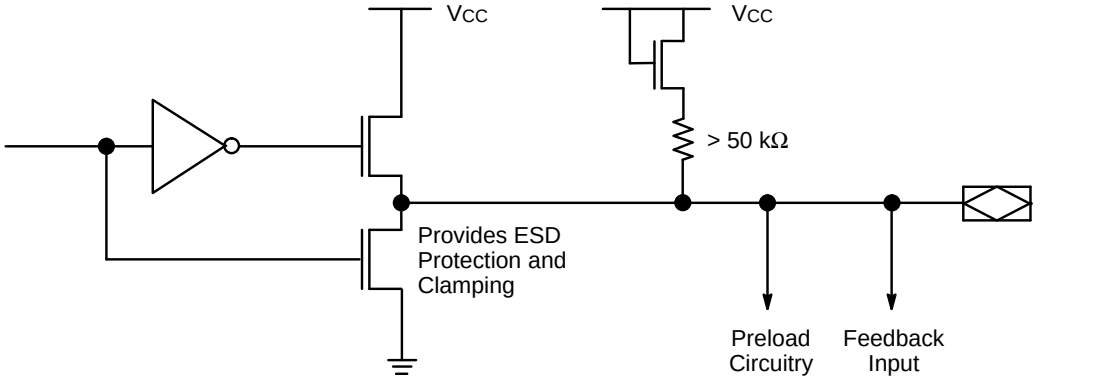
ROBUSTNESS FEATURES

The PALCE22V10X-X/5 devices have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 version. Selected /4 devices are also being retrofitted with these robustness features. See the chart below for device listing.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSION AND SELECTED /4 DEVICES*



Typical Input



Typical Output

*

Device	Rev Letter
PALCE22V10H-15	D
PALCE22V10H-25	D
PALCE22V10Q-25	F

Topside Marking:

AMD CMOS PLD's are marked on top of the package in the following manner:

PALCEXXXX
Datecode (3 numbers) Lot ID (4 characters)– –(Rev Letter)

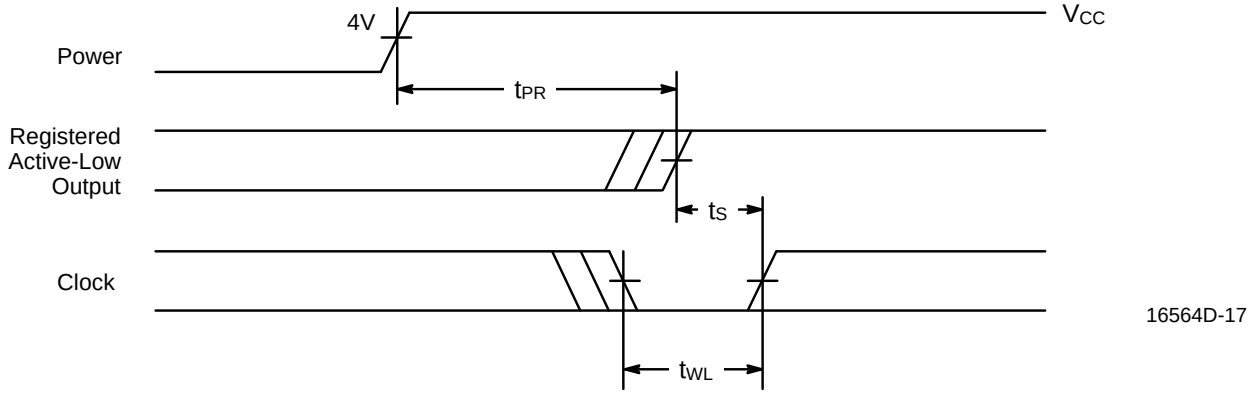
The Lot ID and Rev Letter are separated by two spaces.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

PALCE22V10/4 (PALCE22V10H-15)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		15	16	°C/W
θ_{ja}	Thermal impedance, junction to ambient		72	54	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	67	49	°C/W
		400 lfpm air	60	43	°C/W
		600 lfpm air	53	37	°C/W
		800 lfpm air	46	31	°C/W

PALCE22V10/5 (PALCE22V10H-10)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θ_{jc}	Thermal impedance, junction to case		20	18	°C/W
θ_{ja}	Thermal impedance, junction to ambient		73	55	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	66	48	°C/W
		400 lfpm air	61	43	°C/W
		600 lfpm air	55	40	°C/W
		800 lfpm air	52	37	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.