PBA 3369/1
Dual Channel Complete Line Interface Circuit, DCLIC

Description

The PBA 3369/1 is a Dual Channel Complete Line Interface Circuit (DCLIC) manufactured in thick-film technology.

The PBA 3369/1 Dual CLIC consists of two Ericsson SLIC´s, two Combo 2 Codecs and all other necessary components to interface two seperate analogue extensions to the PCM highway.

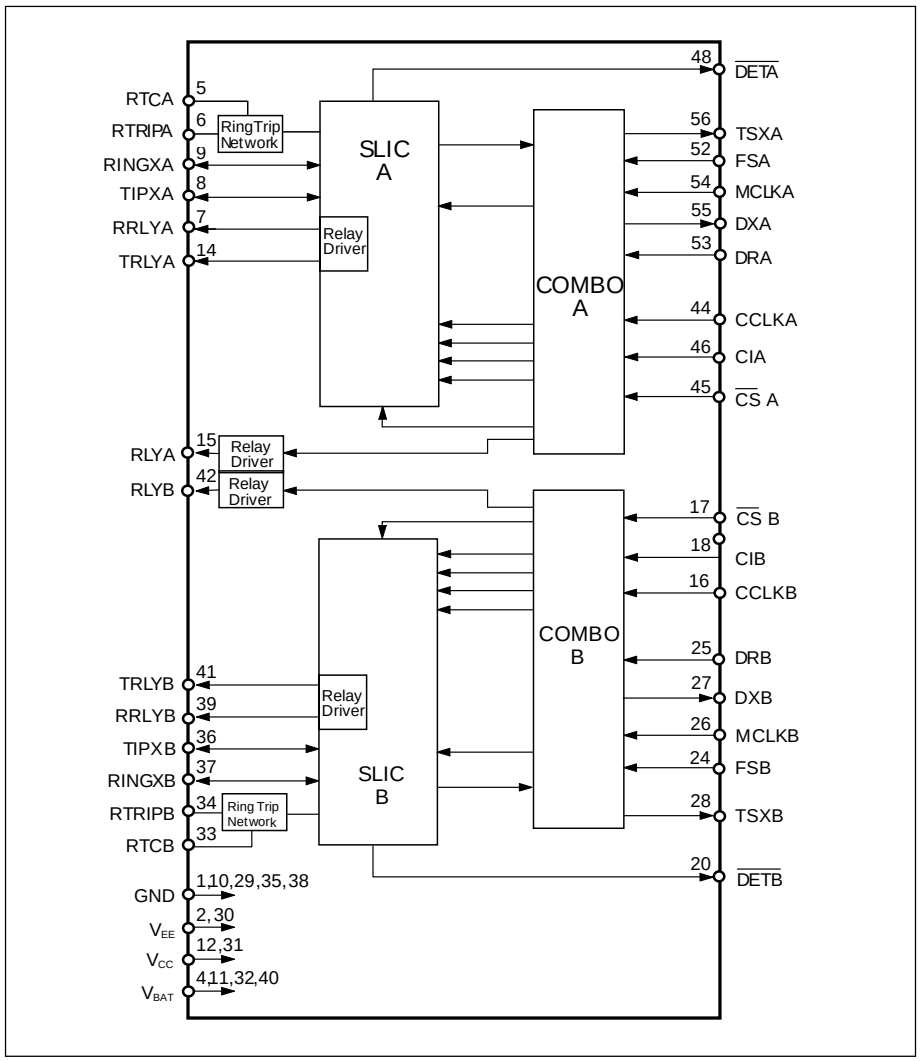

Figure 1: Block Diagram

Key Features

- Constant Current. I_{LDC}=min 18 mA at R_{LOOP}=1800 Ω
- Software programmable functions:
  - Receive gain *(with 0 dBm0 in PCM- code*):
  - -20 to 0 dB in 0,1 dBsteps
  - Transmitt gain: *(with 0 dBm0 at 2-wire*):
    -5 to 0 dB in 0,1 dB steps
    Transmit and Receive channel can be turned off
  - Hybrid balance cancellation
  - Time slot Assignments
  - SLIC control
  - Relay drivers
- Polarity reversal
- On-Hook Transmission
- Three relay drivers/line; a total of six relay drivers
- Nominal impedance Z_{TR}=200 Ω+ (680 Ω//100 nF)
- Longitudinal balance; typical 60 dB
- Nominal V_{BAT}=- 48 V
- Few additional external components needed
- Small physical size: 34,4 x 71,1 mm

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature				
Storage temperature range	T_{stg}	-40	+125	°C
Power Supply				
Positive Supply voltage with respect to Ground (GND)	V_{CC}	-0,4	+6,5	V
Negative Supply voltage with respect to Ground	V_{EE}	-6,5	+0,4	V
Battery voltage with respect to Ground	V_{BAT}	-70	+0,4	V
Ring Relay Driver				
Relay Supply voltage	V_{RRLY}	V_{BAT}	V_{CC}	V
Current	I_{RRLY}		80	mA
Test Relay Driver				
Relay Supply voltage	V_{TRLY}	V_{BAT}	V_{CC}	V
Current	I_{TRLY}		80	mA
Additional Relay Driver				
Relay Supply voltage	V_{RLY}	-30	V_{CC}	V
Current	I_{RLY}		70	mA
TIPX and RINGX terminals (V_{BAT} = -50V)				
Voltage (each terminal), Continous (with respect to GND)	V_{TA}, V_{RA}	-70	1	V
Voltage (each terminal), Pulse t_{ON} < 10 ms. t_{REP}>10 s, (Note 1)	V_{TA}, V_{RA}	-70	5	V
Voltage (each terminal), Pulse t_{ON} < 1 µs. t_{REP}>10 s, (Note 1)	V_{TA}, V_{RA}	-90	10	V
Voltage (each terminal), Pulse t_{ON} < 250 ns. t_{REP}>10 s, (Note 1)	V_{TA}, V_{RA}	-120	15	V
Current (each terminal)	I_{DCMET}	-105	105	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Temperature					
Ambient temperature range, Operating	T_{amb}	0		+70	°C
Ambient temperature range, Test	T_{amb}		+23		°C
Power Supply					
Positive Supply voltage with respect to Ground (GND)	V_{CC}	+4,75	+5	+5,25	V
Negative Supply voltage with respect to Ground	V_{EE}	-5,25	-5	-4,75	V
Battery voltage with respect to Ground	V_{BAT}	-56	-48	-44	V

Electrical Characteristics

T_{amb} = 0 - 70 °C, V_{CC}= +5 V ± 5 %, V_{EE}=-5 V ± 5 %, V_{BAT}=-44 - -56 V, R_{LDC}= 600 Ω, Z_L=200 Ω+ (680 Ω//100 nF) See also fig 7

Parameter	Condition	Min	Typical	Max	Unit
Battery Feed Characteristics					
Line Current	$R_L \leq 1800\ \Omega$	18,0		28,0	mA
Line Voltage	$R_L = \infty\ \Omega$, V_{BAT}= -48 V	35		39	V
Battery Feed Characteristics, Polarity Reversad					
Line Current	$R_L \leq 1800\ \Omega$	-28,0		-18,0	mA
Line Voltage	$R_L = \infty\ \Omega$, V_{BAT}= -48 V	-39		-35	V

Electrical Characteristics cont.

Parameter	Ref. fig.	Condition	Min	Typical	Max	Unit
Loop Current Detector						
Loop Resistance R_L		Active, $\overline{DET}$ output High ("1")	20			kΩ
Loop Resistance R_L		Stand-by, $\overline{DET}$ output High ("1")	20			kΩ
Loop Resistance R_L		Active, $\overline{DET}$ output Low ("0")			2,3	kΩ
Loop Resistance R_L		Stand-by, $\overline{DET}$ output Low ("0")			2,3	kΩ
Off hook Detection delay time		-			100	ms
Dial Pulse Distortion, *(Note 6)*		10 pulses/s, Period 1000 ± 100 ms, *(Note 2)*	-10	0	10	ms
Ring Trip Detector, *(Note 6)*						
Delay time from Off hook ringing to detection. ($\overline{DET}$ from High to Low)		R_L = 1800 Ω, U_{RG}= 60 V			150	ms
$\overline{DET}$ minimum output low, "0" time		-	20	30		ms
Ring Relay Driver						
On-state Voltage		I_{OL}= 25 mA	(V_{CC}-2,0)	(V_{CC}-1,8)		V
Test Relay Driver						
On-state Voltage		I_{OL}= 25 mA	(V_{CC}-2,0)	(V_{CC}-1,8)		V
Additonal Relay Driver						
On-state Voltage		I_{OL}= 25 mA	(V_{CC}-1,0)			V
Power Dissipation per Line		**V_{BAT} = - 48 V**				
Active (Off hook)		R_L= 500 Ω		1150	1315	mW
Active (Off hook)		R_L= 0 Ω		1450	1650	mW
Active (On hook), (Note 5)		R_L ≥ 20 kΩ		350	440	mW
Stand-By (On hook), (Note 5)		R_L ≥ 20 kΩ, COMBO power-up		320	400	mW
Stand-By (On hook), (Note 5)		R_L ≥ 20 kΩ, COMBO power-down. Power Amplifier Disabled		250	310	mW
Gain, Absolute						
The absolute reference level at the 2-wire interface, 0 dBm0		P= 1mW, Z_{TR}= 200Ω+(680Ω//100nF) f= 1014 Hz		0,9008		V_{RMS}
Transmit (A-D), Li = 0 dBr		f=1014 Hz, Level: -10dBm0	-0,4	0,0	+0,3	dB
Receive (A-D), Li = 0 dBr		f=1014 Hz, Level: -10dBm0	-0,4	0,0	+0,3	dB
Attenuation / Frequency Distortion						
Transmit connection (A-D)		Reference: f = 1014 Hz				
(CCITT Q552 3.1.1.5)		f = 200-300 Hz	-0,3	0,0	-	dB
		f = 300-400 Hz	-0,3	0,0	+1,0	dB
		f = 400-600 Hz	-0,3	0,0	+0,75	dB
		f = 600-2400 Hz	-0,3	0,0	+0,35	dB
		f = 2400-3000 Hz	-0,3	0,0	+0,55	dB
		f = 3000-3400 Hz	-0,3	0,0	+1,5	dB
Receive connection (D-A)		Reference: f = 1014 Hz				
(CCITT Q552 3.1.1.5)		f = 200-400 Hz	-0,3	0,0	+1,0	dB
		f = 400-600 Hz	-0,3	0,0	+0,75	dB
		f = 600-2400 Hz	-0,3	0,0	+0,35	dB
		f = 2400-3000 Hz	-0,3	0,0	+0,55	dB
		f = 3000-3400 Hz	-0,3	0,0	+1,5	dB

Electrical Characteristics cont.

Parameter	Condition	Min	Typical	Max	Unit
Variation of Gain with Input Level, *(Note 7)*					
Transmit (A-D) and	Reference: f = 1014 Hz, Level -10 dBm0				
Receive (D-A) connection	Input level = -55 to -50 dBm0	-1,5	0,0	+1,5	dB
(CCITT Q552 3.1.1.4)	Input level = -50 to -40 dBm0	-0,5	0,0	+0,5	dB
	Input level = -40 to -3 dBm0	-0,3	0,0	+0,3	dB
	Input level = -3 to +3 dBm0	-0,5	0,0	+0,5	dB
Signal to Total Distortion, *(Note 7)*					
Transmit (A-D) connection	Li = 0 dBr (Ref: CCITT Q552)				
(CCITT Q552 3.3.3)	Input level = -45 dBm0	19,9			dB
	Input level = -40 dBm0	24,9			dB
	Input level = -30 dBm0	32,9			dB
	Input level = -20 dBm0	35,0			dB
	Input level = -10 dBm0	35,0			dB
	Input level = 0 dBm0	35,0			dB
Receive (D-A) connection	Lo = 0 dBr (Ref: CCITT Q552)				
(CCITT Q552 3.3.3)	Input level = -45 dBm0	19,9			dB
	Input level = -40 dBm0	24,9			dB
	Input level = -30 dBm0	32,9			dB
	Input level = -20 dBm0	35,0			dB
	Input level = -10 dBm0	35,0			dB
	Input level = 0 dBm0	35,0			dB
Idle Channel Noise, (CCITT Q552 3.3.2)*(Note 8)*					
Transmit (A-D) connection	Li = 0 dBr			-66	dBm0p
Receive (D-A) connection	Lo = 0 dBr			-70	dBm0p
Power Supply Rejection Ratio (PSRR)					
V_{CC} to Analog Interface	f= 50 to 4000 Hz	35			dB
V_{EE} to Analog Interface	f= 50 to 4000 Hz	10			dB
V_{BAT} to Analog Interface	f= 50 to 4000 Hz	25			dB
Impedance					
Nominal Impedance	Z_{TR} = 200 Ω + (680 Ω // 100 nF)				
Return Loss	*Note 3*				
(CCITT Q552 2.1.1.2)	f= 300 Hz	14	30		dB
	f= 500 to 2000 Hz	18	35		dB
	f= 3400 Hz	14	30		dB
Longitudinal Balance, L-T	f= 300 to 600 Hz	40	60		dB
(CCITT Q552 2.2.2)	f= 600 to 3400 Hz	46	60		dB
Terminal Balance Return Loss, TBRL					
(CCITT Q552 3.1.8.1)	*Note 4*				
	f= 300 Hz	16	25		dB
	f= 500 to 2500 Hz	20	25		dB
	f= 3400 Hz	16	25		dB

Electrical Characteristics cont.

Parameter	Ref fig	Min	Typical	Max	Unit
Outband Signalling					
Transmit (A-D) connection	Input level: -25 dBm0				
(CCITT Q552 3.1.6)	f= 4600 to 72000 Hz				
	In-band signal			-50	dBm0
Receive (D-A) connection, *(Note 7)*	Input level: 0 dBm0				
(CCITT Q552 3.1.7)	f= 300 to 3400 Hz				
	Out-band signal (f= 4600 - 72000 Hz)			-25	dBm0
Intermodulation					
	2nd or 3rd order, 4-tone, A-D			-41	dB
	2nd or 3rd order, 4-tone, D-A			-41	dB
Crosstalk					
Input Crosstalk	CCITT Q552 3.1.4.1 (far-end) FEXT			-70	dBm0
Output Crosstalk	CCITT Q552 3.1.4.2 (far-end) FEXT			-73	dBm0
Digital Inputs					
Input Low voltage	All inputs	0,0		0,7	V
Input High voltage	All inputs	2,0		V_{CC}	V
Input Low current		-10		+10	µA
Input High current		-10		+10	µA

Parameter	Ref fig	Symbol	Min	Typical	Max	Unit
Timing Specification						
Frequency of Master Clock, MCLK	2	$1/T_{PM}$	2,037	2,048	2,062	MHz
Width of Master Clock High (V_{IH} to V_{IH})	2	t_{WMH}	80			ns
Width of Master Clock Low (V_{IL} to V_{IL})	2	t_{WML}	80			ns
Rise time of Master Clock (V_{IL} to V_{IH})	2	t_{RM}			30	ns
Fall time of Master Clock (V_{IH} to V_{IL})	2	t_{FM}			30	ns
Delay time to valid Data from FS	3	t_{DFD}			80	ns
Delay time from MCLK8 High to Data output Disabled	2	t_{DBZ}	15		80	ns
Setup time from DR valid to MCLK, Low	3	t_{SDB}	30			ns
Hold time from MCLK Low to DR Invalid	3	t_{HBD}	10			ns
Hold time from MCLK Low to FS high or low	3	t_{HBF}	0			ns
Setup time from FS to MCLK	3	t_{SFB}	30			ns
Delay time from MCLK8 low to TSX disabled (if FS low) FS low to TSX (if MCLK8 low) MCLK9 high to TSX (if FS still high)	2	t_{ZBT}	15		60	ns
Delay time from MCLK High to Data valid	2	t_{DBD}			80	ns
Setup time from FS to MCLK Low	2	t_{SFB}	30			ns
Hold time from MCLK Low to FS Low	2	t_{HBF}	0			ns
Delay time TSX Low	2	t_{DBT}			60	ns

Parameter	Ref fig	Symbol	Min	Typical	Max	Unit
Frequency of CCLK	4	f_{CCLK}			2,048	MHz

Period of CCLK High (V_{IH} to V_{IH})	4	t_{WCH}	160		
Period of CCLK Low (V_{IL} to V_{IL})	4	t_{WCL}	160		
Rise Time of CCLK (V_{IL} to V_{IH})	4	t_{RC}			50
Falltime of CCLK (V_{IH} to V_{IL})	4	t_{FC}			50
Hold time, CCLK Low to CS Low *(CCLK 1)*	4	t_{HCS}	10		
Hold time, CCLK Low to CS High *(CCLK 8)*	4	t_{HSC}	100		
Setup time, CS Transition to CCLK Low	4	t_{SSC}	70		
Setup time, CI Data In to CCLK Low	4	t_{SDC}	50		
Hold time, CCLK Low to CI Non-valid	4	t_{HCD}	50		
Setup time, CS Transistion to CCLK High	4	t_{SSCO}	50		

Notes

1. Requires D_{BAT}; see Figure 6.
2. Dial Pulse Distortion at the DET output. Pulse tone: 8-14 pulses / s, 40 to 77 % duty factor for in-out application of a external resistance (200 - 1800 Ω) on the two-wire terminal.
3. Rising log scale from 14 dB @ 300 Hz up to 18 dB @ 500 Hz and falling log scale from 18 dB @ 2000 Hz down to 14 dB @ 3400 Hz.
4. Rising log scale from 16 dB @ 300 Hz up to 20 dB @ 500 Hz and falling log scale from 20 dB @ 2000 Hz down to 16 dB @ 3400 Hz.
5. Both channels measured at the same time and divided by two
6. The CLIC state during the pause of the ringing cadence or pulse dialling shall be active.
7. At V_{BAT} = -44 V and R_{LDC} = 1800Ω the SLIC has start to saturate. This will effect some transmission parameters, for high signal levels (> -10dBm0).
8. The noise increase when the saturation guard becomes active arround R_{LDC} ≥1400 Ω but is still better than CCITT Q552.3.3.2.

Reference Figures

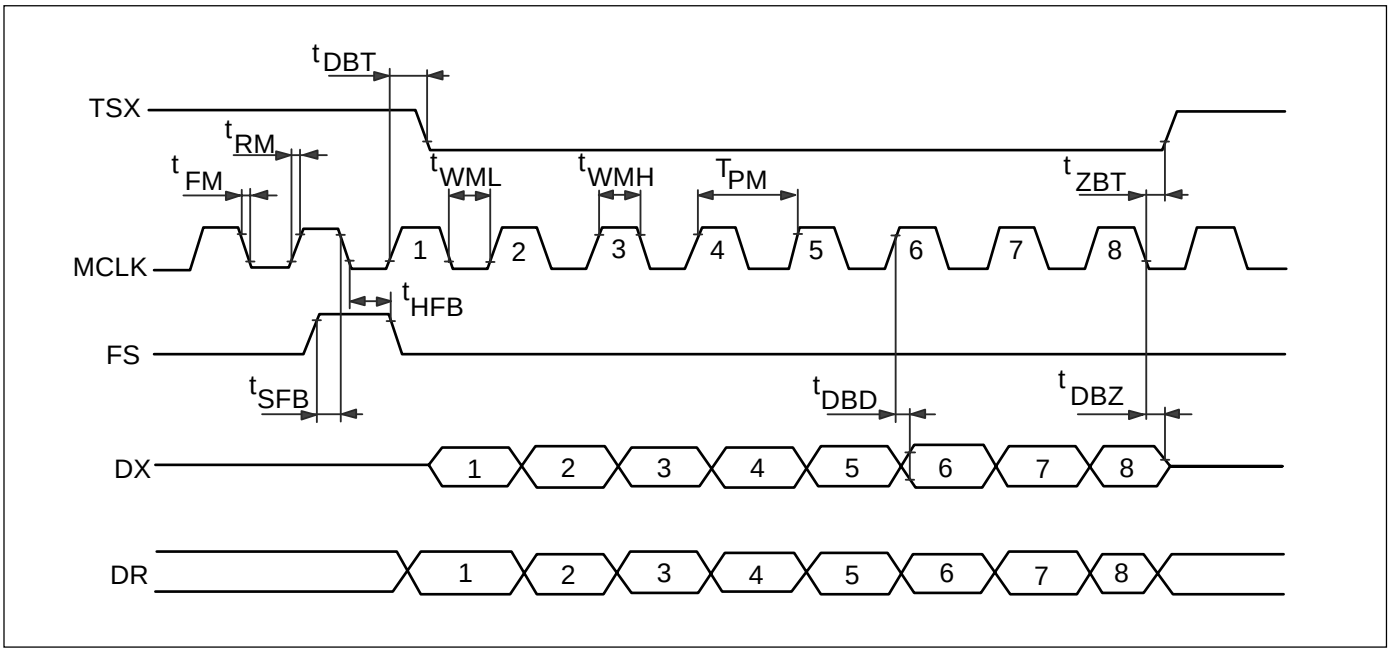

Figure 2. Short Frame Sync Timing diagram.

Reference Figures

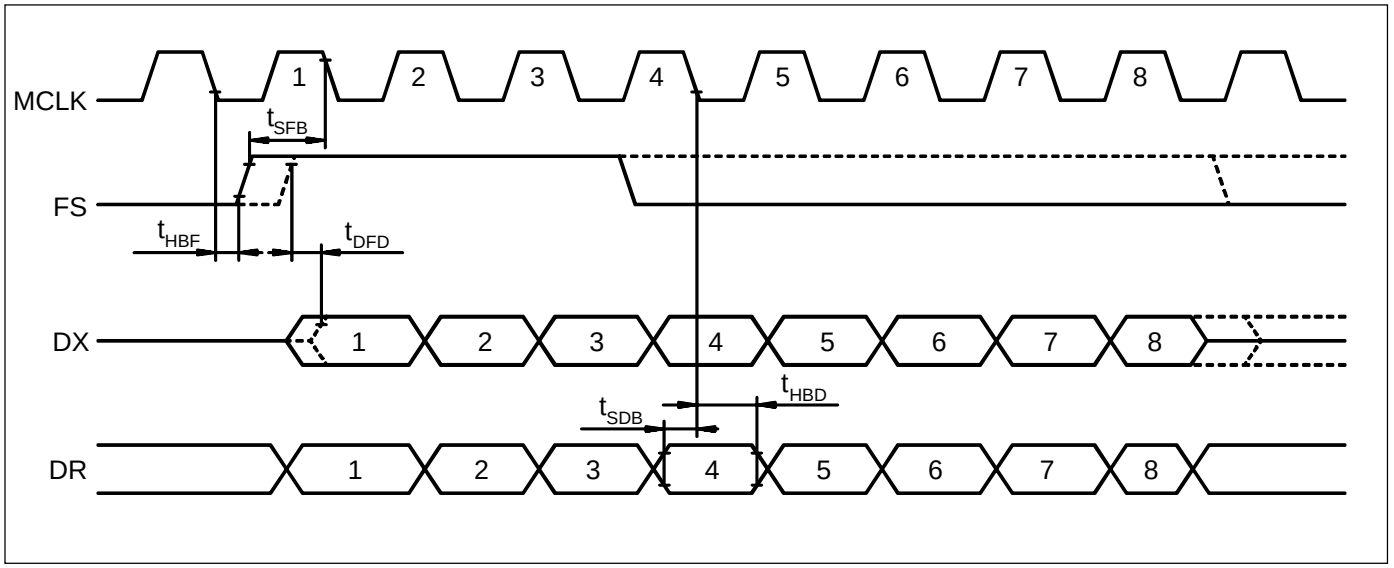

Figure 3. Long Frame Sync Timing diagram.

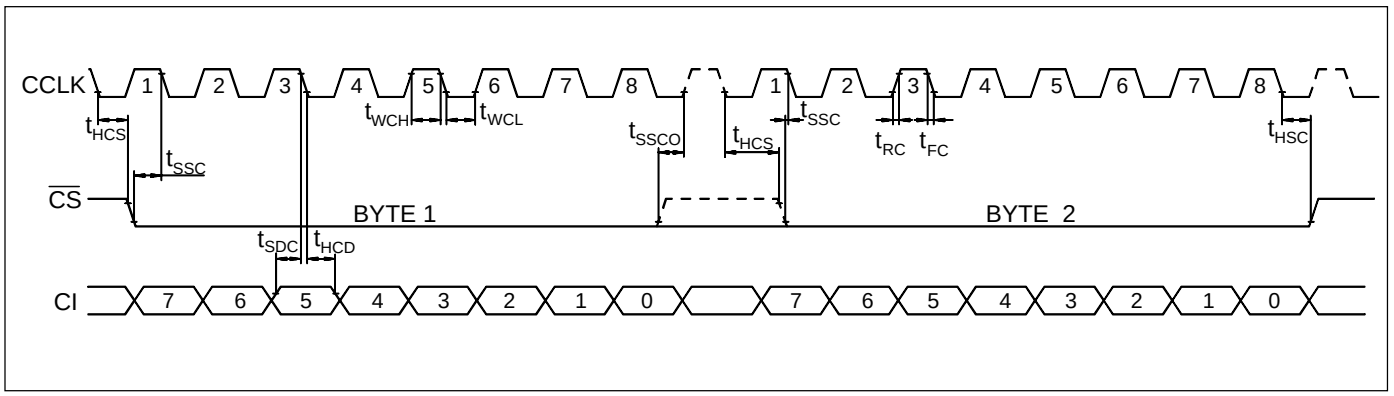

Figure 4. Control Timing diagram.

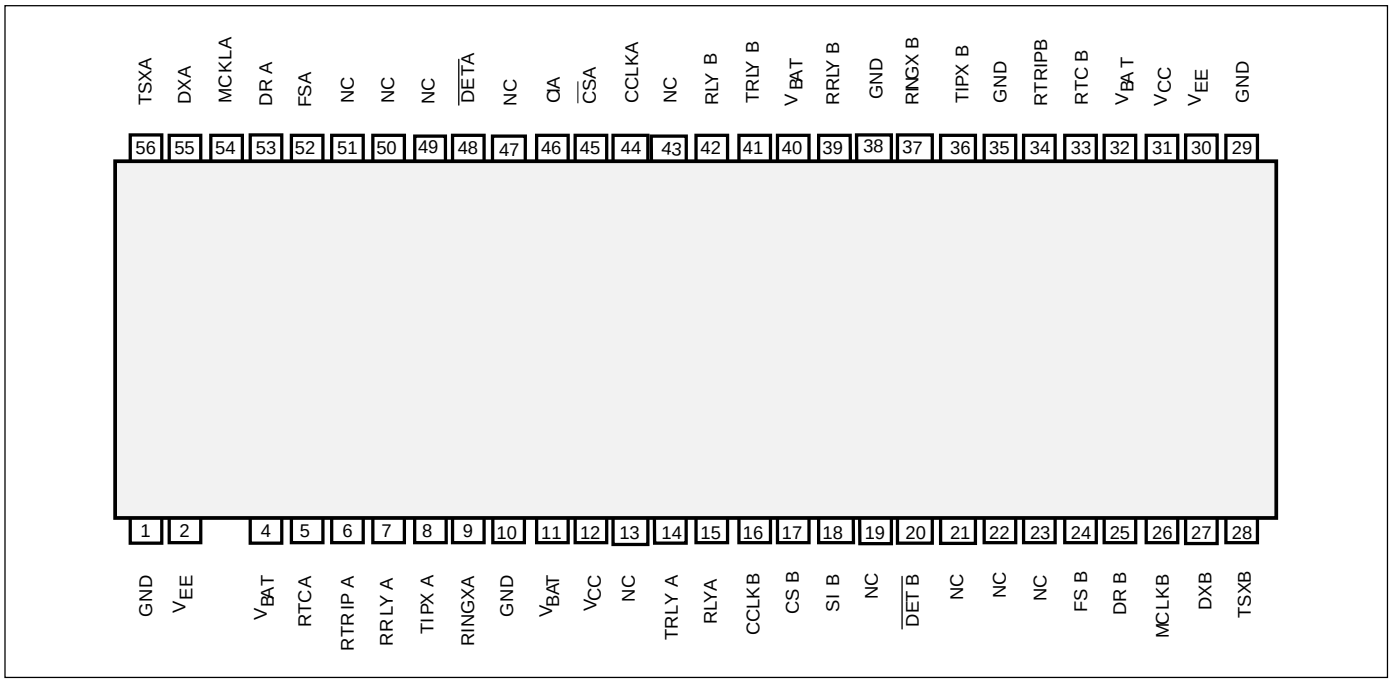

Figure 5. Pin-configuration, 56 pin DIL.

Pin Description

Pin	Symbol	Description
1	GND	Ground.
2	V_{EE}	Negative Supply Voltage, - 5V, for the CLIC.
3		Omitted Pin.
4	V_{BAT}	Battery Voltage, - 48 V to the CLIC.
5	RTC A	A ring Trip filter Capacitor input for Channel A. For standard performance of the CLIC, leave the pin open.
6	RTRIP	A Ring Trip network input for Channel A. Connect to the resistor RRT A. The resistor RRT A causes a voltage drop when Off-hook occurs during ringing. The voltage will cause a change of state in DET A.
7	RRLY A	Ring Relay driver output for Channel A. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
8	TIPX A	Tip lead input for Channel A to the CLIC from the subscriber line (two-wire).
9	RINGX A	Ring lead input for Channel A to the CLIC from the subscriber line (two-wire).
10	GND	Ground.
11	V_{BAT}	Battery Voltage, - 48 V to the CLIC.
12	V_{CC}	Positive Supply Voltage, + 5V, for the CLIC.
13	NC	Not connected pin.
14	TRLY A	Test Relay driver output for Channel A. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
15	RLY A	Additional Relay driver output for Channel A. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
16	CCLK B	Control Clock for Channel B. Clocks data into the shift-register on high-to-low
17	$\overline{CS}$ B	Chip Select for Channel B. When low. Control data can be written into the control register
18	CI B	Control Data Input for Channel B. Serial Control data is clocked into the Control register from this pin
19	NC	Not Connected pin.
20	$\overline{DET}$ B	Detector output for Channel B. The output is a Open-collector with internal pull-up resistor to V_{CC}.

Pin Description cont.

Pin	Symbol	Description
21	NC	Not connected pin.
22	NC	Not Connected pin
23	NC	Not Connected pin
24	FS B	Frame Sync for Channel B; Transmit and Receive.
25	DR B	PCM Receive Data Input for Channel B.
26	MCLK B	Master Clock for Channel B.
27	DX B	PCM Transmit data Output for Channel B; Tri-state.
28	TSX B	Time Slot for Channel B; Open-drain. Output pulse low during encoding.
29	GND	Ground.
30	V_{EE}	Negative Supply Voltage, - 5V, for the CLIC.
31	V_{CC}	Positive Supply Voltage, + 5V, for the CLIC.
32	V_{BAT}	Battery Voltage, - 48 V to the CLIC.
33	RTC B	Ring Trip filter Capacitor input for Channel B. For standard performance of the CLIC, leave the pin open.
34	RTRIP B	Ring Trip network input for Channel B. Connect to the resistor RRT B. The resistor RRT B causes a voltage drop when Off-hook occurs during ringing. The voltage will cause a change of state in DET B.
35	GND	Ground.
36	TIPX B	Tip lead input for Channel B to the CLIC from the subscriber line (two-wire).
37	RINGX B	Ring lead input for Channel B to the CLIC from the subscriber line (two-wire).
38	GND	Ground.
39	RRLY B	Ring Relay driver output for Channel B. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
40	V_{BAT}	Battery Voltage, - 48 V to the CLIC.
41	TRLY B	Test Relay driver output for Channel B. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
42	RLY B	Additional Relay driver output for Channel B. The output is Open-collector, with a Kick-back diode included, designed to be connected to a negative voltage.
43	NC	Not connected pin.
44	SCLK A	Control Clock for Channel A. Clocks data into the shift-register on high-to-low transitions (edge).
45	$\overline{CS}$A	Chip Select for Channel A. When low, Control data can be written into the control register
46	CI A	Control Data Input for Channel A. Serial Control data is clocked into the Control register from this pin
47	NC	Not Connected pin.
48	$\overline{DET}$ A	Detector output for Channel A. The output is a Open-collector with internal pull-up resistor to V_{CC}.
49	NC	Not connected pin.
50	NC	Not connected pin
51	NC	Not connected pin
52	FS A	Frame Sync for Channel A Transmit and Receive.
53	$\overline{DR}$ A	PCM Receive Data Input for Channel A.
54	MCLK A	Master Clock for Channel A.
55	DX A	PCM Transmit data Output for Channel A; Tri-state.
56	TSX A	Time Slot for Channel A; Open-drain. Output pulse low during encoding.

Functional Description and Applications Information

General

The PBA 3369/1 is a Dual Complete Line Interface Circuit. Only a small number of additional external components are required.

In case of a requirement for test of the subscriber line and system, two relays per line will be needed.

In figure 6 they are relay RL1, RL2, RL4 and RL5. One ring relay per channel will be needed to apply the ring signal to the subscriber line (RL3 and RL6).

Ring Trip

The ring trip function has been designed to the following conditions:

- Unbalanced ringing super-imposed on the battery voltage.
- Ring generator data:
  Output typical 75 V_{RMS}
  min 60 V_{RMS}, max 90 V_{RMS}
  Impedance min 20 Ω, max 40 Ω
  Frequency typ 25 ± 3 Hz
- Loop Resistance <1800 Ω
- On-hook impedance @ 25 Hz (Ringing signal) is 7,5 to 18 k Ω

One, two or three POT's (Plain Ordinary Telephone or equal) in parallell on each line.

In order to sense off-hook during ringing, two resistors per line is required; R_{RT} and R_{RG}.

They should be 240 Ω, min 2 W.

Note: R_{RT} and R_{RG} must fulfill CCITT k20. Lightning Surge.

The CLIC state during the pause of the ringing cadence shall be active due to longer stabilization time in stand-by state.

TTL or CMOS use

The integrated circuit of the interface are LSTTL or CMOS. CMOS use need specific attention during the board insertion under back panel power on condition.

Over Voltage Protection

The CLIC must be protected against surge voltages and power cross conditions.

In figure 6, the line resistors with fuse function, R_{F1} and R_{F2}, PTC:s, together with the voltage clamping device OVPD form the secondary protection. The PTC acts as a resettable fuse for non destructive power contact.

The protection network in figure 6 is designed to meet requirements in CCITT k20, Table 1.

If overvoltages with magnitudes higher than CCITT k20, Table 1, primary protection is required. A gas Discharge Tube is recommended.

Z_{BAT} protects against overvoltage on V_{BAT} and ensure that the OVP-device can trigger if -48 V should not be connected.

The capacitor C_G Between ground and the OVP-device should be as close as possible to the OVP-device.

The OVP-device ground should be connected as close as possible to the CLIC ground connector.

Grounding

The ”grounds”; GND’s shall be tied together as close as possible; i.e. in one point on the PCB.

The different ground points on the linecard shall also be connected together into one point.

GND should be distributed with a very low impedance as a ground plane or a grid in order to sink the overvoltage current with low voltage drops between the connectors of the components.

Power-up Sequence

The optimum power-up sequence, in order to avoid any problem, is: Ground, V_{BAT} (-48 V), V_{EE} (- 5 V) and V_{CC} (+ 5 V) in stated order.

If it is not possible to control the power-up sequence , the following design must be used:

1. **6,2 V Zener diode D_{VCC}, D_{VEE2}:**
   The zener diodes will protect all +5 V and -5 V IC´s on the linecard from overvoltage caused by Ground being connected after V_{CC}/V_{EE} and V_{BAT}.in the power-up sequence. This due to the voltage dividing between the decoupling capacitors on the line card.
2. **Schottky diode D_{VEE1}:**
   The schottky diode, with low forward voltage drop, will protect all -5 V IC’s on the linecard from reverse voltage if Ground is connected after V_{EE} and V_{BAT}.in the power-up sequence. This due to the voltage dividing between the decoupling capacitors on the line card.
3. **Resistor R_{VEE}:**
   The resistor will reduce the charging current into the decoupling capacitors and limit dV/dt.
4. **RC-network R_{BAT} and C_{BAT}:**
   To protect the V_{BAT} - pin from being exposed to a faster dV/dt - rate than 4 V / µs when connecting to V_{BAT}. This can be achieved by using a RC-filter with the time constant (t) formed by a 5,1 Ω resistor (R_{BAT}) and a 0,47 µF capacitor (C_{BAT}).

To ensure a fail-safe function in the system, it is recommended to use resistors with some type of fuse function and a Fuse on V_{CC} connection, in series with the power supplies to avoid resulting failures in the system.

Programmable Functions

Power-on

When power is first applied, power-on reset circuitry initializes the CLIC and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for “no output“, hybrid balance circuit turned off and in non-delayed timing mode.
The TIPX and RINGX terminals will present a high impedance state to the line and all relay drivers is put in off-state.

Power-down state

When, following a period of activity in the power-up state, a power-down instruction is sent into the serial control port as indicated in table 1, the DX output is set in high impedance condition. The coefficients stored in the Hybrid Balance circuit and the Gain control bits remain unchanged unless new data are written via the serial control port.
The operating state and the state of relay drivers will also remain unchanged. It is recommended that the CLIC is powered down before executing any instruction.

Serial control port

Control information and data are written into CLIC via the serial control port consisting of the control clock CCLK, the serial data input CI and the Chip Select input CS. All control instructions require 2 bytes, as listed in table 1, with the exception of a single byte power-up/down command.
To shift control data into CLIC, 8 transitions low to high must be present on CCLK while CS is low. Data on the CI input is shifted into the serial input register on the falling edge of each CCLK pulse.
After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS pulse or may follow the first continuously, i.e. it is not mandatory for CS to return high in between the first and second control bytes. On the falling edge of the 8th CCLK clock pulse in the 2nd control byte the data is loaded into the appropriate programmable register. CS may remain low continuously when programming successive registers, if desired. However CS shall be set high when no data transfers are in progress.

Function	Byte 1								Byte 2							
	7	6	5	4	3	2	1	0								
Single Byte Power-up/down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See table 2							
Write Latch Direction Register	P	0	0	1	0	0	1	X	1	1	1	1	1	1	0	0
Write Latch Content Register	P	0	0	0	1	0	1	X	See table 3 and 4							
Write Transmit Time-slot/port	P	1	0	1	0	0	1	X	See table 5							
Write Recieve Time-slot/port	P	1	0	0	1	0	1	X	See table 5							
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See table 6							
Write Receive Gain Register	P	0	1	0	0	0	1	X	See table 7							
Write Hybrid Balance Register 1	P	0	1	1	0	0	1	X	1	0	1	0	1	1	0	0
Write Hybrid Balance Register 2	P	0	1	1	1	0	1	X	1	0	0	1	0	1	0	0
Write Hybrid Balance Register 3	P	1	0	0	0	0	1	X	1	0	0	0	1	1	0	0

Notes: 1. Bit 7 of bytes 1 and 2 is alwoys the first bit clocked into CI pin.
2. “P“ is the power-up/down control bit, “0“ = Power up, “1“ = Power down.
X = Don’t care.

Master clock frequency selection

A Master clock must provided to the CLIC for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1,536 MHz, 1,544 MHz, 2,048 MHz or 4,096 MHz.
Bits F1 and F0 (see table 2) must be set during initialization to select the correct internal divider.
Bits MA and IA in table 2 permit the selection of μ255 coding or A-law coding with or without even-bit inversion.

Bit Number								Function
7	6	5	4	3	2	1	0	
F1	F0	MA	IA	DN	DL	AL	PP	
0	0							MCLK = 512 kHz
0	1							MCLK = 1,536 or 1,544 MHz
1	0							MCLK = 2,048 MHz*
1	1							MCLK = 4,096 MHz
		0 1 1	X 0 1					Select μ255 Law* A-law, including even bit inversion A-law, no even bit inversion
				0 1				Delayed Data Timing Non-delayed Data Timing*
					0	0		Normal Operation*
							0 1	Power Amp Enabled in PDN Power Amp Disabled in PDN*

* = State at power-on initialization (bit 4 = 0)

Interface latch directions

The interface latches which controls relay drivers and the SLIC operating states can be programmed as logic inputs or as logic outputs. Following a power-on, all latches assume that they are inputs. In this application all interface latches shall be programmed as logic outputs by sending hexcode FC (this must not be done until after the interface latch states has been programmed).

Interface latch states

Table 3: *Latch content register byte 2 functions.*

Bit #	Function	Low (0)	High (1)
7	SLIC C1 control input	See table 4	
6	SLIC C3 control input	See table 4	
5	SLIC C2 control input	See table 4	
4	Testrelay driver	Activated	Not activated
3	DET output selection	Loop current / ringtrip	Ground key
2	Relay driver	Activated	Not activated
1	None (don't care)		
0	None (don't care)		

Table 4: *Interface latches whitch controls the SLIC operating states. Bit # 7, 6, 5*

Bit #	7	6	5	Operating state	Conditions	Active Detector
	0	0	0	Open circuit		None
	1	0	0	Ringing, ring relay driver		Ring trip comparator
	0	1	0	Tip open		Loop current
	1	1	0	No function		
	0	0	1	Active	Bit 3 Low/High	Loop current/ground key
	1	0	1	Stand-by	Bit 3 Low/High	Loop current/ground key
	0	1	1	Active polarity reversal	Bit 3 Low/High	Loop current/ground key
	1	1	1	Stand-by polarity reversal	Bit 3 Low/High	Loop current/ground key

Time-slot assignment

PBA 3369/1 can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync input FS. Time-Slot Assignment may only be used with Delayed Data timing.

Table 5: *Byte 2 of Time-SLot and Port Assignment Instructions.*

Bit number								Function
7	6	5	4	3	2	1	0	
0	X	X	X	X	X	X	X	Disable DX output (transmit instruction)* Disable DR input (receive instruction)*
1	0	Assign One Binary Coded Time-Slot from Time-Slot 0 to Time-Slot 63						Enable DX Output (transmit instruction) Enable DR Input (receive instruction

** = State at power-on inialization*

Transmit gain

The transmit gain can be programmed in 0,1 dB steps by writing to the Transmit Gain Register as defined in table 1 and 6.

Table 6: *Byte 2 of Transmit Gain Instructions*

Bit Number								Dec no	Hex code	Transmit Gain Absolute
7	6	5	4	3	2	1	0			
0	0	0	0	0	0	0	0	0	00	No output *
1	1	1	0	1	0	0	0	232	E8	-3,5 dB
1	1	0	0	0	1	0	1	197	C5	0 dB

** = State at power-on initialization*

For every increase with 1 the actual gain will decrease with 0,1 dB.
The decimal number of 197 equals 0 dB Absolute Gain.

The decimal number of 207 equals 0 - 0,1 • 10 = - 1,0 dB Absolute Gain.

Receive gain

The receive gain can be programmed in 0,1 dB steps by writing to the Receive Gain Register as defined in table 1 and 7.

Table 7: *Byte 2 of Receive Gain Instructions*

Bit Number								Dec no	Hex code	Receive Gain Absolute
7	6	5	4	3	2	1	0			
0	0	0	0	0	0	0	0	0	00	No output *
1	0	1	1	0	0	1	1	178	B2	-7 dB
1	1	0	1	0	1	1	0	213	D5	-3,5 dB
1	1	1	1	1	0	0	1	248	F8	0 dB

** = State at power-on initialization*

For every decrease with 1 the actual gain will decrease with 0,1 dB.

The decimal number of 248 equals 0 dB Absolute Gain.

The decimal number of 238 equals 0 - 0,1 • 10 = - 1,0 dB Absolute Gain.

Example of programmable functions

Example: Hex code 82A98A3492FCD280CA80AAC5A2F8B2ACBA94C28C00

Hex code	Byte 1	Byte 2	Function
82A9	1 0 0 0 0 0 1 0	1 0 1 0 1 0 0 1	MCLK=2,048MHz A-law incl. Even Bit Inversion Non-delayed data timing Normal operation Power Amp disabled in PDN
8A34	1 0 0 0 1 0 1 0	0 0 1 1 0 1 0 0	Active state No relaydrivers active Loop current detector
92FC	1 0 0 0 1 0 1 0	1 1 1 1 1 1 0 0	All interface latches are set to outputs*
D280	1 1 0 1 0 0 1 0	1 0 0 0 0 0 0 0	DX enabled
CA80	1 1 0 0 1 0 1 0	1 0 0 0 0 0 0 0	DR enabled
AAC5	1 0 1 0 1 0 1 0	1 1 0 0 0 1 0 1	Transmit Gain = 0dB
A2F8	1 0 1 0 0 0 1 0	1 1 1 1 1 0 0 1	Recieve Gain = 0dB
B2AC	1 0 1 1 0 0 1 0	1 0 1 0 1 1 0 0	Programming hybrid balance
BA94	1 0 1 1 1 0 1 0	1 0 0 1 0 1 0 0	filter for best TBRL performance
C28C	1 1 0 0 0 0 1 0	1 0 0 0 1 1 0 0	
00	0 0 0 0 0 0 0 0	None	Power-up

* *In this example, if this is the first programming after power-on, the CLIC will be put in active state directly when 92FC has been sent.*

Application Reference Figures

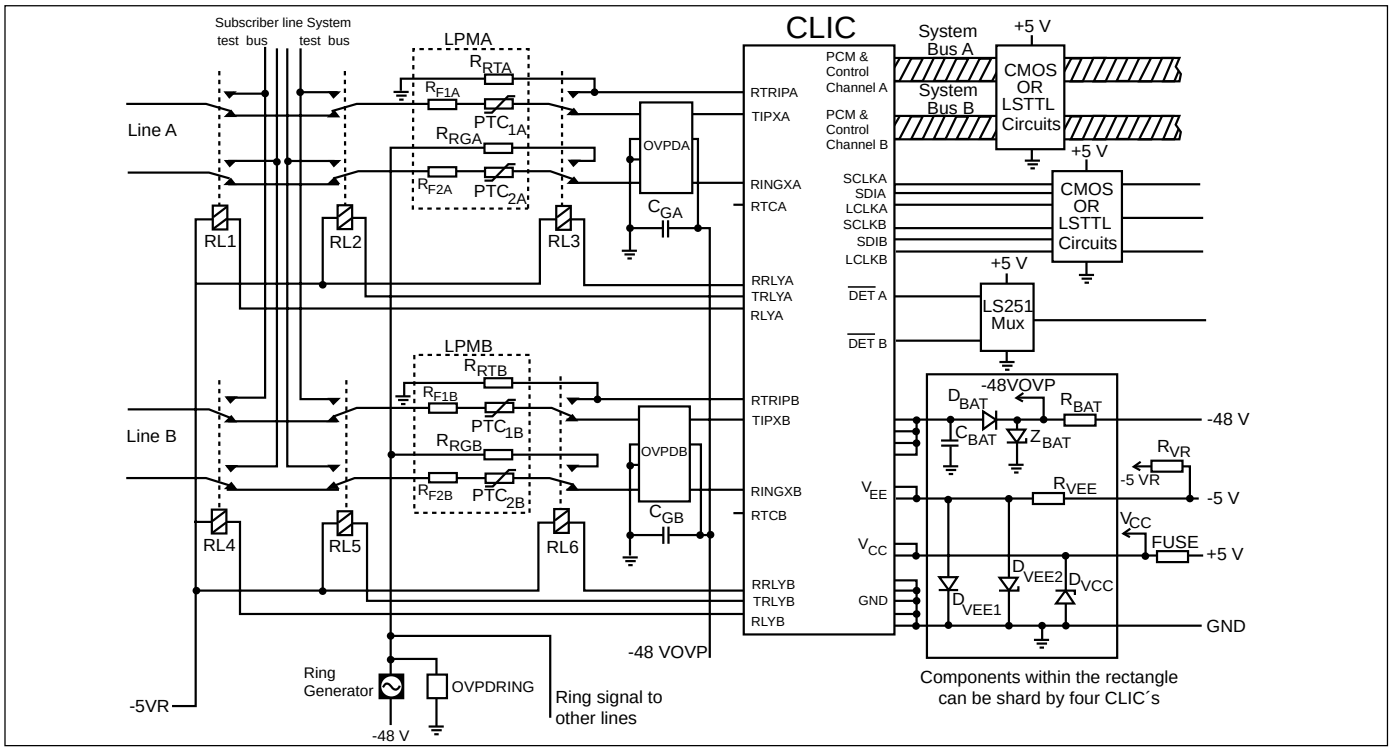

Figure 6: Typical Application for Dual CLIC PBA 3369/1 on a 16 Lines Line Card

Denotation	Type of Component; Requirements, name etc
OVPDA, OVPDB	TISP61CAP3
OVPDRING	Transient supressor, Zener diode type, 200 V
D_{VCC}, D_{VEE2}	Zener diode 6,2V 1W; BZX85C6V2
D_{VEE1}	Schottky diode 1N5818, 1N5820
D_{BAT}	Diode 1N4004 or similar
Z_{BAT}	Transient supressor, BZW04-58 or SA58A
RL1-RL6	Relay; 9 V type
LPMA, LPMB	PBR 522 01/1 2 • 40 Ω, matched, Line Resistor with PTC and two 240 Ω resistor.
R_{VEE}, R_{VR}	1,0 Ω, ± 20 %, 1 Ω (with fuse function)
R_{BAT}	5,1 Ω, ± 20 %, 1 Ω (with fuse function, max 4 dual CLIC's)
C_{BAT}	0,47 µF, ± 20 %, 100 V. Recommended types: 1. Ceramic, X7R, with low voltage coefficient; max 15 % at 50 V_{DC} 2. Metallized polyester film (stacked MKT); Prefered
C_{GA}, C_{GB}	0,22 µF ± 20 %, 100 V. Recommended types: see C_{BAT}
Fuse	Fuse ≥ 1A depending on the power supply current in the interface circuits.

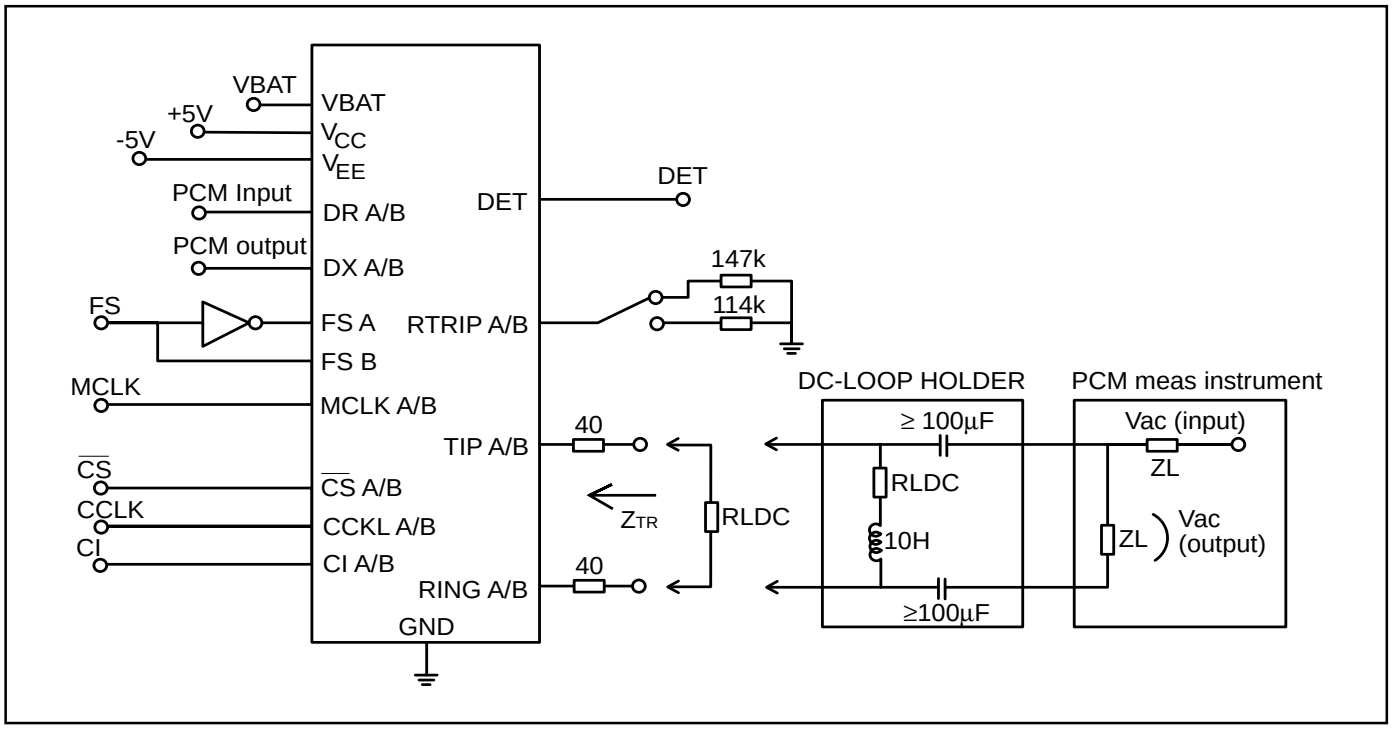

Figure 7. Reference diagram for Transmission Measurement.

Mechanical Outline

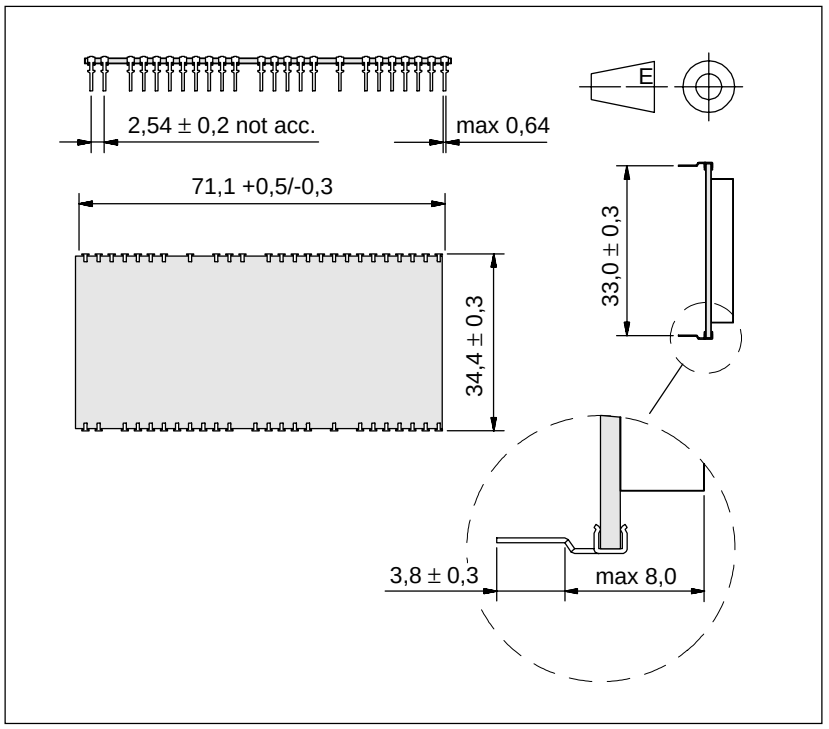

Figure 8. Mechanical outline.

1522-PBA 3357/3 Uen Rev. A

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