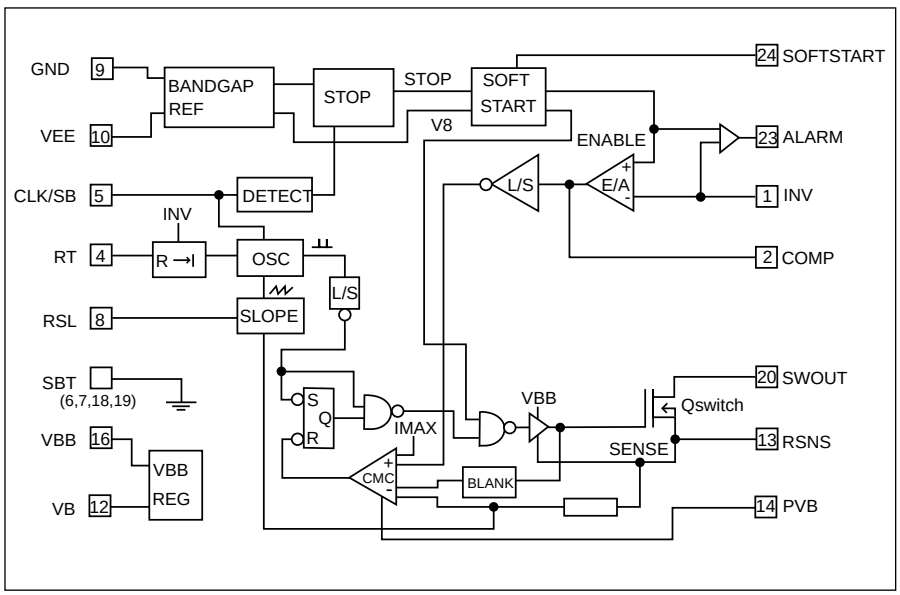
PBK 203 02
Telecom switched mode power supply regulator

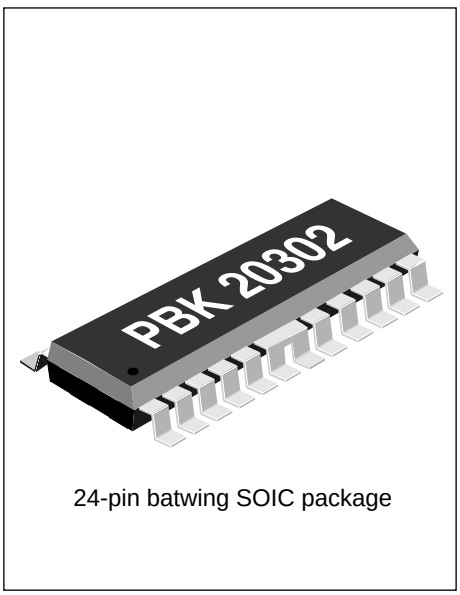
Description

PBK 203 02 is a monolithic control circuit intended for unisolated buck-mode (step-down) DC/DC-converters. It works directly of a high voltage power supply (-38V to -80V) making it ideal for use in telecom line-card applications. It includes all necessary functions to achieve a high performance solution with a minimum of external components. PBK 203 02 includes a N-channel power-DMOSFET switch.

Key Features

- Current mode control with internal slope compensation
- External programmed softstart/ softstopp
- Internal power-DMOS as switch
- Over temperature protection (OTP)
- Under voltage lockout (UVL)
- Alarm output for OTP and current limit





24-pin batwing SOIC package

Figure 1. Block diagram.

Maximum Ratings

Parameter	Pin No.*	Symbol	Min	Max	Unit
Voltage					
Input supply voltage	12	VB	-80		V
Digital inputs voltage	5	VS	0	6,5	V
Digital output pull-up voltage	23	VA	0	6,5	V
Digital output sink current		I_A	300		uA
Error amplifier input			-9	0	V
Error amplifier max output current			-1	1	mA
Output driver currents					
peak				2	A
continuos				0,8	A
Storage temperature			-55	+150	°C
Junction temperature			-35	+150	°C

Recommended Operating Conditions

Parameter	Pin No.*	Symbol	Min	Max	Unit
Temperature range			-35	+130	°C
Oscillator frequency			100	600	kHz
Frequency programming resistor		RT	70	300	kΩ
Current sense resistor			0,39		Ω

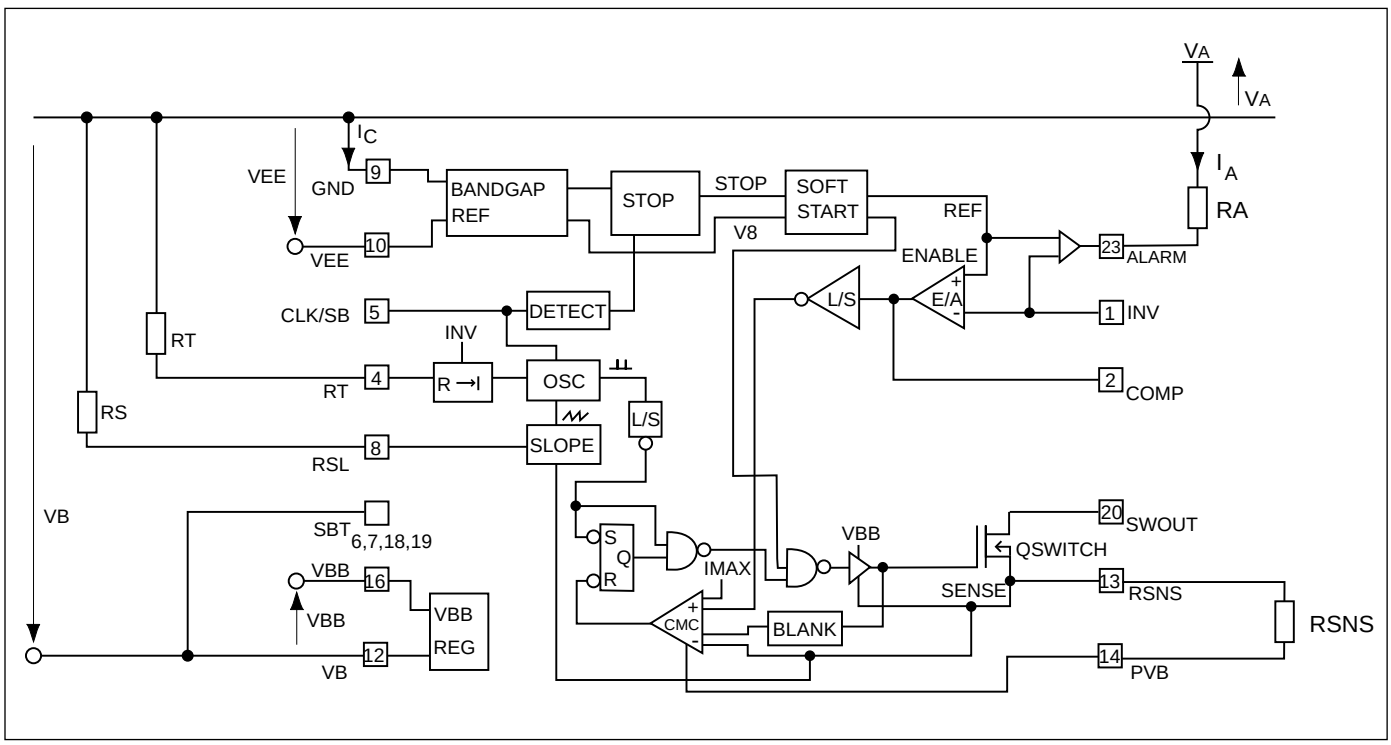


Figure 2. Definition of symbols

Electrical Characteristics

Electrical characterstics over recommended operating conditions, unless otherwise noted -20°C, CT: ≤ 125°C

Parameter	Pin No.*	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage (VB)	12	VB		-80		-38	V
Supply Current							
Ic		I_C		2	2,5	3	mA
Ic-standbye				0,2	0,35	0,5	mA
Voltage Reference							
VEE T=25°C	10	VEE		-11,22	-11,0	-10,78	V
VEE				-11,33	-11,0	-10,67	V
VBB	16	VBB		8	10	12	V*
VEE- Short circuit current				3		10	mA
VBB-short circuit current				3		10	mA
* measured with respect to VB							
Under voltage lockout							
Stop Threshold				-35		-29	V
Hysteresis				1,5		4	V
Over temperature protection							
Stop Threshold				130		150	°C
Hysteresis				10		30	°C
Softstart							
Power-on-delay				0,2	0,6	2	ms
Start/ Stopp -time			CSOFT=2nF		3,8		ms
Standby delay at 500 kHz				5		7	us
Oscillator section							
Initial frequency, Fi			RT=90kOhm	450	500	550	kHz
Temperature stability			RT=90kOhm	-3		+3	%
SYNK/SB logic ‘0’				0		1,5	V
SYNK/SB logic ‘1’		VS		2,0		6,5	V
SYNK/SB Pin impedance				20		40	kΩ
Synk-area related to Fi				102		135	%
Slope compensation							
slope amplitude (p-p)			RS=18kOhm		320		mV
slope duty cycle				85		95	%

Electrical Characteristics

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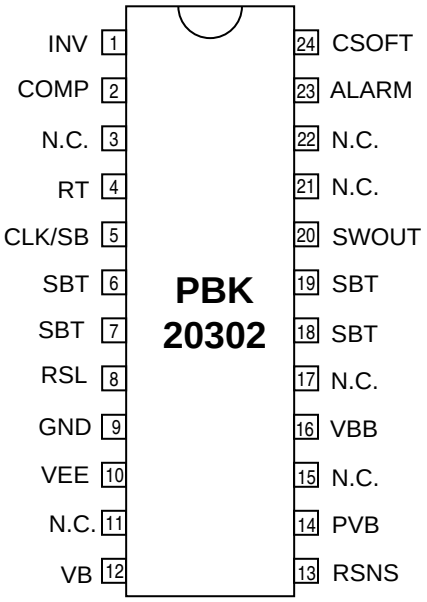
Parameter	Pin No.*	Symbol	Conditions	Min	Typ	Max	Unit
Comparator section							
Delay RSNS to SWOUT				200		240	ns
Blanking time				40		100	ns
Error amplifier							
Open Loop Gain					85		dB
Bandwidth				800	1000	1300	kHz
Input common mode range					0	-9	V
Output range					-9,5	-8	V
Max output current					-1	1	mA
INV startpoint for frequency decrease	1	INV		-5,1		-4,9	V
Frequency decrease rate (% of Fi/INV)				20	25	30	%/V
Max frequency decrease (% of Fi)					20		%
Offset (including softstart error)				-25		+25	mV
Alarm							
Current limit alarm level (INV rel V8)				-4		-12	%
Sink current					0,5		mA
Logic low voltage (Ia=0,5mA)				0		1	V
Pull-up voltage		VA				6,5	V
Power DMOSFET							
Switch-fet RON			T=27°C	0,7	0,9	1,2	Ohm
Switch-fet RON				0,5		2,0	Ohm

Thermal Charactenstics

Parameter	Pin No.*	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance			24 SOIC BW		13	K/W	
Power losses			24 SOIC BW		1,5	W	



Pin description

SO	Symbol	Description
1	INV	Inverted input to error amplifier. The error amplifier has a bandwidth of typical 1MHz.The non-inverted input is internally connected to a reference voltage. The reference voltage is at softstart decreased from 0V to -8V. The slope length TSOFT depens on the external capacitor CSOFT, TSOFT(ms) = 1,6 x CSOFT(nF)
2	COMP	This is the output of the error amplifier as well as input to the current mode PMW-comparator. The level at COMP sets the peak output current from the switch . Connect a RC-link between COMP and INV to set the regulator loop compensation. The normal output range at COMP is -8V to -9V.
3	N.C.	
4	RT	The oscillator uses an internal capacitance and an external resistor to set the regulator switching frequency. The external resistor is connected between RT and GND and sets the frequency according to the following equation: f(kHz)=45000/RT(kOhm). Recommended operating frequency is maximum 600kHz.
5	CLK / SB	The oscillator can be synchronised with an external digital signal. TTL or 3V-logic levels can be used (referred to GND). The frequency can only be increased, not decreased. Oscillator will lock on down-going flank. When the regulator is in current limit operation the synchronisation is disabled. The regulator is free running when CLK/SB is connected to GND. The regulator is set to standby mode if CLK/SB is connected to a Logic high level (+3V to +6,5V).
6,7	SBT	SBT shall be connected to VB.
8	RSL	Slope compensation is needed to prevent instability when duty cycle is above 50%. Slope compensation is added to the sensed current signal. The amount of slope compensation is programmed with an external resistor between RS and GND. The slope length is 90% of the oscillator period. The slope peak to peak value is set according to the following equation: Uslope(V) = 9 / RS (KΩ).
9	GND	All voltages are measured with respect to GND.

Pin description

SO	Symbol	Description
10	VEE	The control circuit includes a linear regulator for internal power supply of the circuit. This voltage is accessible at VEE and should be bypassed to GND with a ceramic low ESL capacitor. VEE = -11V. VEE is generated with a bandgap reference and has an accuracy of +/- 3%. VEE can be externally loaded with maximum 1mA. The internal reference voltage to the error amplifier is derived directly from VEE (via softstart)
11	N.C.	
12	VB	The power supply - battery voltage - is connected to VB. VB should be bypassed to GND with a ceramic, low ESL capacitor. The maximum battery voltage is -80V. At voltages bellow -35V the under voltage lockout will disable the driver to the DMOSFET resulting in a high impedance output at SWOUT.
13	RSNS	A current sense resistor should be connected between RSNS and PVB. Maximum current is programmed with the value of the resistor. The internal current limit level is set to 0,5V measured at RSNS with respect to PVB.
14	PVB	Power supply connection to power switch. PVB should be connected via an inductor to VB.
15	N.C.	
16	VBB	The power to the DMOSFET driver is supplied from VBB. VBB is approximately 10V above VB. VBB should be bypassed to VB with a ceramic, low ESL capacitor.
17	N.C.	
18,19	SBT	SBT shall be connected to VB.
20	SWOUT	Switching power output. Recommended output current is up to 800mA.
21,22	N.C.	
23	ALARM	To use the alarm output a pull-up resistor should be connected from ALARM to a logic level power supply (3V to 6,5V). ALARM is forced low if the over temperature protection (OTP) is activated or if the regulator works in the current limit mode. The OTP is activated if chip temperature is above 130°C and it has an hysteresis of minimum 10 °C.
24	CSOFT	An external softstart/softstopp capacitor shall be connected between CSOFT and GND. The start/stopp time is set according to the following equation: TSOFT (ms) = 1,6 CSOFT (nF) Softstopp is activated only with the SB signal. At softstopp the output voltage is decreased from nominal voltage to near zero voltage. At an output voltage <4% of nominal output voltage the output drive are disabled.

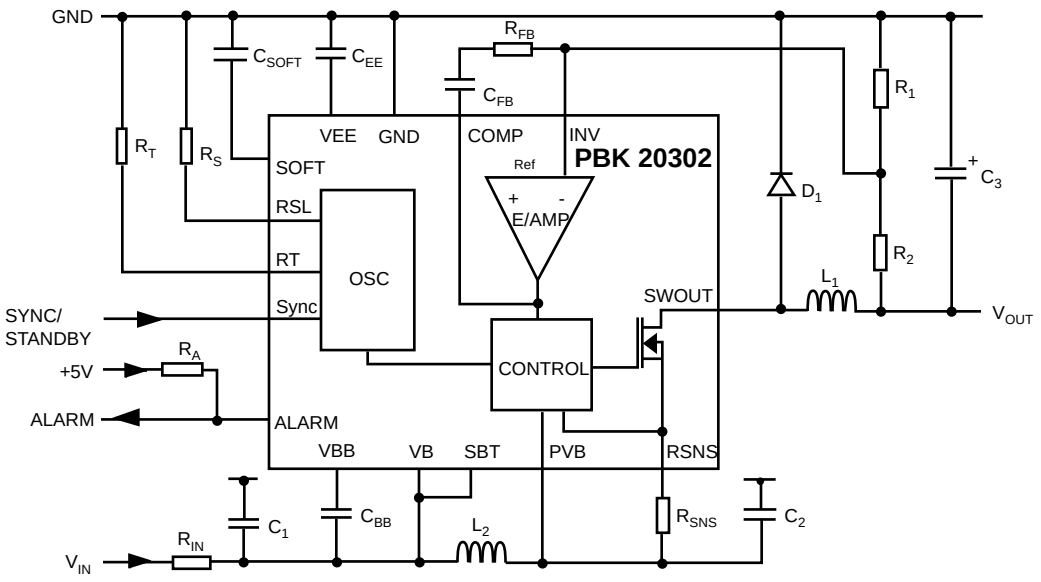
Applications information

Parameters you can control in your application.

- Output voltage by the equation $V_{out} = 8 \times \frac{R_1 + R_2}{R_1}$
- Max output current by the equation $I_{OUTMAX}\ (A) = \frac{-7}{8} \times R_{SNS}\ (\Omega) + 1.$
- The switch frequency by the equation $F\ (kHz) = \frac{45000}{R_T(k\Omega)}$
- The loop amplification, which is $Loop_{Amp} = \frac{R_{FB}}{R_1 \,||\, R_2}$, recommended to be 0.5
- The soft start and stop, which is set by the eqation $T_{Soft}(ms) = 1.6 \times C_{SOFT}\ (nF)$
- The slope compensation resistor Rs by the equation $R_S = \frac{1}{23} \times \frac{V_{out}}{L_1}$

Example of a -48V / -28V step down converter.

Input Voltage (V_{IN})	-38V .. -72V
Output voltage (V_{OUT})	-28 V
Output voltage accuracy	<+/- 2V
Output voltage ripple	<90 mV rms
Induced ripple on power supply	<10mV rms
Output impedance	< 10 Ω
Max Output current	700 mA
Min Output current	7 mA
PSRR	40dB (0-20 kHz)
Clock frequency	490 kHz
Soft start time	3,5ms



R_1 = 100 kΩ	0.2%	C_3= 47µF	50V, elyt
R_2 = 250kΩ	0.2%	C_{SOFT} = 2,2nF	50V, ker
R_T = 90kΩ		C_{FB} = 10 nF	
R_S = 18kΩ		C_{BB} = 100nF	50V, ker
R_{FB} = 30kΩ		C_{EE} = 100nF	50V, ker
R_A = 20kΩ		L_1 = 68µH	910 mA
R_{IN} = 4.7Ω		L_2 = 10µH	1000mA
R_{SNS} = 0.39Ω		D_1 = 1A	70V, schottky
C_1= 470nF	50V, ker		
C_2=680nF	100V, ker		

Figure 4. Typical step-down converter application.

Functional description

PBK 20302 is a current mode regulator with fixed frequency. It has good load transient response and automatic feed-forward compensation. Slope compensation, necessary for operation with duty cycle >50%, is provided by an internal slope compensation circuit that is programmed with an external resistor. Current mode control makes it possible to current limit the regulator pulse by pulse. A blanking circuit disables the current mode comparator for the leading edge of the current sense signal. This eliminates the need for an external current sense filter. Minimum on-time is limited by the blanking time and propagation delay from the current mode comparator to SWOUT and is approximately 200ns. The characteristics of the current limit is improved by a decrease in switching frequency when the regulator is short circuited.

The decrease in switching frequency starts when output voltage is 5/8 of nominal value. It decreases linear to nominal frequency divided by of 4 when output voltage reaches 15% nominal output voltage. This prevents the output current to raise uncontrollable when the output is short circuid. Switching frequencies up to 600kHz is possible. Duty cycle on the switch DMOSFET is maximised to 90%.

The regulator includes an Over Temperature Protection (OTP) with hysteresis . An Under Voltage Lockout (UVL) shuts of the regulator when the input voltage is below 35V. The synchronise input to the oscillator can be used to set the regulator in a standby (SB) mode. The OTP can be monitored at the ALARM output from the regulator. The ALARM output also indicate if the regulator works in current limit. When OTP, UVL and SB is true the driver to the switch and are disabled and softstart is reset. When OTP, UVL and SB turns false softstart is performed after a delay of approx. 1 ms. The softstart ramps the reference voltage to the error amplifier with a slope that depend on the external capacitor CSOFT. When the requlator is set to standby mode the reference voltage decrease with the same slope.The drivers to the switch is then disabled when the reference to the error amplifier is below -0,3V.

The error amplifier has high impedance inputs. The bandwith is typical 1 MHz. The output and INV input is accesible for loop compensation. The output is level-shifted /inverted to the current mode comparator.

Specifications subject to change without notice.

1522-PBK 203 02 Uen Rev. A

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