PBL 3755
PCM-Repeater

Description

The PBL 3755 is a bipolar integrated circuit that contains all the necessary functions to form a regenerative repeater for Pulse Code Modulated (PCM) telecommunications systems. The circuit is designed to operate at 2.048 Mbps CEPT lines with HDB3 code as well as at 1.544 Mbps T1 American standard PCM lines. PBL 3755 can also be used in line terminating equipment (S1 to D1 station repeaters) and as a T1 line receiver.

The circuit operates with a single 5.25 V supply, which allows a compact design due to low power dissipation. With a typical supply current of only 8 mA for each PBL 3755. Other features, such as error detection and fault location can also be powered from a 48 mA line. A built-in stabilized DC-regulator eliminates the need for an external power supply or biasing components.

The PBL 3755 has a double Automatic Line Build Out (ALBO) section, which together with a high performance pre-amplifier gives an ALBO gain range of 45 dB or more. Automatic equalization for the whole range from 0 dB is possible.

The clock regenerator gives a well defined and accurate sampling time without external components for delay generation. Its operation is stable and independent of the specific frequency.

Internally protected inputs and outputs reduce the need for external overvoltage protection components. The supply pins can withstand the triggering voltage of an inexpensive thyristor diode.

Key Features

- Low voltage operation
- Low current consumption
- On-chip power supply
- Over-voltage protection
- High-gain wide-band amplifier
- Double ALBO section
- Fully integrated clock regenerator
- Output stages suitable for transformer load
- Output-disable for power-up and loss of signal
- Buffered output for trimming of LC-tank

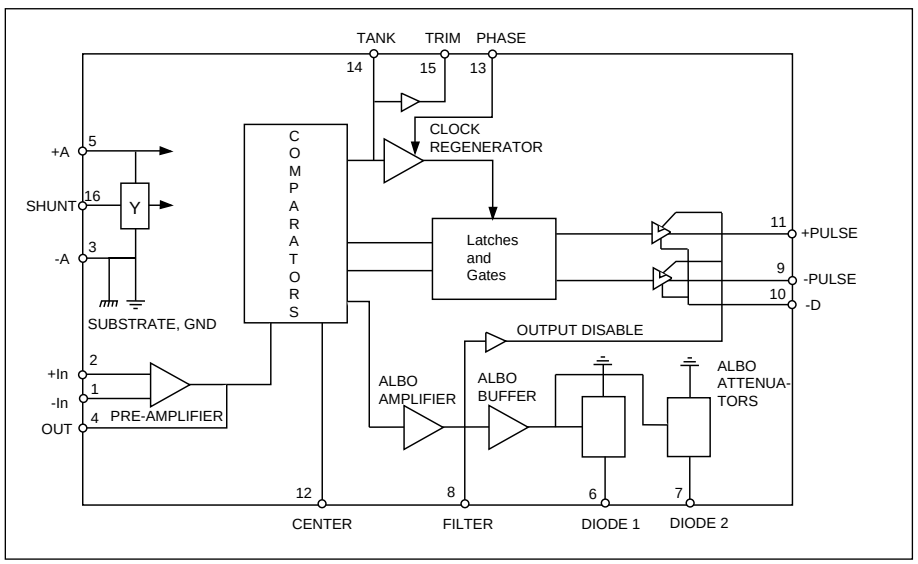
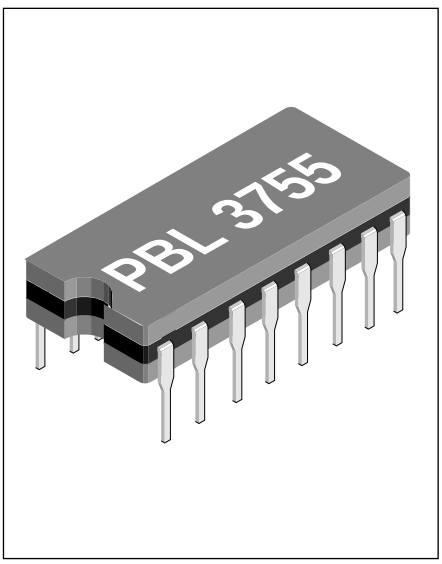


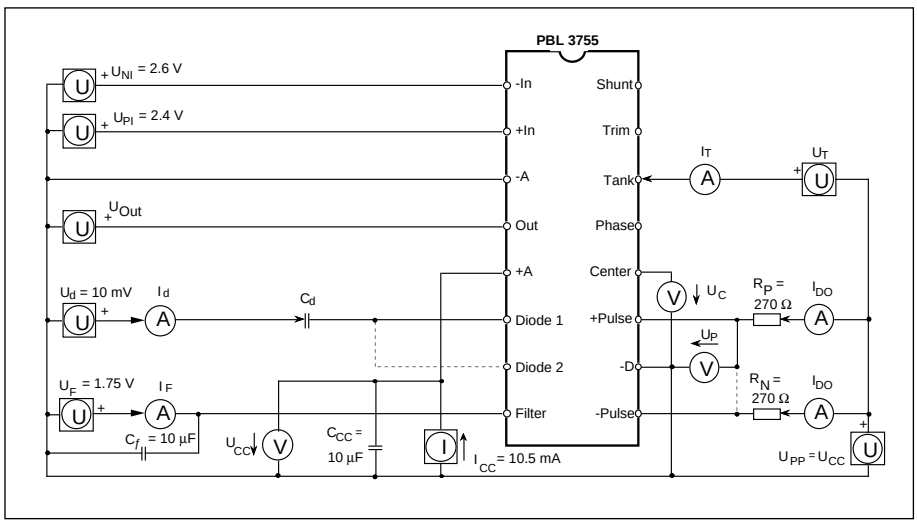
Figure 1. Block diagram.



Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	-40	70	°C
Temperature, storage and shipping	T_{Stg}	-65	150	°C
Power dissipation (T_{Amb} = 70 °C, Note 2)	P_D		1	W
Supply voltage, continuous (see figure 3)	U_{CC}	-1.0	10.0	V
Supply voltage, half-wave (f = 50 Hz, t= 0.5 s) (see figure 3)	u_{CCP}	-2.5	25.0	V
Output voltage, continuous	U_{DD}	-1.0	15.0	V
Output voltage, single pulse (t=2 µs)	u_{DDP}	-5.0	17.0	V

Note 1: The permissible power dissipates linearly, passing 1 W at 70 °C and 0 W at 150 °C. For low temperatures maximum U_{CC} limits power. For normal constant current feed neither will be violated, but note that characteristics are guaranteed only for steady state operation at conditions stated therein.



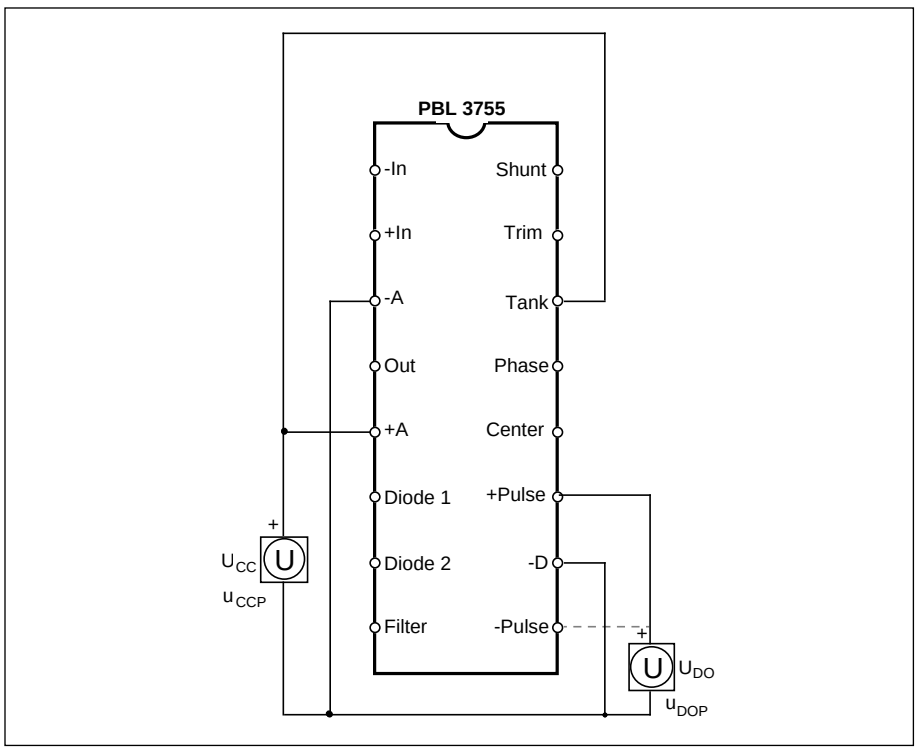


Figure 3. Test circuit for over-voltage stress.

Figure 2. Test circuit for threshold measurements.

U_{CC} as a function of I_{CC} must be measured when both outputs are activated with a +1, -1, +1 .... -sequence PCM-signal.

C_f lets U_F be open circuit during Z_{On} and Z_{Off} tests.

$$C_d >> \frac{1}{2\pi f \, |\min(Z_{On})|}$$

$$Z_{On} = \frac{U_d}{I_d}, U_{Out} = U_C + \frac{\max(U_{TPP})}{2}, U_F : I_F = 0$$

$$Z_{Off} = \frac{U_d}{I_d}, U_{Out} = U_C, U_F : I_F = 0$$

U_{TPP} is defined for a dynamic cosine-shaped signal. In a static measurement it must be compensated to yield correct thresholds:

$$U_1 = U_{Out} : I_F = 0 \; ; \; U_2 = U_{Out} : I_F = 0$$

$$U_{TPP} = U_1 - U_2 + 2 \cdot 86.17086 \cdot \frac{(T_a + 273.15\ K)}{10^6} \cdot \ln(5.677)$$

$$U_{TD} = \frac{(U_{Out} - U_C)}{U_{TPP}/2} :$$

Signal from +Pulse or -Pulse appears after U_T has been clocked from +1V to -1V.

$$I_T = I_T(U_T, U_{Out})$$

$$U_{TC} = \frac{(U_{Out} - U_C)}{U_{TPP} / 2} : I_T = I_T(0, U_C) + 0.5\, I_{Tank}$$

$$Z_{Tank} = \frac{4}{Y_{Tank}(+) + 2\, Y_{Tank}(0) + Y_{Tank}(-)}$$

$$Y_{Tank}(+) = \frac{I_T(0.5\ V, U_C + 0.9\, U_{TPP}/2) - I_T(-0.5\ V, U_C + 0.9\, U_{TPP}/2)}{0.5\ V - (0.5\ V)}$$

$$Y_{Tank}(0) = \frac{I_T(0.5\ V, U_C) - I_T(-0.5\ V, U_C)}{0.5\ V - (0.5\ V)}$$

$$Y_{Tank}(-) = \frac{I_T(0.5\ V, U_C - 0.9\, U_{TPP}/2) - I_T(-0.5\ V, U_C - 0.9\, U_{TPP}/2)}{0.5\ V - (-0.5\ V)}$$

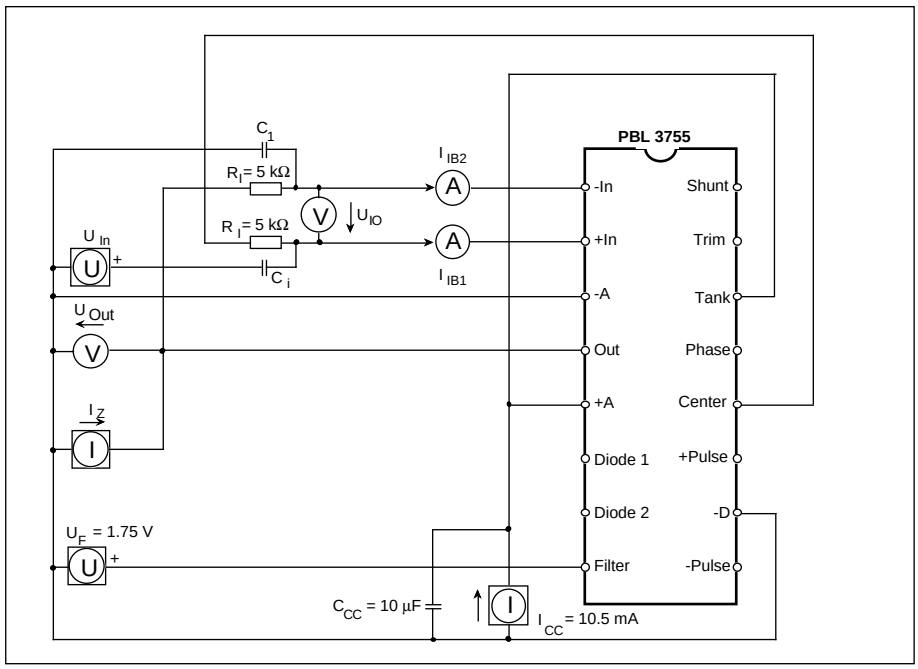
$$I_{Tank} = \frac{I_T(0, U_C + 0.9\, U_{TPP}/2) + I_T(0, U_C - 0.9\, U_{TPP}/2)}{2} - I_T(0, U_C)$$

Electrical Characteristics

Applicable for T_{Amb} = -40°C to 70°C, I_{CC} = 10.5 to 50.0 mA

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Supply voltages regulator						
Supply voltages, U_{CC}	2		5.00	5.25	5.50	V
Pre-amplifier						
Input offset voltage, U_{IO}	4			0	15	mV
Input offset current, I_{IO}	4			0	2	µA
Input bias current, I_{IB}	4			0.4	4	µA
Voltage gain, A_{V0}	4	5 kΩ load, f = 10 kHz	55	60	65	dB
Voltage gain,A_{V1}	4	5 kΩ load, f = 1 MHz	49	59		dB
Voltage gain,A_{V2}	4	5 kΩ load, f = 25 MHz	22	37		dB
Phase lag	4	5 kΩ load, f = 25 MHz		155	165	°
Input impedance,Z_{In}	4	f = 10 kHz	20	5000		kΩ
Output impedance,Z_{Out}		f = 10 kHz		100	150	Ω

Figure 4. Test circuit for amplifier measurements.



$$I_{I0} = I_{IB1} - I_{IB2}$$

$$I_{IB} = \frac{I_{IB1} + I_{IB2}}{2}$$

$$A_{vd} = 20 \log \frac{U_{Out}}{U_{In}}$$

$$\phi = \arg \frac{U_{Out}}{U_{In}}$$

$$Z_{In} = \frac{U_{Out}}{I_{In}} \quad I_z = 0$$

$$Z_{Out} = \frac{U_{Out}}{I_z} \quad U_{In} = 0, \; |I_Z| < 100\ \mu A$$

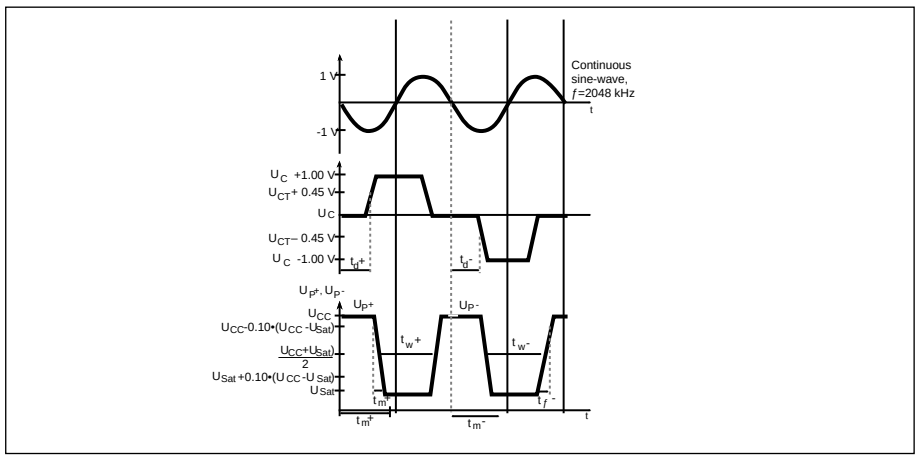
$$C_i >> \frac{1}{2\pi f R_1}, \; C_1 >> \frac{A+1}{2\pi f R_1}, \; A \approx 1000$$

Figure 5. Waveforms, test circuit as in figure 2.

$t_s = t_d$: The first signal appears on -Pulse or -Pulse when t_d is slowly adjusted from 102 ns towards 142 ns.

$|\Delta_{two}| = |t_w (U_T = 2\ V \text{ peak to peak}) - t_w (U_T = 0.4\ V \text{ peak to peak})|$

$|\Delta_{tw1}| = |t_w(+) - t_w(-)|$



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
ALBO regulation						
Impedance, ALBO on i.e. minimum cable length, Z_{On}	2	f = 10 kHz		25	40	Ω
Impedance, ALBO off i.e. maximum cable length, Z_{Off}	2	f = 10 kHz	20	1000		kΩ
ALBO threshold voltage peak to peak for sine-wave, U_{TPP}	2		1.8	2.0	2.2	V
Comparators						
Data threshold relative to ALBO threshold ($U_{TPP/2}$), U_{TD}	2		42	45	48	%
Clock threshold relative to ALBO threshold ($U_{TPP/2}$), U_{TC}	2		65	70	75	%
Pulse current on Tank, I_{Tank}	2		85	100	115	µA
Clock regenerator						
Impedance shunting tank, Z_{Tank}	2	f = 0	100	700		kΩ
Sampling instant, t_s	5	f = 2.048 MHz	102	122	142	ns
Pulse-width variation on change of amplitude in the tank, $\|\Delta t_{wo}\|$	5	f = 2.048 MHz			20	ns
Trim output when tank voltage is applied, $\|\Delta U_{Tr}\|$	6		0.5			V
Output stages						
Saturation voltage, U_{Sat}	6	I_{Sat} = 15 mA	0.365	0.475	0.660	V
Imbalance in U_{Sat} between channels, $\|\Delta U_{Sat}\|$	6				0.20	V
Output leakage current when off, I_{DO}	2	$U_{DO} = U_{CC}$		1	100	µA
Pulse-width of output, t_w	5	f = 2.048 MHz	220	244	268	ns
Rise-time of output, t_r	5	f = 2.048 MHz		40	60	ns
Fall-time of output, t_f	5	f = 2.048 MHz		40	60	ns
Imbalance in t_w between channels, $\|\Delta t_{w1}\|$	5				12	ns

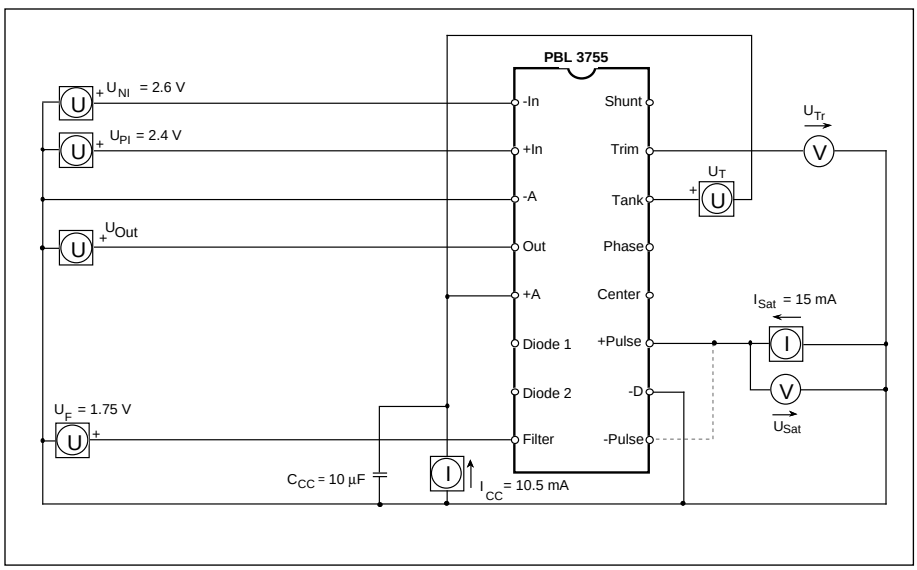


Figure 6. Test circuit for output saturation and trim output measurement.

$|\Delta U_{Sat}| = |U_{Sat}(+) - U_{Sat}(-)|$

$|\Delta U_{Tr}| = |U_{Tr}(U_T = 2\ V_{Peak\text{-}to\text{-}peak}) -$

$- U_{Tr}(U_T = 0.4\ V_{Peak\text{-}to\text{-}peak})|$

Pin Descriptions

Refer to figure 7 (22-pin dual-in-line package).

Pin	Symbol	Description
1	-In	Inverting input of the preamplifier. Driven from the detection point (pin 4) by the equalizer network, which provides full DC feedback. The load on the passive network is negligible.
2	+In	Non-inverting input of the preamplifier, which is an operational amplifier although with limited common-mode range. This pin is fed from the ALBO network with the pre-equalized and attenuated line signal. The load on the ALBO network is negligible.
3	-A	Analog ground. Negative supply for everything except the output drivers. Substrate connection which works as a shield for the preamplifier. Excessive supply current is also grounded here by the shunt.
4	Out	Preamplifier output. Detection point. Driving capability for R_{10} of the feedback network.
5	+A	(DC-supply) Positive supply for all parts of PBL 3755. Protected for over-voltage during remaining transient induced by lightning or mains short. It is just as important as signal ground as pin 3 is. C_{20} should be placed near these pins, if possible, by splitting it in one for each PBL 3755 and a major one together with the supply protection, D_1 and S_1.
6 7	Diode 1 Diode 2	Matched variable resistance elements used as active elements in the ALBO network. Can be directly connected to each other if only one ALBO section is used. To avoid distortion and varying bias for the amplifier the signal must be coupled with capacitors C_9 and C_6.
8	Filter	Output of the current amplifier controlling the ALBO diode current. Input to the output disable transistors with a threshold of ca 1.2 V. C_{16} is a smoothing capacitor for the rectified peak detector signals. It provides AC ground for the ALBO diodes and ensures that the Pulse outputs (pins 9 and 11) are disabled during the first fraction of a second after power has been switched on. It also determines the time after loss of input signal when the outputs are disabled. The bleeding resistor for this is built in, and is on the order of 200 kΩ.
9 11	-Pulse +Pulse	Outputs from the line driver stages. Basically it is a Schottky-clamped open-collector output, but it has a Miller-type feedback capacitor which determines the rise- and fall times. They are also provided with protection networks, which keep currents within a safe operating area for the grounded-emitter output transistors as long as voltages are kept within the limits given under Maximum ratings.
10	-D	Digital ground. Emitters of the output transistors and negative supply for their driver stages. This pin allows the high pulse currents in the output transformers to be grounded near the supply smoothing capacitor, C_{20}. -D is intended to be connected to analog ground, -A, (pin 3), but a small differential voltage will not interfere with any internal function.
12	Center	Bias output to the preamplifier. This is a buffered tap on the threshold-voltage generator, which defines the reference for all detectors.
13	Phase	Normally this possibility of fine-adjusting the sampling time (ts) will not be needed and should be left unconnected.
14	Tank	Output of pumping current from the clock detectors. Input of the clock regenerator, which is referenced to +A (pin 5). The resistive and capacitive load of the LC-tank is negligible, but a small bias, 60 μA, is present.
15	Trim	(Monitor). Output from a peak rectifier and buffer with smoothing, connected to pin 14. Thus, a simple voltmeter can be used to monitor the amplitude of the tank when trimming its resonant frequency. This saves either a FET-probe, an additional winding on L_1 or several external components.
16	Shunt	Base of the Darlington transistor in the shunt regulator. When two PBL 3755 circuits are used in the repeater, the power-dissipation can be divided equally between them, if their pins 16 are connected. When used in a line terminal, this pin can drive an external series- or shunt-regulator power transistor.

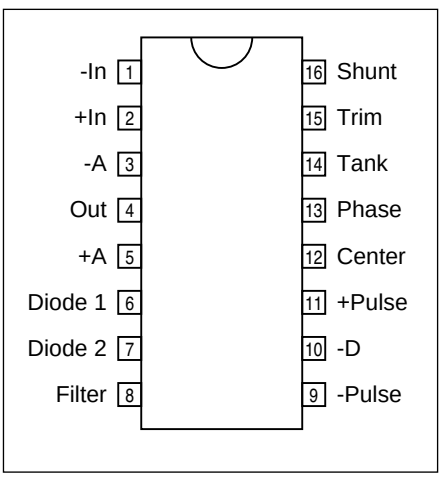


Figure 7. Pin configuration.

Functional Description

General

PBL 3755 contains all the active function necessary for a regenerative repeater optimized for a digital line interface. It meets the requirements for primary multiplexing equipment specified in CCITT G.703 with bit rates of 2048 respectively 1544 kbit/s.

The function blocks are: pre-amplifier, threshold-voltage generator, comparator bank, buffer and active controlled impedance elements for double section ALBO (Automatic Line-Build-Out) circuit, clock-regenerator, latches, gates, line drivers and a voltage regulator (see figure 8).

The external functions, equalizer and protection diodes, are shown in figure 10. It is assumed that the input from the line is transformer-coupled as well as the output. Power can then be supplied in the phantom circuit using center-tapped transformers.

PBL 3755 is designed primarily for HDB-3 coded signals at 2.048 Mbit/s but will equally well work at 1.544 Mbit/s and AMI coding (values for 1.544 Mbit/s are given within parentheses when applicable). Its low current consumption, typically 8 mA for internal circuitry, allows two repeater chips (for example one for each direction of transmission) to be powered from a standard 48 mA source — also extra facilities such as error detection and addressing.

The supply voltage for both PBL 3755 and the output transformer is only 5.25 V (5.5 V max.), determined by the internal shunting voltage regulator at balanced supply currents.

Pre-amplifier

The amplifier brings the level of the input signal to a value of 2 V (peak to peak) at the Out pin (pin4). These waveforms are shown in figure 9. The external feedback network, ß(s) in figure 10, provides the non-variable equalization necessary for maximum cable length. The high open-loop gain, 60 dB, together with a gain-bandwith product of 2 GHz allows the closed-loop transfer function to be well determined by external components, quite independently of the exact shape of the open loop transfer function. Furthermore the open-loop gain is reasonably temperature-stable.

The placement of the input pins makes them insensitive to stray capacitance, together with the fact that the analog ground (-A, pin 3) separates inputs and output, minimizes unwanted feedback. Bias voltage is taken from a temperature-stabilized output on PBL 3755 (Center, pin 12), which guarantees latch-up free operation for all temperatures. The input impedance is far higher than will actually be utilized in this application. The input offsets (current and voltage) are low considering that this is a wide-band device, because the DC-error introduced here will be added to the uncertainty of the detector thresholds.

ALBO

The signal level at the amplifier output is regulated by the peak-comparators, which sense the peaks and produce control current for the ALBO buffer. This, in turn, forces current through the ALBO diodes controlling their dynamic resistance. The ALBO diodes are part of the frequency dependent voltage divider chain preceding the amplifier, ß(s) (figure 10).

Since the amplification of the ALBO buffer is very high, the resulting amplitude at the amplifier output (pin 4) is regulated to an almost constant value, independent of input level from the line. The nominal levels of the peak-comparators are +1 V and -1 V relative to the Center pin.

An optimum design of the ALBO-network makes it simulate the transfer function of any cable up to maximum length, corresponding to an attenuation of 45 dB or more at 1 MHz.

PBL 3755 will always adjust the current in the ALBO diodes so that the pulses at the amplifier output are 2 V (peak-to peak). Thanks to the availability of two impedance elements, each consisting of four diodes, the transfer function is variable at least up to second order, and can equalize all cable lengths in one continuous range - without switching the ALBO network by strapping. In practice, the maximum input level is only limited by the non-linearity in the first diode chain, which can handle at least twice the amplitude of previous designs with a single diode. When maximum cable is connected, the ALBO network does not attenuate at all, and the full closed-loop gain of the amplifier is used. However, it is assumed that there is a high-pass passive filter section, $\alpha(s)$, after the input transformer for pre-equalization, which reduces the total amplitude. The pre-filter also forms the line termination. To keep the load impedance resistive a ”conjugate link”- or ”bridged-T”-network is suitable as $\alpha(s)$. Partly the high-frequency can also be introduced in the ALBO network, but the major cutoff of cross-talk and switching noise is provided by the feedback network ß(s).

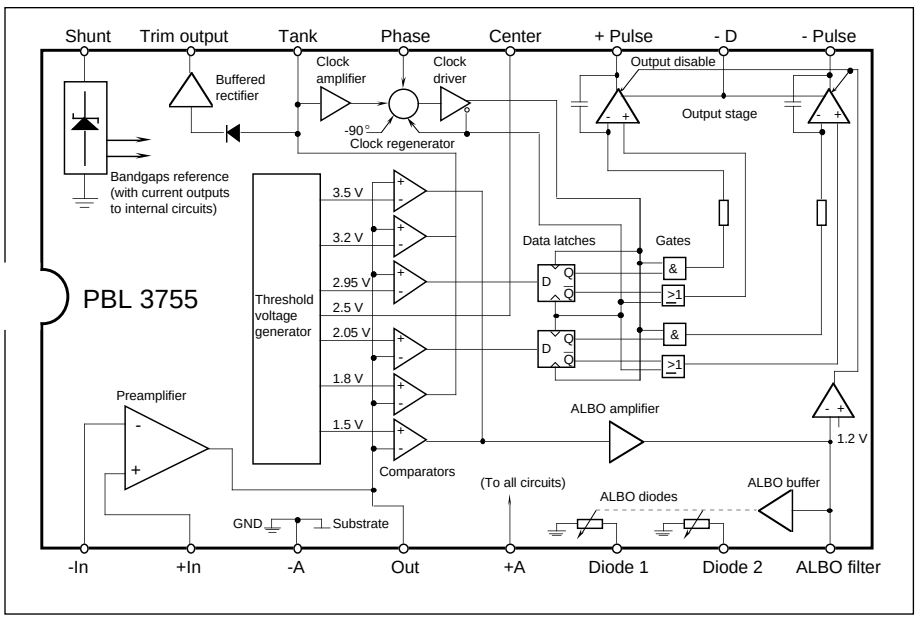


Figure 8. Functional diagram.

Clock Extraction

The clock-comparators have a threshold of 70 % of the ALBO threshold. All thresholds are referenced to the output of the temperature-stabilized voltage-generator, Center (pin 12), which biases the pre-amplifier by the input-network. When the outputs of the two comparators are added, they give pulses that are the full-wave rectified and limited peaks of the amplified signal. See figure 9. These pulses, occurring intermittently depending on the code pattern at the bit-frequency 2.048 MHz (1.544 MHz) with an amplitude of 100 µA, drive the external LCR tank circuit. Thus the clock is recovered in such a phase that the negative peaks of the sinusoidal wave correspond to the peaks of the PCM signal, as in figure 9, curve V(Tank). The quality-factor of the tank is determined by the losses in its inductor and the parallel resistor. A typical value of Q = 50 is supposed to be obtainable with a total loss conductance of 50 µS.

The threshold was chosen to give maximum energy of the dominant Fourier component (after ”rectifying” the input signal at clock frequency) at twice the frequency of the nearly cosine-shaped 1.024 MHz (772 kHz) signal. This results from a bipolar ..+1 ...-1 ...+1.. code sequence, that is to say that the tank current is then a square wave of 100 µA with 50 % duty cycle.

Data Extraction

The threshold of the data comparators are set to 45 % of their corresponding ALBO-thresholds. This value has been found to be the widest point of the eye-diagram of a pseudo-random sequence for most types of equalized lines. The digital signals at the comparator outputs are fed to the latches. These are of the “following, edge-triggered” type, thus allowing an accurate, well confined sampling instant.

Clock Regeneration

The clock regenerator block is needed to amplify and limit the varying tank signal and to provide a driver for the latches and the gates, as well as to give a well controlled sampling time.

Sampling must be done at the peaks of the equalized PCM-signal, where its signal-to-noise ratio is optimum. At these points, the tank sine-wave has its negative peaks. The negative slope zero-crossing of the sinusoidal wave must be phase-shifted 90 degrees to the sampling edge of the internal clock.

It is also obvious from figure 9, curve V(Tank), that the only amplitude-independent point of the sine-wave, from which to trigger the clock generator, is the zero-crossing. This phase shift is performed by an internal delay circuit, which is automatically regulated to a total of 90 degrees, i.e. 25 % of the period or 122 ns at 2.048 MHz (162 ns at 1.544 MHz). The clock regenerator regulates the phase independently of the exact frequency and without any frequency-dependent external components (and will do so also at 1.544 MHz).

It is very important for the sampling phase that the tank coil be well-adjusted. To simplify this during production, PBL 3755 is provided with a rectified and buffered output (Trim, pin 15) reflecting the amplitude of the tank, thus allowing the connection of a simple voltmeter without loading the tank. The capacitive loading even of a high-impedance probe which gives an incorrect adjustment is thus avoided.

The clock driver provides two low-impedance internal clocks of opposite phase to drive the latches and gates.

Latches and Gates

The latches are transparent to the data signal until the sampling instant, their outputs must be gated with the clock to produce PCM pulses of correct duration. The gates are doubled, using both an AND and an OR type, giving two complementary voltages with identical delay times to drive the output stages.

Output Stages

The output stages determine the amplitude of the pulses (the difference between the supply voltage and the saturation voltage of the Schottky-transistors), and also the rise and fall times.

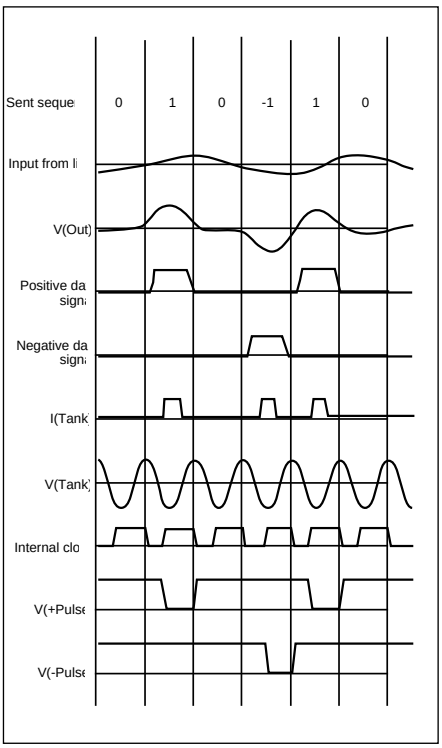


Figure 9. Timing diagram.

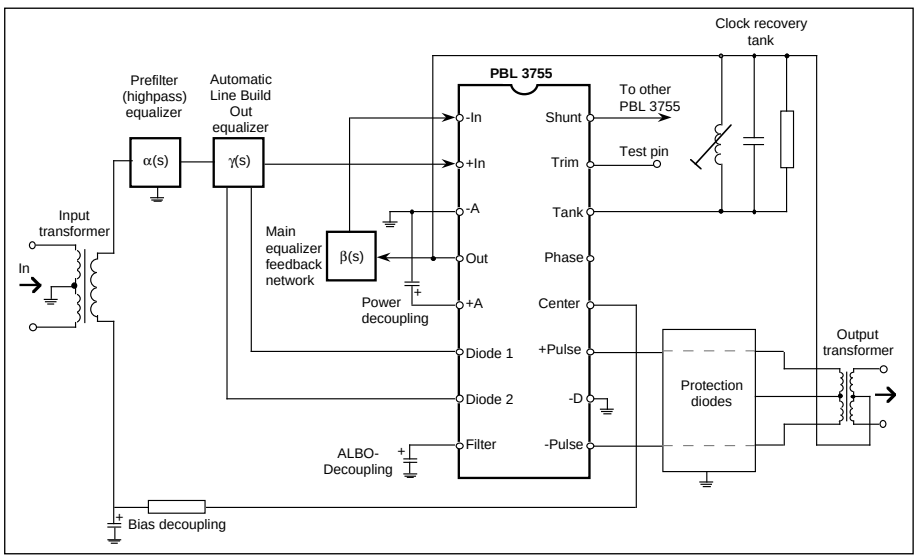


Figure 10. Block diagram.

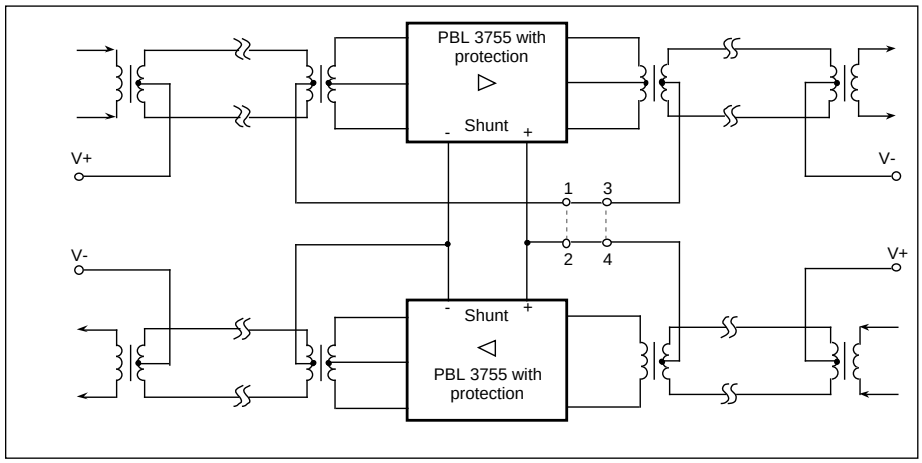


Figure 11. Typical repeater powering arrangement.

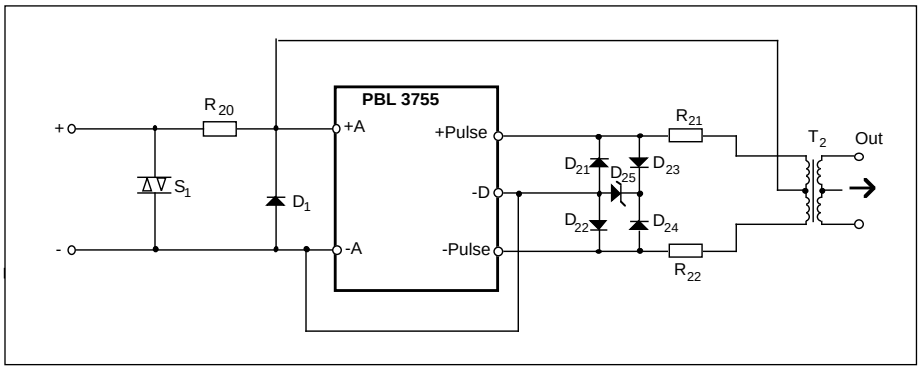


Figure 12. Typical overvoltage protection.

Requirements	Protection of +A	Protection of +Pulse and -Pulse
Lightning, longitudinal 200 A 10/700 us	Positive: S_1 limits to +22 V Negative: D_1 limits to -2.5 V (when S_1 to -22 V)	Less severe than transversal: R_{21}, R_{22} limit current Negative: Not critical thanks to D_1 and R_{20}.
AC short, longitudinal 50 Hz 0.5 s	Positive: S_1 limits to +22 V Negative: D_1 limits to -2.5 V (when S1 to -22 V)	Positive: R_{21}, R_{22} and D_{25} dissipate the power. Negative: Less severe with D_1 and R_{20}.
Lightning, transversal 100 A 10/700 us	Less severe than longitudinal	T_2 saturates. D_{23}, D_{24} and D_{25} limit to +14 at the current peak T_2 gives on its secondary. Similarly D_{21} and D_{22} limit to -3 V.
AC short, transversal 50 Hz 0.5 s	Less severe because of the low inductive reactance in T_2.	

Note: Suggested component types are given in figure 12. There are several cases of transients that must be considered to determine what the repeater can withstand. In the specification of the system these are probably separated in longitudinal (balanced on each pair i.e. in the powering path) and transversal,(symmetric i.e. the signal path) components.

Table 1. Typical overvoltage protection (Refer to figure 11).

The latter are chosen to allow the use of an inexpensive output transformer without interference from leakage inductance and stray capacitance. With the built-in ramp integrator, the edge steepness and hence high-frequency energy is limited. By using a Miller feedback driven by the doubled gates, equal rise and fall times in each channel are obtained that conserve the pulse width.

The pulse outputs also have networks protecting the transistors during over-voltage conditions, thus requiring only low-cost signal diodes external to PBL 3755 (see figure 11). This protection is combined with the output-disable mechanism, which inhibits the pulses on the following conditions:

- during power-up before the supply has reached a sufficiently-high voltage level for safe operation. The outputs cannot latch up in an on-condition sinking all available supply current.
- in the absence of input signal of sufficient strength, which would otherwise produce invalid data, or even (after the tank oscillation has ceased) lock the outputs in an undetermined state.
- when the supply voltage rises above 8V during a lightning or switching surge.

Voltage Regulator

The regulator can be seen as an ideal zener diode, with very low dynamic series resistance even at low current, shunting the excess current at a constant, temperature-stabilized supply voltage. This is the only supply needed for internal circuitry, output transformers and possible external facilities. Since two PBL 3755 normally operate together in the same unit, they can be connected in parallel , equally sinking excess current. The voltage regulator, which is based on the bandgap-reference principle, also supplies other internal parts with sufficient constant quiescent current. The zener characteristic is modified at voltages over 6 V. It limits the current drain during over-voltage conditions to a reasonable value. For the protection circuitry needed see figure 12.

L_1 31 µH Trimmable ferrite core
C_1 191 pF
R_1 43.2 kohm

First ALBO-section
L_6 220 µH Miniature
R_6 154 ohm
C_6 2.2 µF 6V elyt

High-pass pre-filter
R_2 110 ohm
R_3 110 ohm
R_4 10 ohm
C_2 1.00 nF
L_2 10 µH Miniature
R_5 121 ohm

Nyquist low-pass filter
R_7 1.10 kohm
C_7 221 pF

Second ALBO-section
R_8 3.32 kohm
R_9 365 ohm
C_8 5.62 nF
C_9 2.2 µF 6V elyt

Pre-amp feedback network
R_{10} 5.62 kohm
R_{11} 287 ohm
C_{11} 1.00 µF 6V tantal
R_{12} 43.2 ohm
C_{12} 2.15 nF
L_{12} 3.3 µH Miniature
R_{13} 178 ohm

Bias decoupling for pre-amplifier
R_{15} 1.12 kohm
C_{15} 10 µF 6V elyt

Albo-filter capacitor
C_{16} 10 µF 6V elyt

Supply decoupling
C_{20} 22 µF 25V elyt

Thyristor-diode for supply protection
S_1 LS5018
D_1 1N5059
R_{20} 4.7 ohm 1W

Input protection
D_2 - D_5 1N4148

Output protection
R_{21} 30.1 ohm 0.5W
R_{22} 30.1 ohm 0.5W
D_{21} - D_{24} 1N5059
D_{25} BZT03/D12

Ferrite core transformer
T_1 1:1
T_2 1.35:1

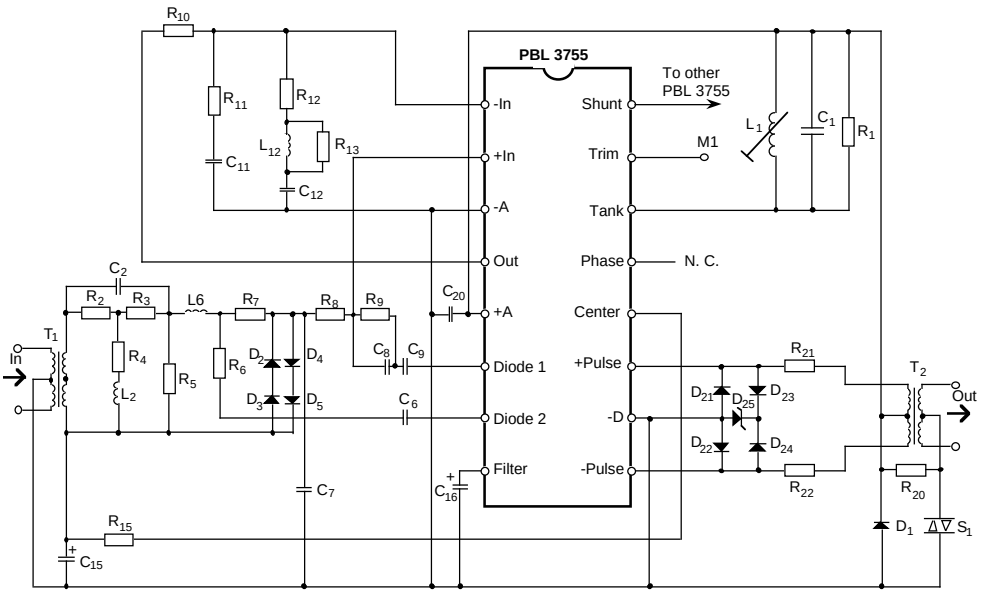


Figure 13. Application example for European S1 repeater.

Tank circuit
L_1 41 µH Trimmable ferrite core
C_1 249 pF
R_1 43.2 kohm

Line-termination
R_5 432 ohm

First ALBO-section
R_6 3.01 kohm
R_7 3.01 kohm
C_6 150 pF
C_7 150 pF

Second ALBO-section
R_8 1.10 kohm
C_8 22.1 nF
R_9 121 ohm
C_9 0.1 µF
C_{10} 0.1 µF

Pre-amplifier fedback network
R_{10} 5.49 kohm
R_{11} 562 ohm
C_{11} 0.1 µF
R_{12} 51.1 ohm
C_{12} 3.92 nF
L_{12} 3.3 µH Miniature
R_{13} 130 ohm

Bias decoupling for pre-amplifier
R_{15} 1.33 kohm = R10-R7-R8
C_{15} 10 µF 6V elyt

ALBO-filter capacitor
C_{16} 10 µF 6V elyt

Supply decoupling
C_{20} 22 µF 25V elyt

Thyristor-diode for supply protection
S_1 LS5018
D_1 1N5059

Output protection
R_{21} 30.1 ohm 0.5W
R_{22} 30.1 ohm 0.5W
D_{21} - D_{24} 1N4148
D_{25} 1N4741

Ferrite core transformer
T_1 1:1
T_2 0.66:1

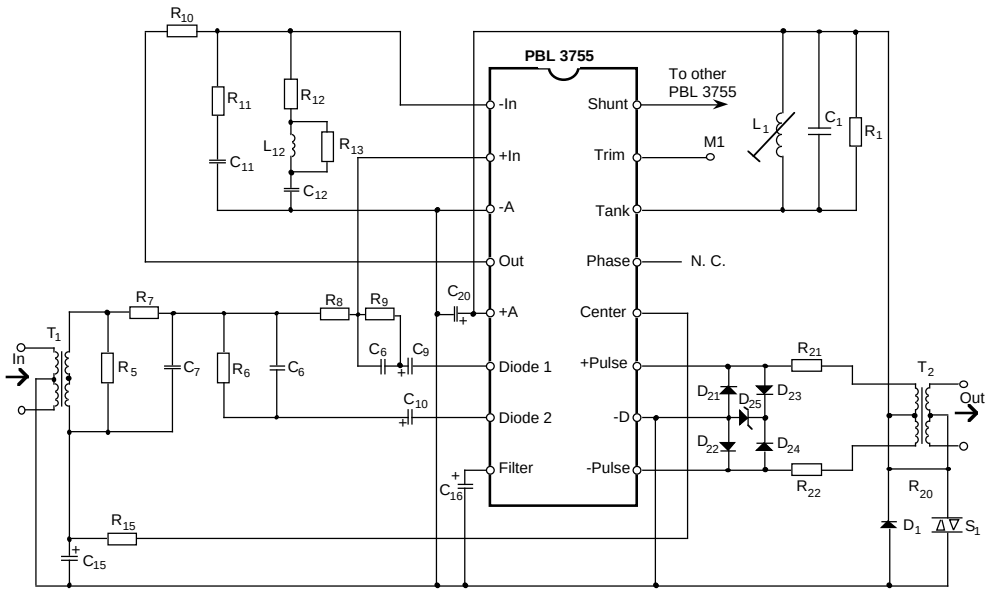


Figure 14. Application example for U.S. T-1 repeater.

Application Examples

European S-1 Repeater

Figure 13 shows PBL 3755 in a typical circuit of a repeater for 2.048 MHz. Special care has been taken to ensure very good capability to withstand current surges from lightning and short-circuits. Depending on external components, chosen CCITT requirements can be fulfilled or surpassed. The supply lines are protected by a low-voltage thyristor-diode, S_1 which is much less expensive than the gas-discharge tubes otherwise often used. The pulse-outputs (pins 9, 11) can be protected by a simple zener-diode bridge, D_{21} … D_{25}, and the input is easily protected by anti-parallel small rectifier diodes, D_2 … D_5, thanks to the higher impedance of the ALBO-components.

The high capability of the ALBO and amplifier sections of PBL 3755 has been fully utilized in this example by applying two ALBO networks, with a preceding highpass filter as line-termination. This amount of external components is typical for a high-performance repeater, which can equalize very long lines, 45 dB or more, if the entire circuit is optimized for the types of cable used. The rather elaborate pre-filter reduces the total amplitude before the ALBO network. High-frequency components, which are already attenuated by the cable, pass without attenuation. A linear attenuation in the line-termination would have demanded more gain in the amplifier, a certain degree of attenuation is necessary not to overload the ALBO diodes causing clipping. PBL 3755, however, can handle up to 120 mV (peak to peak) because of the series-connected diodes, and this is equivalent to another 6 dB in the open-loop gain of the amplifier when comparing to other repeater IC's.

The amplifier's stability margins are good, but if there is coupling capacitance on the board between Out (pin 4) and the ALBO components, a neutralizing capacitor across R_{10} may be needed. In this and other respects board layout is simplified by the pin placement on PBL 3755: groups of signal-carrying pins are separated by those which are AC-grounded. Center (pin 12) and Shunt (pin 16) can also be decoupled in case of problems. The bias decoupling capacitor (C_{15}) is mainly ground for the input signal, although the input transformer is part of the DC-path biasing the amplifier. Instead, an arrangement with coupling capacitors in the signal path and a directly-grounded input transformer is possible, thus the ALBO diodes can still be AC-coupled.

The tank circuit is assumed to have a trimmable coil. A trimmer capacitor is also suitable, provided that the inductance is within such tolerances that the trimming range is sufficient. The trimming rectifier output is simply brought out to a test point or hook.

Decoupling of the power supply is drawn as C_{20}, but for a repeater board with two PBL 3755 it is preferably realized with one small capacitor close to each one of them for HF-decoupling, in addition to a main electrolytic capacitor elsewhere to which -D (pin 10) is directly wired. It is important that +A (pin 5) is just as good as signal ground as is -A (pin 3). Note that the total capacitance in place of C_{20} must be more than 10 µF per PBL 3755 to ensure stability in the voltage regulator. This applies whether their Shunt (pin 16) pins are connected to divide power dissipation equally between them or not.

If the sampling phase adjustment option is not used, as here, the Phase pin (pin 13) should not be connected to copper foil on the board at all, this avoids capacitive pick-up and a sampling offset.

U.S. T-1 Repeater

The example for 1.544 MHz is somewhat simpler than the one above to show an application with minimum component count, figure 14. Mainly the pre- and ALBO- filters are very simple, and this reflects the less stringent requirement of the T-1 line, where the maximum attenuation may be around 35 dB at 772 kHz. Two active ALBO elements are still used, but if PBL 3755 is to replace an older repeater IC in a well-proven circuit with a single ALBO tap, Diode 1 and Diode 2 can be directly tied together.

Also for protection inexpensive standard components have been emphasized and not optimum reliability. Along with this, the input protection diodes are omitted relying on the internal zeners and diodes of PBL 3755. It will have to be carefully investigated what the completed board can withstand, since it depends much on the saturation characteristics of the transformers used and on the board layout. The diodes suggested, although they will usually serve as fairly good transient suppressors, are not intended as such and are not specified accordingly in data sheets. The protection of the S-1 repeater example above is much safer in this respect and is recommended as first choice.

Ordering information

Package	Temp. Range
Part No.	
Ceramic DIP PBL 3755J	-40 to +70°C

1522-PBL 3755 Uen Rev. A

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