PBL 3762A, PBL 3762A/4 Subscriber Line Interface Circuit

Description

The PBL 3762A Subscriber Line Interface Circuit (SLIC) is a bipolar integrated circuit in 90 V technology which replaces the conventional transformer based analog line interface circuit in Digital Loop Carrier, PABX and other telecommunications equipment with a modern, compact solid state design. Not only is required PCB area reduced, but lesser component weight and height result as well. The PBL 3762A has been optimized for low cost and to require only a minimum of external components.

The PBL 3762A is an improved version of the PBL 3762.

The PBL 3762A programmable, resistive battery feed system can operate with battery supply voltages down to 21 V to reduce line card power dissipation.

The SLIC incorporates loop current, ground key and ring trip detection functions as well as a ring relay driver.

Two- to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter (e.g. SLAC, SiCoFi, Combo II). The programmable line terminating impedance could be complex or real to fit every market.

Longitudinal line voltages are suppressed by a feedback loop in the SLIC. Longitudinal balance specifications exceed Bellcore and EIA requirements.

The PBL 3762A has an external saturation guard programming resistor while the PBL 3762A/4 has a preset open loop voltage of 45V.

The PBL 3762A and PBL 3762A/4 packages are 22-pin dual-in-line or 28-pin PLCC.

Key Features

- Battery feed characteristics programmable via external resistors; feed characteristics independent of SLIC battery supply variations
- Battery supply voltage as low as 21 V for power efficient line card designs
- Ring relay driver
- Loop current, ground key and ring trip detection functions
- Programmable loop current detector threshold
- Hybrid function with all types of CODEC/filter devices
- Programmable line terminating impedance, complex or real
- On-hook transmission
- Longitudinal balance specifications in excess of Bellcore and EIA requirements
- Low 35 mW @-24 V on-hook power dissipation
- Tip-ring open circuit state for subscriber loop power denial
- -40°C to +85°C ambient temperature range

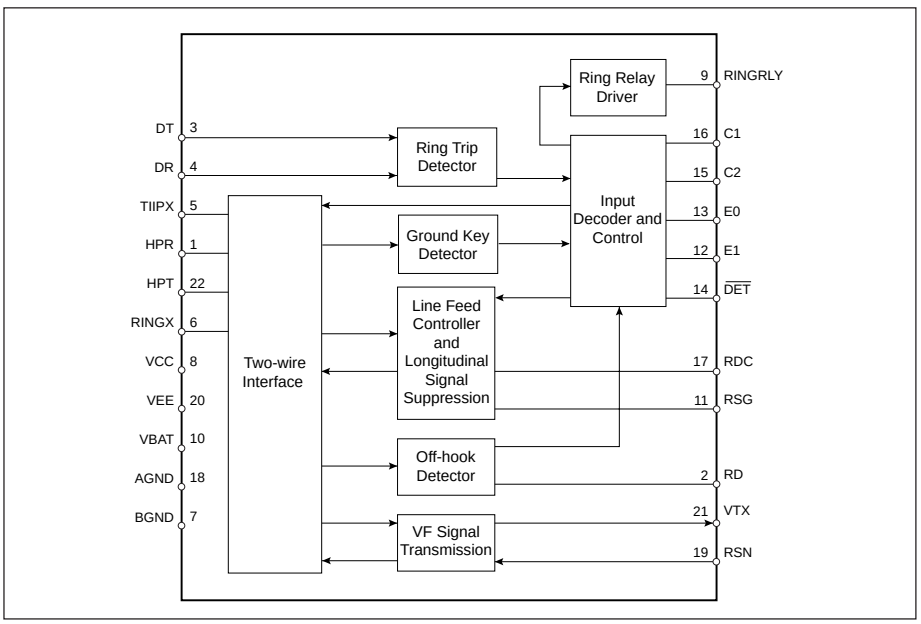
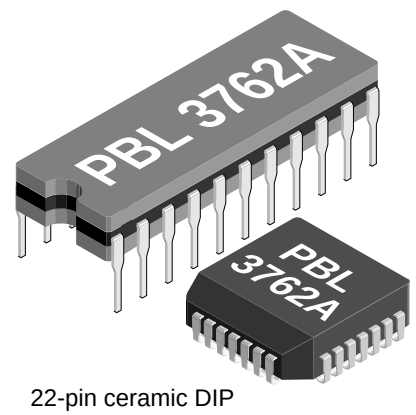


Figure 1. Block diagram.



22-pin ceramic DIP
28-pin PLCC

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-60	+150	°C
Operating junction temperature range	T_J	-40	+140	°C
Storage humidity, Note 1	RH	5	95	% RH
Power supply, -40°C ≤ T_{Amb} ≤ 85°C				
V_{CC} with respect to AGND	V_{CC}	-0.5	6.5	V
V_{EE} with respect to AGND	V_{EE}	-6.5	0.5	V
V_{Bat} with respect to BGND	V_{Bat}	-70	V_{EE}+0.6	V
Power dissipation				
Continuous power dissipation at T_{Amb} ≤ 70 °C	P_D		1.5	W
Peak power dissipation at T_{Amb} ≤ 70 °C, t < 100 ms, t_{Rep} > 1 sec.	P_{DP}		4	W
Ground				
Voltage between AGND and BGND	V_G	-0.3	0.3	V
Relay driver				
Ring relay supply voltage	V_{RRly}	0	V_{Bat}+75	V
Ring relay current	I_{RRly}		50	mA
Ring trip comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	0	V
Input current	I_{DT}, I_{DR}	-5	5	mA
Digital inputs, outputs (C1, C2, E0, E1, $\overline{DET}$)				
Input voltage	V_{ID}	0	V_{CC}	V
Output voltage ($\overline{DET}$ disabled)	V_{OD}	0	V_{CC}	V
Output current ($\overline{DET}$ enabled)	I_{OD}		5	mA
TIPX and RINGX terminals, -40°C < T_{Amb} < 85°C, V_{Bat} = -50V				
TIPX or RINGX voltage, continuous (referenced to AGND), Note 2	V_{TA}, V_{RA}	V_{Bat}	2	V
TIPX or RINGX, pulse < 10 ms, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} -20V	5	V
TIPX or RINGX, pulse < 1 µs, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} -40V	10	V
TIP or RING, pulse < 250 ns, t_{Rep} > 10 s, Note 3	V_{TA}, V_{RA}	V_{Bat} -70V	15	V
TIPX or RINGX current	I_{LT}, I_{LR}		70	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{EE} with respect to AGND	V_{EE}	-5.25	-4.75	V
V_{Bat} with respect to BGND, Note 4	V_{Bat}	-58	-24	V

Notes

1. Applicable for ceramic package.
2. A diode in series with the V_{Bat} input increases the permitted continuous voltage and pulse < 10ms to -70V. A pulse ≤ 1µs is increased to the greater of |-70V| or |V_{Bat} - 40V|.
3. R_{F1}, R_{F2} ≥ 20 Ω is also required. Pulse is supplied to TIP and RING outside R_{F1}, R_{F2}.
4. -24 V < V_{Bat} < -21 V may be used in applications requiring maximum vf signal amplitudes less than 3 V_{Pk} (8.75 dBm, 600 Ω).

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ 85 °C, Note 10, V_{CC} = +5V ±5 %, V_{EE} = -5V ±5%, V_{Bat} = -48V, AGND = BGND, R_{SG} = 20kΩ (for PBL 3762A/4 R_{SG} = 0Ω), R_{DC1} = R_{DC2} = 20 kΩ. Z_L = 600 Ω, C_{HP} = 10 nF, C_{DC} = 3.3 µF unless otherwise specified. All pin number references in the text and figures refer to the 22-pin DIP unless otherwise specified.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	2	Z_L = 600 Ω, 1% THD, Note 1	3.1			V_{Peak}
Input impedance, Z_{TR}		Note 2				
Longitudinal impedance, Z_{LoT}, Z_{LoR}		0 < f < 100 Hz		10	35	Ω/wire
Longitudinal current limit, I_{LoT}, I_{LoR}		active state		27		mA_{rms}/wire
		stand-by state		8,5		$mA_{rms/}$ wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985				
		0.2 kHz ≤ f ≤ 3.4 kHz				
		0°C ≤ T_{Amb} ≤ 70°C	63	70		dB
		-40°C ≤ T_{Amb} ≤ 85°C	55	70		dB
Longitudinal to metallic balance, B_{LME}	3	0.2 kHz ≤ f ≤ 3.4 kHz				
		$B_{LFE} = 20 \bullet \text{Log} \left\lvert \frac{E_{Lo}}{V_{TR}} \right\rvert$				
		0°C ≤ T_{Amb} ≤ 70°C	63	70		dB
		-40°C ≤ T_{Amb} ≤ 85°C	55	70		dB
Longitudinal to four-wire balance, B_{LFE}	3	0.2 kHz ≤ f ≤ 3.4 kHz				
		$B_{LFE} = 20 \bullet \text{Log} \left\lvert \frac{E_{Lo}}{V_{TX}} \right\rvert$				
		0°C ≤ T_{Amb} ≤ 70°C	63	70		dB
		-40°C ≤ T_{Amb} ≤ 85°C	55	70		dB
Metallic to longitudinal balance, B_{MLE}	4	0.2 kHz ≤ f ≤ 3.4 kHz	50	55		dB
		$B_{MLE} = 20 \bullet \text{Log} \left\lvert \frac{E_{TR}}{V_{Lo}} \right\rvert$, E_{RX} = 0				
Four-wire to longitudinal balance, B_{FLE}	4	0.2 kHz ≤ f ≤ 4.0 kHz	50	55		dB
		$B_{FLE} = 20 \bullet \text{Log} \left\lvert \frac{E_{RX}}{V_{Lo}} \right\rvert$				
		E_{TR} source removed				

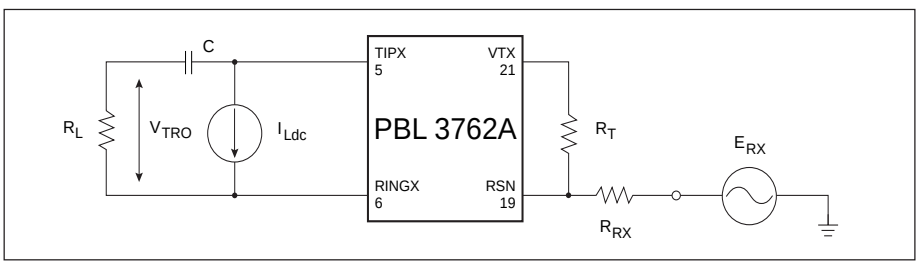


Figure 2. Overload level, V_{TRO}, two-wire port.

$\frac{1}{\omega C}$ << R_L, R_L= 600 Ω

R_T = 600 kΩ, R_{RX} = 300 kΩ

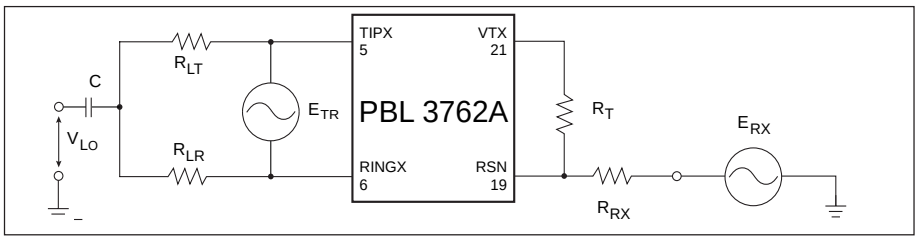


Figure 3. Longitudinal to metallic (B_{LME}) and Longitudinal to four-wire (B_{LFE}) balance.

$\frac{1}{\omega C}$ << 150 Ω, R_{LR} = R_{LT} = 300 Ω

R_T = 600 kΩ, R_{RX} = 300 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire return loss, r		$r = 20 \bullet \text{Log} \frac{\lvert Z_{TR} + Z_L \rvert}{\lvert Z_{TR} - Z_L \rvert}$				
		$Z_{TR} \approx Z_L$ = nom. 600 Ω				
		0.2 kHz ≤ f ≤ 0.5 kHz	25			dB
		0.5 kHz ≤ f ≤ 1.0 kHz	27			dB
		1.0 kHz ≤ f ≤ 3.4 kHz, Note 3	23			dB
TIPX idle voltage, V_{Ti}		3762A, active, I_L = 0		- 3		V
		3762A/4, active, I_L = 0		-1.5		V
		stand-by, I_L = 0		0.6		V
RINGX idle voltage, V_{Ri}		3762A, active, I_L = 0		- 45		V
		3762A/4, active, I_L = 0		- 46.5		V
		stand-by, I_L = 0		- 48		V
TIPX-RINGX open loop		3762A, I_L = 0, R_{SG} = 20 kΩ		42.0		V
metallic voltage, V_{TR}		3762A/4, I_L = 0, R_{SG} = 0 Ω, V_{Bat}= -52V	43.0	45.0	47.0	V
Four-wire transmit port (V_{TX})						
Overload level, V_{TXO}	5	Load impedance > 20 kΩ, 1% THD, Note 4	3.1			V_{Peak}
Output offset voltage, ΔV_{TX}		0°C ≤ T_{Amb} ≤ 70°C	-30		30	mV
		-40°C ≤ T_{Amb} ≤ 85°C	-40		40	mV
Output impedance, z_{TX}		0.2 kHz ≤ f ≤ 3.4 kHz		<5	20	Ω
Four-wire receive port (RSN)						
Receive summing node (RSN) dc voltage		I_{RSN} = 0 mA		0		V
Receive summing node (RSN) impedance		0.2 kHz ≤ f ≤ 3.4 kHz		<10	20	Ω
Receive summing node (RSN) current (I_{RSN}) to metallic loop current (I_L) gain, α_{RSN}		0.3 kHz ≤ f ≤ 3.4 kHz		1000		ratio
Frequency response						
Two-wire to four-wire, g_{2-4}	6	0.3 kHz ≤ f ≤ 3.4 kHz relative to 0 dBm, 1.0 kHz. E_{RX} = 0 V				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB

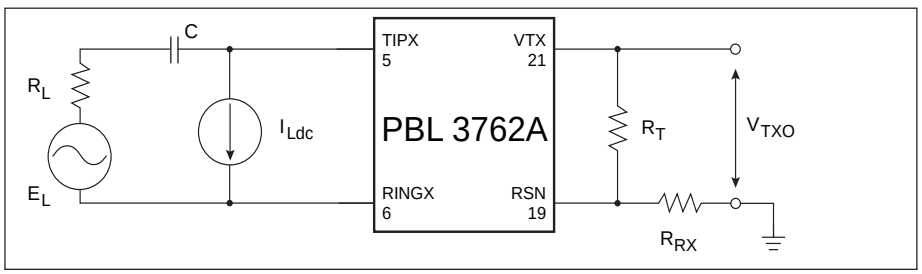


Figure 4. Metallic to longitudinal and four-wire to longitudinal balance

$\frac{1}{\omega C} << 150\ \Omega$, $R_{LT} = R_{LR} = 300\ \Omega$

R_T = 600 kΩ, R_{RX} = 300 kΩ

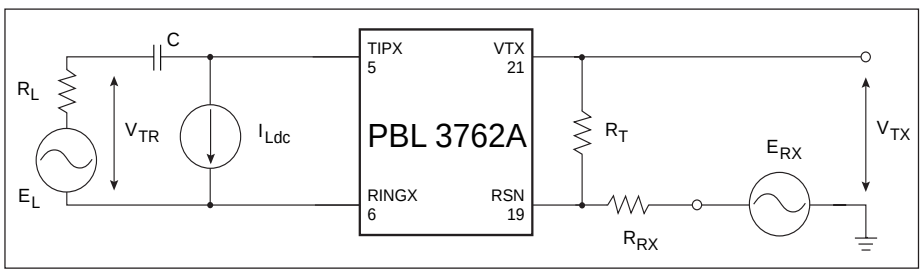


Figure 5. Overload level, V_{TXO}, four-wire transmit port

$\frac{1}{\omega C} << R_L$, R_L = 600 Ω

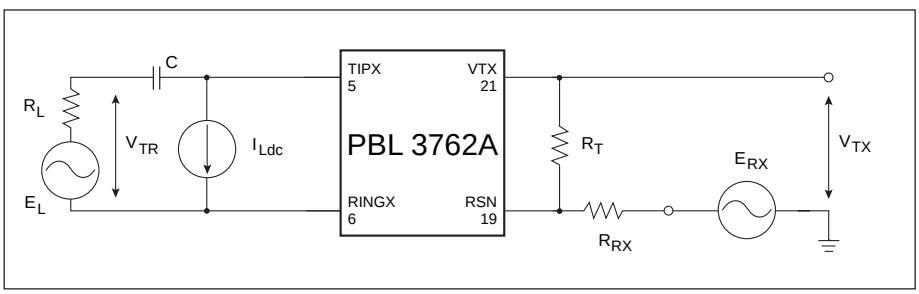
R_T = 600 kΩ, R_{RX} = 300 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to two-wire, g_{4-2}	6	0.3 kHz ≤ f ≤ 3.4 kHz relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Four-wire to four-wire, g_{4-4}	6	0.3 kHz ≤ f ≤ 3.4 kHz relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	6	0 dBm, 1.0 kHz, Note 5 $G_{2-4} = 20 \bullet \text{Log} \left\lvert \frac{V_{TX}}{V_{TR}} \right\rvert, E_{RX} = 0$				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Four-wire to two-wire, G_{4-2}	6	0 dBm, 1.0 kHz, Notes 5, 6 $G_{4-2} = 20 \bullet \text{Log} \left\lvert \frac{V_{TR}}{E_{RX}} \right\rvert, E_G = 0$				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Gain tracking						
Two-wire to four-wire	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Four-wire to two-wire	6	Ref. -10 dBm, 1.0 kHz, Note 8				
		-40 dBm to +7 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Noise						
Idle channel noise at two-wire (TIPX-RINGX) or four-wire (V_{TX}) output		C-message weighting		8.5	12.0	dBrnC
		Psophometrical weighting Note 9		-81.5	-78	dBmp
Harmonic distortion						
Two-wire to four-wire		0 dBm, 1.0 kHz test signal		-65	-54	dB
Four-wire to two-wire		0.3 kHz ≤ f ≤ 3.4 kHz		-65	-54	dB
Battery feed characteristics						
Active state loop current, I_L tolerance range		$I_L = \frac{50}{R_L + \frac{R_{DC1} + R_{DC2}}{50}}$	0.9•I_L	I_L	1.1•I_L	mA
Stand-by state loop current, I_L, tolerance range		$I_L = \frac{\lvert V_{Bat} \rvert - 3}{R_L + 1800}$ T_{Amb} = 25 °C	0.80 • I_L	I_L	1.20 • I_L	mA

Figure 6. Frequency response, insertion loss, gain tracking.

$\frac{1}{\omega C} << R_L$, R_L = 600 Ω

R_T = 600 kΩ, R_{RX} = 300 kΩ



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Loop current detector						
Loop current detector threshold, I_{LTh}		R_D= 33 kΩ				
		0°C ≤ T_{Amb} ≤ 70°C	9.8	375/R_D	12.8	mA
		-40°C ≤ T_{Amb} ≤ 85°C	9.0	375/R_D	13.7	mA
Ground key detector						
I_{LTIPX} and I_{LRINGX} current difference, ΔI_{LOn},		0°C ≤ T_{Amb} ≤ 70°C	9	12	16	mA
to trigger the ground key detector		-40°C ≤ T_{Amb} ≤ 85°C	8	12	17	mA
I_{LTIPX} and I_{LRINGX} current difference, ΔI_{LOff},		0°C ≤ T_{Amb} ≤ 70°C	4	7	11	mA
to return the triggered ground key		-40°C ≤ T_{Amb} ≤ 85°C	3	7	12	mA
detector to idle state						
Hysteresis, ∂I_{LGK}		$\lvert\Delta I_{LOn} - \Delta I_{LOff}\rvert$				
		0°C ≤ T_{Amb} ≤ 70°C	3	5	8	mA
		-40°C ≤ T_{Amb} ≤ 85°C	0	5	9	mA
Ring trip detector						
Offset voltage, ΔV_{DTR}		Source resistance, R_S = 0 Ω	-20	0	20	mV
Input bias current, I_B		$I_B = (I_{DT} + I_{DR})/2$	-500	-100		nA
Input resistance						
unbalanced			1			MΩ
balanced			3			MΩ
Input common mode range, V_{DT}, V_{DR}			V_{Bat}+1		-2	V
Ring relay driver						
Saturation voltage, V_{OL}		I_{OL} = 25 mA		0.2	0.6	V
Off state leakage current, I_{Lk}		V_{OH} = 12 V			10	µA
Digital inputs (C1, C2, E0, E1)						
Input low voltage, V_{IL}			0		0.8	V
Input high voltage, V_{IH}			2.0		V_{CC}	V
Input low current, I_{IL}		V_{IL} = 0.4 V				
C1, C2			-400			µA
E0, E1			-100			µA
Input high current, I_{IH}		V_{IH} = 2.4 V			40	µA
Detector output ($\overline{DET}$)						
Output low voltage, V_{OL}		I_{OL} = 2 mA			0.45	V
Output high voltage,V_{OH}		I_{OH} = 100 µA	2.7			V
Internal pull-up resistor			8	15	25	kΩ
Delay time E0 to $\overline{DET}$						
transition high to low, t_{DHL}	7				1	µs
transition low to high, t_{DHL}	7				2	µs
Power dissipation (V_{Bat} = -48V)						
P_1		Open circuit state, C1,C2 = 0, 0		40	70	mW
P_2		Stand-by state, C1, C2 = 1, 1; on-hook		60	85	mW
		Active state, C1, C2 = 0, 1				
P_3		On-hook, R_L = ∞ Ω		200	300	mW
P_4		Off-hook, R_L = 600 Ω		1.1	1.3	W
Power supply currents						
V_{CC} current, I_{CC}		Open circuit state		1.7	2.9	mA
V_{EE} current, I_{EE}		C1, C2 = 0, 0		1.0	2.0	mA
V_{Bat} current, I_{Bat}		On-hook		0.6	1.3	mA
V_{CC} current, I_{CC}		Stand-by state		2.1	3.5	mA
V_{EE} current, I_{EE}		C1, C2 = 1, 1		1.0	2.0	mA
V_{Bat} current, I_{Bat}		On-hook		0.9	1.6	mA

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
V_{CC} current, I_{CC}		Active state		5.1	8.0	mA
V_{EE} current, I_{EE}		C1, C2 = 0, 1		2.0	3.5	mA
V_{Bat} current, I_{Bat}		On-hook		3.3	5.2	mA
Power supply rejection ratios						
V_{CC} to 2- or 4-wire port		Active State	43	45		dB
V_{EE} to 2- or 4-wire port		C1, C2 = 0, 1	40	45		dB
V_{Bat} to 2- or 4-wire port		50 Hz < f< 3400 Hz, V_n = 100mV_{rms}	40	45		dB
V_{Bat} to 2- or 4-wire port		V_n = 2V_{PP}, Note 11	40	45		dB
Temperature Guard						
Junction threshold temperature, T_{JG}				150		°C
Thermal resistance						
28-pin PLCC, $\theta_{RJP28plcc}$		Junction to terminals 3, 6, 10, 17, 24 connected together, Note 12		13		°C/W
22-pin CDIP, $\theta_{RJP22dip}$				30		°C/W

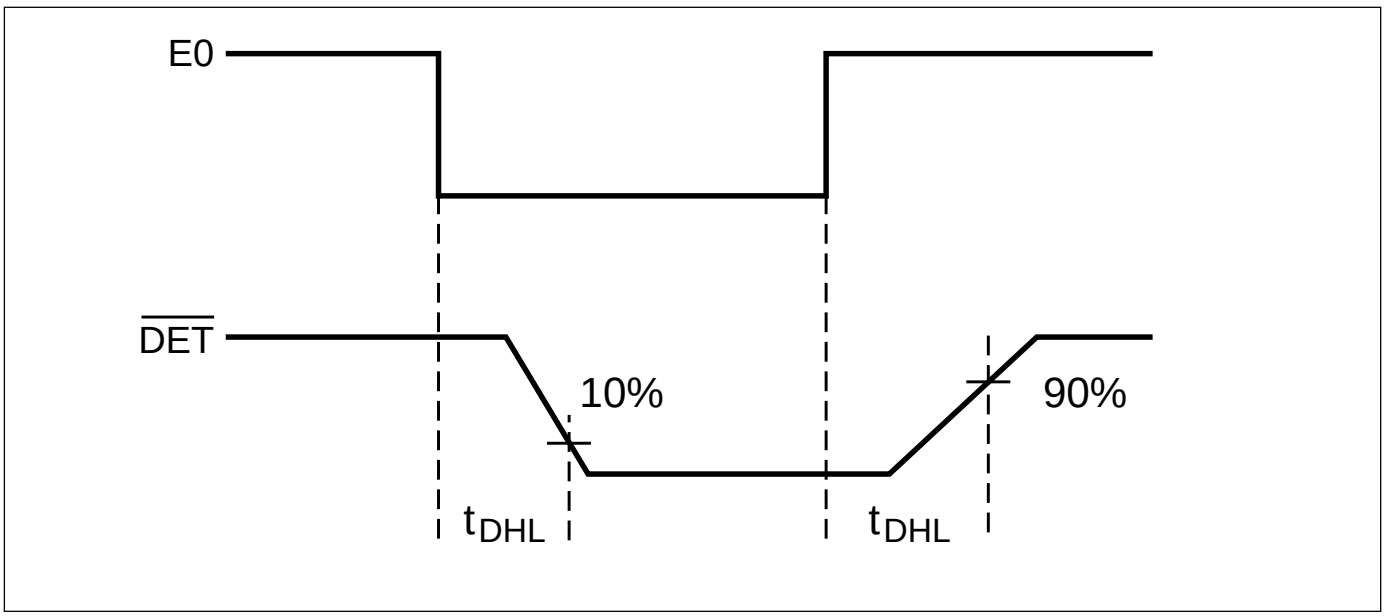


Figure 7. Detector output delay time.

Notes

1. The overload level is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:

   $Z_{TRX} = Z_T/|G_{2-4} \bullet \alpha_{RSN}|$ where:

   Z_{TRX} = impedance between the TIPX and RINGX terminals

   Z_T = programming network between the VTX and RSN terminals

   G_{2-4} = transmit gain, nominally = 1

   α_{RSN} = receive current gain, nominally = -1000 (current defined as positive flowing into the receivesumm-ing node, RSN, and when flowing from tip to ring).
3. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground. For R_T = 560 kΩ this capacitor would be approximately 30 pF. Increasing C_{HP} to 0.033 µF improves low frequency return loss.

4. The overload level is specified at the four-wire transmit port, V_{TX}, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2-4} = 1$.
5. Fuse resistors R_F impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for $R_F = 0$.
6. The specified insertion loss tolerance does not include errors caused by external components.
7. The level is specified at the two-wire port.
8. The level is specified at the four-wire receive port and referenced to a 600 Ω impedance level.
9. The two-wire idle noise is specified with the port terminated in 600 Ω (R_L) and with the four-wire receive port grounded ($E_{RX} = 0$; see figure 6).
   The four-wire idle noise at VTX is specified with the two-wire port terminated in 600 Ω (R_L). The noise specification is referenced to a 600 Ω impedance level at VTX. The four-wire receive port is grounded ($E_{RX} = 0$).
10. The -40°C – +85°C values are tested while the 0°C - 70°C values are given as an indication.
11. PSRR for V_{Bat} is reduced to min. 37 dB when the PLCC package is used.
12. Junction to ambient thermal resistance will be dependent on external thermal resistance from V_{Bat} terminals to ambient.

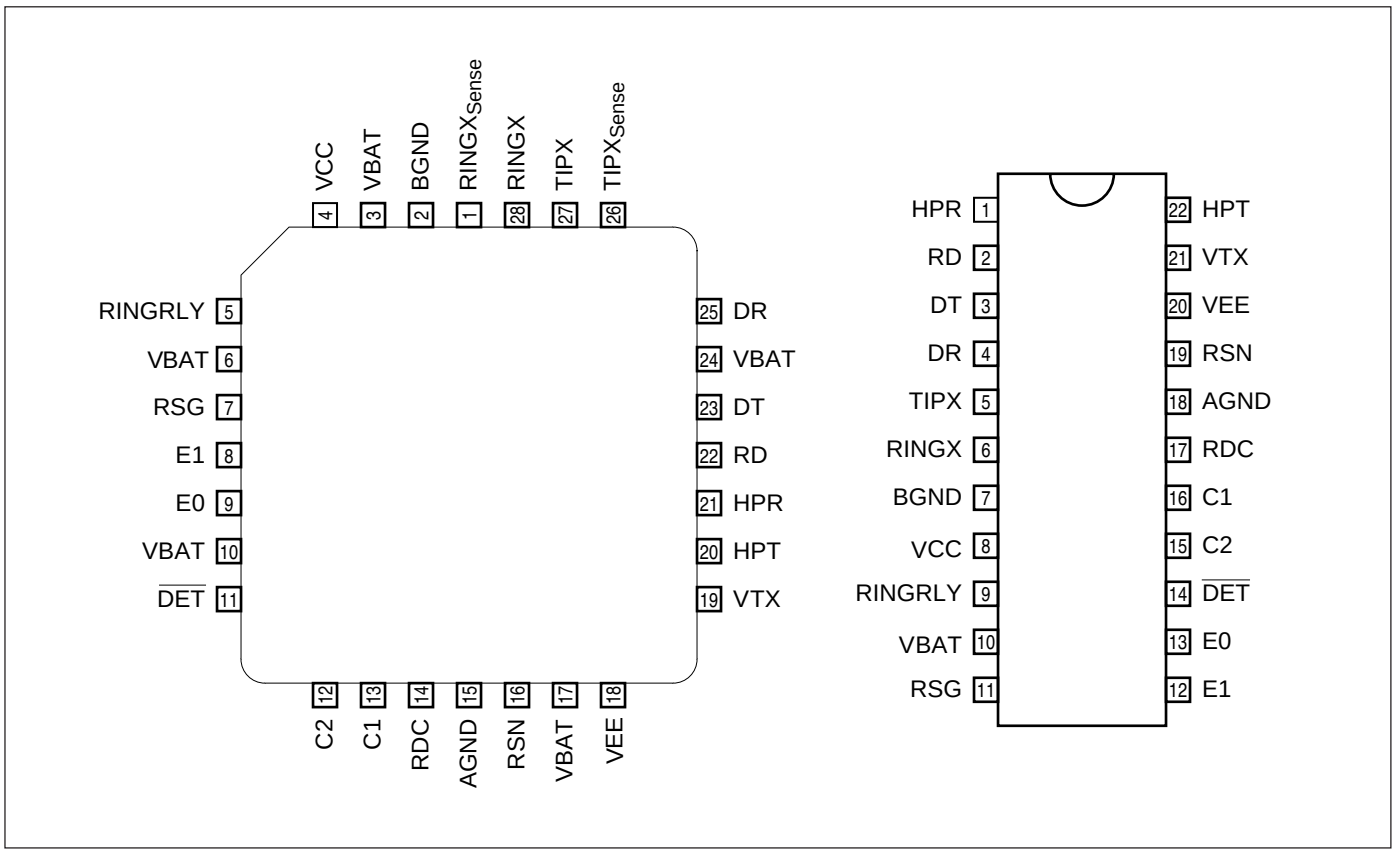


Figure 8. Pin configuration, 28-pin PLCC and 22-pin dual-in line package, top view.

Pin Descriptions

Refer to figure 8. Note: All pin number references in the text and figures refer to the 22-pin DIP unless otherwise specified.

DIP	PLCC	Symbol	Description
1	21	HPR	Ring side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} connects to pin 22, HPT.
2	22	RD	Off-hook detector programming resistor R_D in parallel with filter capacitor C_D connect from RD to VEE.
3 4	23 25	DT DR	Inputs to the ring trip comparator. With DR more positive than DT the detector output, $\overline{DET}$ (pin 14), is at logic level low, indicating off-hook condition. The ring trip network connects to these two inputs.
5 6	27 28	TIPX RINGX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relay).
7	2	BGND	Ground. Should be tied together with AGND (pin 18).
8	4	VCC	+5V power supply
9	5	RINGRLY	Ring relay driver output. Open collector. Sinks 50 mA to GND. Must be protected by external inductive kick-back diode.
10	6	VBAT	Battery supply voltage, -24V to -58V. Negative with respect to GND (pins 7, 18).
11	7	RSG	Saturation guard programming resistor, R_{SG}, connects from this terminal to VEE (pin 20). Refer to section Battery feed for detailed information.
12	8	E1	TTL compatible enable input. Enables desired detector to be gated to the $\overline{DET}$ (pin 14) output. Refer to section Enable inputs for detailed information.
13	9	E0	TTL compatible enable input. Enables the $\overline{DET}$ (pin 14) output when set to logic level low and disables the $\overline{DET}$ output when set to logic level high. Refer to section Enable inputs for detailed information.
14	11	$\overline{DET}$	Detector output. Inputs C1 (pin 16) and C2 (pin 15) together with enable inputs E0 (pin 13) and E1 (pin 12) select one of the three detectors to be connected to the DET output. A logic low at the enabled DET output indicates a triggered detector condition. The DET output is open collector with internal pull-up resistor (approximately 15 kΩ to VCC (pin 8)).
15 16	12 13	C2 C1	C1 and C2 are TTL compatible inputs controlling the SLIC operating states. Refer to section Control inputs for details.
17	14	RDC	Constant current feed is programmed by two resistors connected in series from this pin to the receive summing node (RSN, pin 19). The resistor junction point is decoupled to GND to isolate the ac signal components.
18	15	AGND	Ground. Should be tied together with BGND (pin 7).
19	16	RSN	Receive summing node. 1 000 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing from RINGX (pin 6) to TIPX (pin 5). Programming networks for constant current feed, two- wire impedance and receive gain connect to the receive summing node.
20	18	VEE	-5V power supply.
21	19	VTX	Transmit vf output. The ac voltage difference between TIPX (pin 5) and RINGX (pin 6), the ac metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one. The two-wire impedance programming network connects between VTX and RSN (pin 19).
22	20	HPT	Tip side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} capacitor connects to pin 1, HPR.
	3,10 17,24	VBAT VBAT	These pins marked VBAT are used for heat sinking and internally connected to VBAT.
	26 1	$TIPX_{Sense}$ $RINGX_{Sense}$	$TIPX_{Sense}$ and $RINGX_{Sense}$ are internally connected to TIPX and RINGX respectively. $TIPX_{Sense}$ and $RINGX_{Sense}$ are used during manufacturing, but require no connections in SLIC applications, i.e. leave open.

Functional Description and Applications Information

Transmission

General

A simplified ac model of the transmission circuits is shown in figure 9. Circuit analysis yields:

$$V_{TR} = V_{TX} + I_L \bullet 2R_F \qquad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{1000} \qquad (2)$$

$$V_{TR} = E_L - I_L \bullet Z_L \qquad (3)$$

where:

- V_{TX} is a ground referenced unity gain version of the ac metallic voltage between the TIPX and RINGX terminals.
- V_{TR} is the ac metallic voltage between tip and ring.
- E_L is the line open circuit ac metallic voltage.
- I_L is the ac metallic current.
- R_F is a fuse resistor.
- Z_L is the line impedance.
- Z_T determines the SLIC TIPX to RINGX impedance.
- Z_{RX} controls four- to two-wire gain.
- V_{RX} is the analog ground referenced receive signal.

Two-wire impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse resistors R_F, let:

$V_{RX} = 0$. Then from (1) and (2):

$$Z_{TR} = Z_T/1000 + 2R_F$$

Thus with Z_{TR} and R_F known:

$$Z_T = 1000 \bullet (Z_{TR} - 2R_F)$$

Example:

Calculate Z_T to make $Z_{TR} = 900\ \Omega$ in series with 2.16 µF. $R_F = 40\ \Omega$

$$Z_T = 1000 \bullet \left(900 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 40\right)$$

which yields:

$Z_T = 820\ k\Omega$ in series with 2.16 nF.

It is always necessary to have a high ohmic resistor in parallel with the capacitor. This gives a DC-feedback loop for low frequency which ensures stability and reduces noise.

Two-wire to four-wire gain

From (1) and (2) with $V_{RX} = 0$:

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F}$$

Four-wire to two-wire gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4\text{-}2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L}{Z_T/1000 + 2R_F + Z_L}$$

For applications where $Z_T/1000 + 2R_F$ is chosen to be equal to Z_L the expression for $G_{4\text{-}2}$ simplifies to:

$$G_{4\text{-}2} = -\frac{Z_T}{Z_{RX}} \bullet \frac{1}{2}$$

Four-wire to four-wire gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4\text{-}4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L + 2R_F}{Z_T/1000 + 2R_F + Z_L}$$

Hybrid function

The PBL 3762A SLIC forms a particularly flexible and compact line interface when used with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.

The hybrid function can also be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 10. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \ (E_L = 0)$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = -R_{TX} \bullet \frac{V_{RX}}{V_{TX}} =$$

$$= R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{Z_T/1000 + 2R_F + Z_L}{Z_L + 2R_F}$$

Example: calculate R_B for the line interface shown in figure 12.

$$R_B = 20 \bullet 10^3 \bullet \frac{261 \bullet 10^3}{523 \bullet 10^3} \bullet \frac{523 \bullet 10^3/1000 + 2 \bullet 40 + 600}{600 + 2 \bullet 40}$$

= 17.66 kΩ,(i.e. standard value 17.8 kΩ, 1%)

If calculation of the Z_B formula above yields a balance network containing an inductor, an alternate method is recommended. Contact Ericsson Components for assistance.

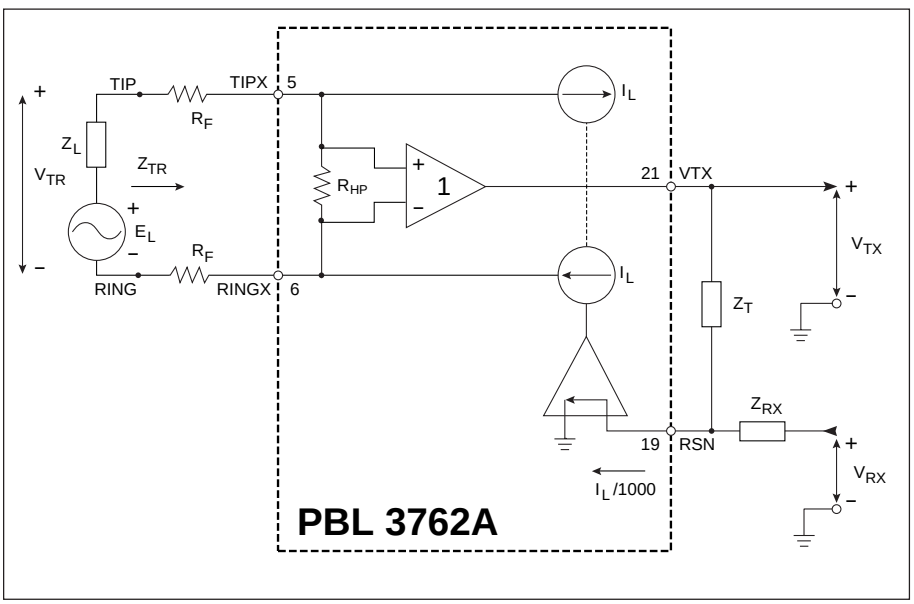


Figure 9. Simplified ac transmission circuit.

Longitudinal Impedance

A feed back loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range. This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal longitudinal reference voltage, V_{LoRef}.

$$V_{LoRef} = \frac{V_{Bat}}{2} = \frac{V_T + V_R}{2}$$

where V_T and V_R are tip and ring ground referenced voltags without any longitudinal component. As shown below, the SLIC appears as 20 Ω per wire to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission. Refer to figure 11.

Circuit analysis yields:

$$\frac{V_{Lo}}{R_{Lo}} = \frac{I_{Lo}}{1000}$$

which reduces to

$R_{LoT} = R_{LoR} = V_{Lo} / I_{Lo} = 20k\Omega/1000 =$ 20 Ω where:

R_{Lo} = 20 kΩ

$R_{LoT} = R_{LoR}$ = longitudinal resistance/wire

V_{Lo} = longitudinal voltage at TIPX, RINGX

I_{Lo} = longitudinal current

Capacitors C_{TC} and C_{RC}

The capacitors designated C_{TC} and C_{RC} in figure 12, connected between TIPX and ground as well as between RINGX and ground, are recommended as an addition to the overvoltage protection network. Very fast transients, appearing on tip and ring, may pass by the diode and SCR clamps in the overvoltage protection network, before these devices have had time to activate and could damage the SLIC. C_{TC} and C_{RC} short such very fast transients to ground. The recommended value for C_{TC} and C_{RC} is 2200 pF. Higher capacitance values may be used, but care must be traken to prevent degradation of either longitudinal balance or return loss. C_{TC} and C_{RC} contribute a metallic impedance of $1/(\pi \cdot f \cdot C_{RC}) \approx 1/(\pi \cdot f \cdot C_{TC})$, a TIPX to ground imped-ance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedanc of $1/(2 \cdot \pi \cdot f \cdot C_{RC})$.

Ac - dc Separation Capacitor, C_{HP}

The high pass filter capacitor connected between terminals 1 and 22 provides the separation between circuits sensing tip-ring dc conditions and circuits processing ac signals. A C_{HP} value of 10 nF will position the low end frequency response 3dB break point at 48 Hz (f_{3dB}) according to $f_{3dB} = 1/(2 \cdot \pi \cdot R_{HP} \cdot C_{HP})$ where$R_{HP} \approx$ 330 kΩ.

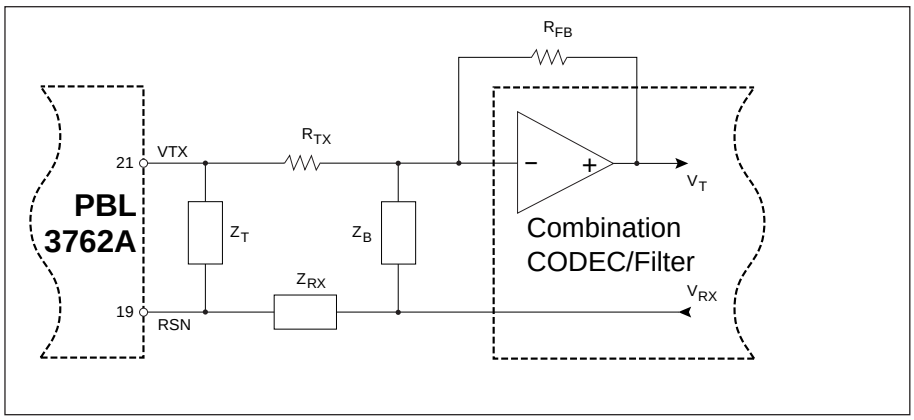


Figure 10. Hybrid function.

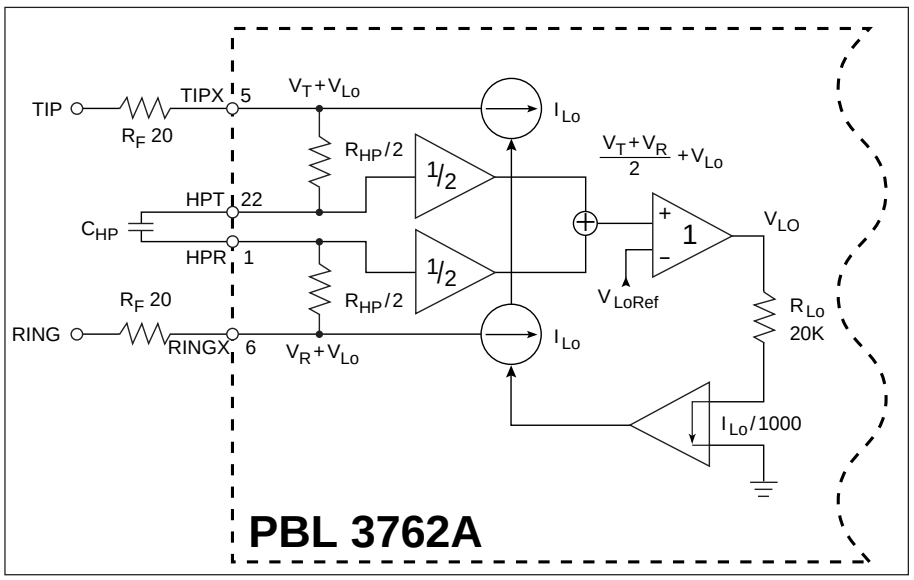


Figure 11. Longitudinal impedance.

Battery Feed

The block diagram in figure 13 shows the PBL 3762A battery feed system.

For a tip to ring dc voltage V_{TR} less than the saturation guard reference voltage V_{SGRef}, the SLIC emulates a resistive feed characteristic with an apparent battery voltage of 50 V. The apparent battery voltage is independent of the actual battery voltage, V_{Bat}, connected to the SLIC.

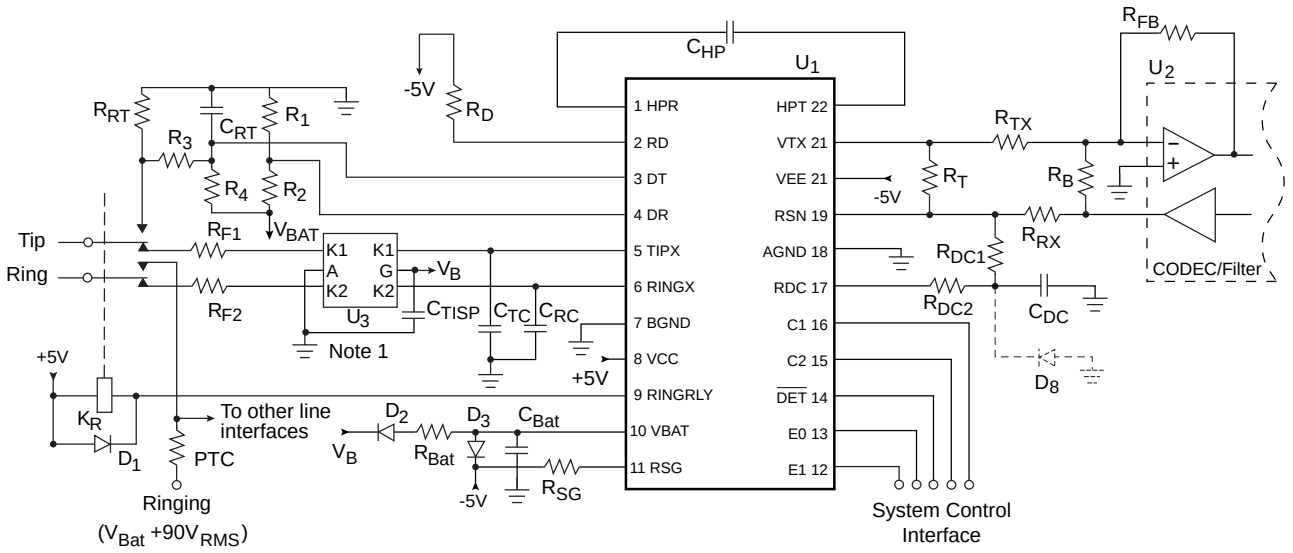
With the tip to ring dc voltage V_{TR} exceeding V_{SGRef}, the feed characteristic changes to a nearly-constant voltage feed. This is to prevent the tip and ring drive amplifiers from distorting the ac signal as might have otherwise occurred due to insufficient voltage margin between V_{TR} and V_{Bat} (pin 10). Thus the SLIC automatically adjusts the tip to ring dc voltage V_{TR} to the maximum safe value.

With the SLIC in the stand-by state (C1, C2= 1,1) a high resistance feed characteristic is enabled.

The following text explains the three battery feed cases in more detail.

Case 1: SLIC in the active state; $V_{TR} < V_{SGRef}$.

In the active state C1 = 0 and C2 = 1. In this operating state tip to ring voltages V_{TR} less than V_{SGRef} cause the block titled saturation guard (figure 13) to be disabled, i.e. its output is equal to zero. For this case circuit analysis yields:



U1	SLIC (Subscriber Line Interface Circuit) PBL 3762A	R_2	910 kΩ, 5%, 1/4 W	C_{Bat}	0.47 µF, 20%, $\|V_{Bat}\|$ + 20V
U2	Combination CODEC/Filter, e.g. TP3054 or programmable CODEC/ filter, e.g. SiCoFi	R_4	1.2 MΩ, 5%, 1/4 W	C_{DC}	3.3 µF, 20%, 10V
U3	Secondary protection (e.g. Texas Instruments TISP PBL 2)	R_{Bat}	5.1 Ω, 5%, 1/4 W	C_{HP}	0.010 µF, 20%, 100V
K_R	Relay, 2C contacts, 12V coil	R_B	17.8 kΩ, 1%, 1/4 W	C_{RT}	0.39 µF, 20%, 100V
D_1	Diode, 1N4454	R_D	39 kΩ, 5%, 1/4 W	C_{TC}, C_{RC}	2200 pF, 20%, 100V
D_2, D_3	Diode, e.g. 1N4004	R_{DC1}, R_{DC2}	20 kΩ, 5%, 1/4 W	C_{TISP}	220nF, 20%, 100V
R_{F1}, R_{F2}	Line resistor, 40 Ω, 1% match, Ericsson Components PBR 51XX	R_{FB}	24.3 kΩ, 1%, 1/4 W		
R_1, R_3	200 kΩ, 5%, 1/4 W	R_{RX}	261 kΩ, 1%, 1/4 W		
		R_{SG}	Short Circuit		
		R_T	523 kΩ, 1%, 1/4 W		
		R_{TX}	20 kΩ, 1%, 1/4 W		
		R_{RT}	150 Ω, 5%, 2 W		

Note 1: The ground terminals of the secondary protection should be connected to the ground terminal of the SLIC, and to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably a groundplane.

Figure 12. Single-channel subscriber line interface with PBL 3762A and combination CODEC/filter.

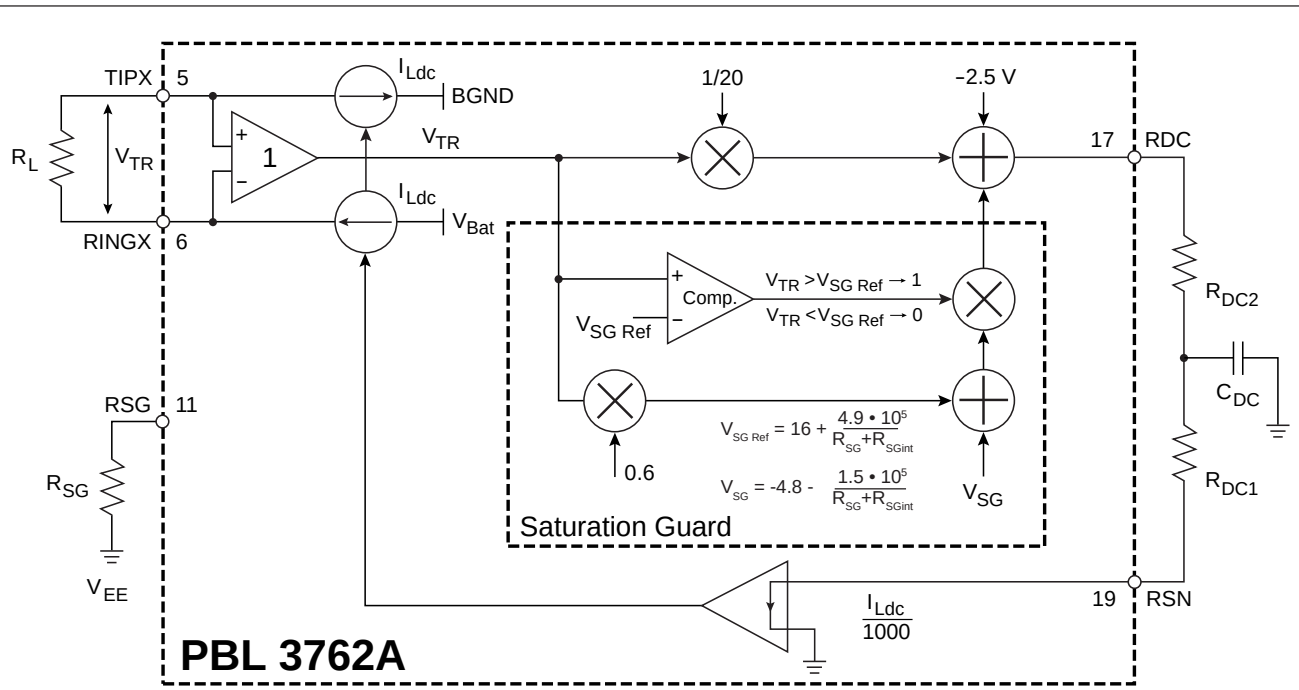


Figure 13. Battery feed (C1 ,C2= 0, 1; active state).

$$V_{TR} = 50 \bullet \frac{R_L}{R_L + R_{DC}/50} \quad \text{or,}$$

$$I_{Ldc} = \frac{50}{R_L + R_{Feed}}$$

where:

I_{Ldc} = the loop current

R_L = the line resistance

R_{DC} = (= R_{DC1} + R_{DC2}) the programming resistance which sets the equivalent feed resistance, $R_{Feed} = R_{DC}/50$

V_{TR} = the tip to ring dc metallic voltage

Note that for simplicity the fuse resistors R_F have not been included.

For tip to ring voltages V_{TR} less than V_{SGRef} the PBL 3762A thus emulates a resistive battery feed with 50 V apparent battery and a feed resistance, R_{Feed}, equal to $R_{DC}/50$.

Capacitor C_{DC} at the R_{DC1} - R_{DC2} common point removes vf signals from the battery feed control loop. C_{DC} is calculated according to:

$$C_{DC} = T \bullet \left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right), \text{ where T = 30ms}$$

Note that $R_{DC1} = R_{DC2}$ yields minimum C_{DC} value. For this case the feed resistance programming resistors can be calculated from $R_{DC1} + R_{DC2} = R_{Feed} \bullet 50$, where R_{Feed} is the desired feed resistance.

Case 2: SLIC in the active state; $V_{TR} > V_{SGRef}$

In the active state C1 = 0 and C2 = 1. The saturation guard reference voltage is user programmable according to:

$$V_{SGRef} = 16 + \frac{4.9 \bullet 10^5}{R_{SG} + R_{SGint}}$$

where:

R_{SG} = saturation guard reference programming resistor in Ω.

R_{SGint} = internal saturation guard reference programming resistor. R_{SGint} = 0Ω for PBL 3762A and R_{SGint} = 17.3 kΩ for PBL 3762A/4.

V_{SGRef} = saturation guard reference voltage in volts.

Once the dc metallic voltage, V_{TR}, exceeds the saturation guard reference voltage, V_{SGRef} , the saturation guard becomes active and the following expression describes the battery feed characteristic:

$$V_{TR} = \frac{(20.5 + 4.24 \bullet 10^5/(R_{SG}+R_{SGint})) \bullet R_L}{R_L + R_{DC}/350}$$

where R_{SGint}, R_L and V_{TR} have the same meaning as described above. The reduced apparent battery voltage limits the open circuit dc voltage to:

$$V_{TR} = 20.5 + \frac{4.24 \bullet 10^5}{R_{SG}+R_{SGint}}$$

For PBL 3762A/4 with R_{SG} = 0Ω, V_{TR} = 45V.The saturation guard ensures the line drive amplifiers of sufficient bias voltage at high R_L values or even at open loop by limiting the tip-to-ring dc voltage. Without this function, distortion of the vf signal would result. Of interest for some applications is, that the saturation guard permits on-hook (open loop) transmission. The function of the saturation guard is user-programmable through R_{SG}, which can be calculated from:

$$R_{SG} + R_{SGint} = \frac{4.24 \bullet 10^5}{\frac{(|V_{Bat}|-V_{Margin}) \bullet [R_{LMax}+(R_{DC1}+R_{DC2})/350]}{R_{LMax}} - 20.5}$$

which for $R_{LMax} \rightarrow \infty$ simplifies to:

$$R_{SG} + R_{SGint} = \frac{4.24 \bullet 10^5}{|V_{Bat}| - V_{Margin} - 20.5}$$

where

R_{LMax} = maximum loop resistance in Ω

V_{TRMax} = tip-to-ring dc voltage at maximum loop resistance in volts

V_{Margin} = $|V_{Bat}| - V_{TRMax}$ = 8V to allow distortion-free transmission of a $3.1V_{Peak}$ vf signal

Note that if the RSG terminal is left open, the tip-to-ring dc voltage will be limited to 20.5V.

In many applications a less than $3.1V_{Peak}$ maximum vf signal is satisfactory. In such applications, V_{Margin} may be set to less than 8V in accordance with the diagram shown in figure 14. The maximum tip-to-ring dc voltage will consequently be somewhat greater and a correspondingly longer loop can be accommodated.

Figure 15 illustrates three PBL 3762A battery feed curves. Note the knee where the saturation guard becomes active. The R_{SG} terminal is left open for these three curves, i.e. V_{SGRef} = 16 V. $R_{SG} = \infty$ is selected for operation with -28 V < V_{Bat} < -24 V. For other V_{Bat} values the knee can be transported along the R_L axis by calculation of R_{SG} as described in the text.

Figure 17 illustrates the power dissipation advantage of PBL 3762A line feed with V_{Bat} = -28 V over a conventional –48 V resistive feed.

Case 3: SLIC in the stand-by state.

In the stand-by state, C1 = 1 and C2 = 1. With the SLIC operating in the stand-by, power saving state the tip and ring drive amplifiers are disconnected and a high resistance battery feed is engaged. The loop current can be calculated from:

$$I_{Ldc} \approx \frac{V_{Bat} - 3\ V}{R_L + 1800\ \Omega}$$

where:

I_{Ldc} = the loop current

R_L = the loop resistance

V_{Bat} = the battery supply voltage

PBL 3762A battery feed in long loop applications

To feed a long loop, e.g. 2000 Ω, from a 50 V battery with a minimum of 16 mA to 18 mA demands a low feed resistance value. While the PBL 3762A is capable of meeting such requirements, two other

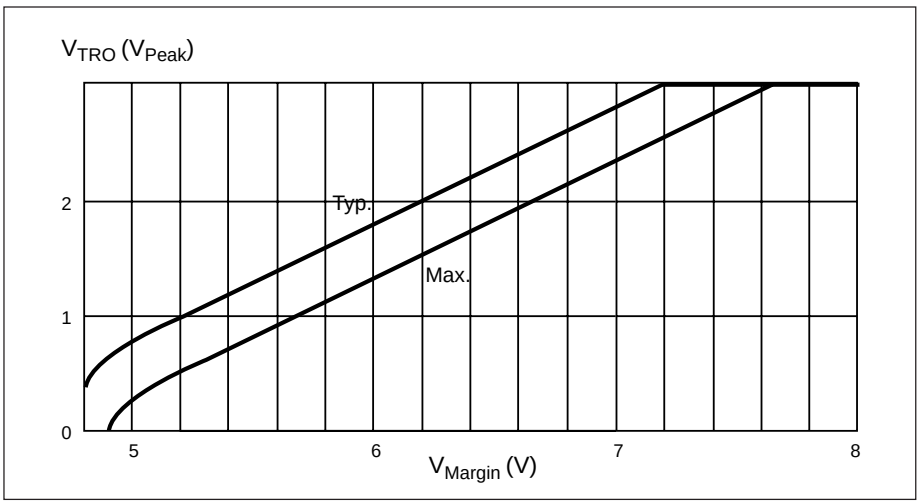


Figure 14. Overload level, V_{TRO} as a function of V_{Margin}.

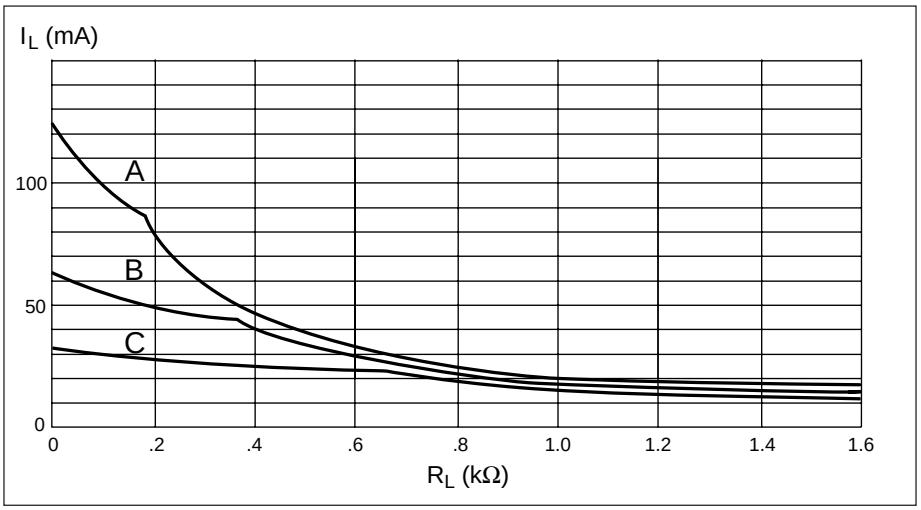


Figure 15. Examples of PBL 3762A loop feed. $R_{SG} \rightarrow \infty$, V_{Bat} = -28V.

$$R_L < \text{Knee} : I_L = \frac{50}{R_L + R_{DC}/50}$$

$$R_L > \text{Knee} : I_L = \frac{20.4}{R_L + R_{DC}/350} \quad (R_{SG} \rightarrow \infty)$$

Curve A: 2 • 200 Ω Feed
Curve B: 2 • 400 Ω Feed
Curve C: 2 • 800 Ω Feed

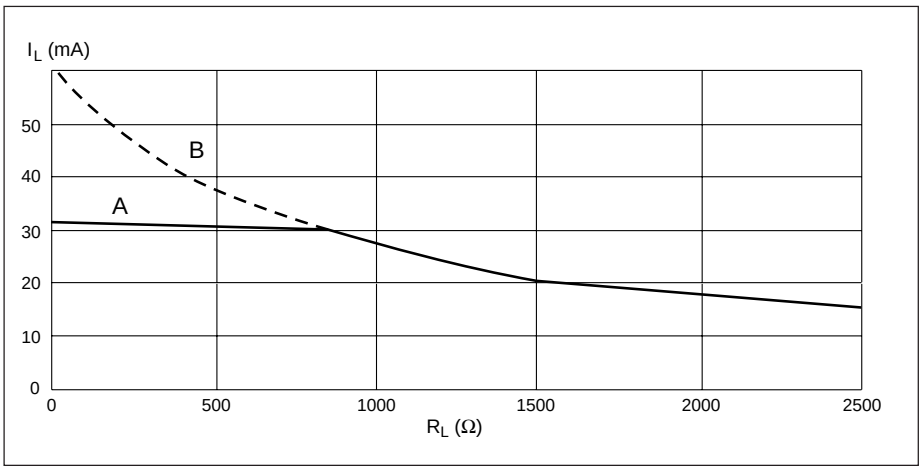


Figure 16. Example of PBL 3762A loop feed with current limiting.

Curve A: 50V apparent battery voltage
782 Ω + 40 Ω feed resistance
Current limited to 32 mA
$V_{SGRef} \approx 37V$

Curve B: 50V apparent battery voltage
782 Ω + 40 Ω feed resistance
Current not limited
$V_{SGRef} \approx 37V$

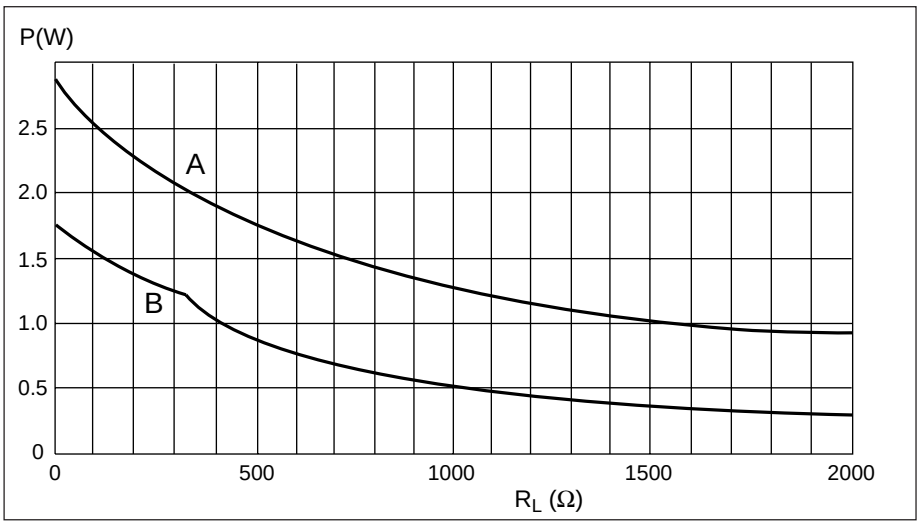


Figure 17. Power dissipation as a function of loop resistance, R_L.

Curve A: Conventional resistive feed:
-48V, 2 • 400Ω

Curve B: PBL3762A resistive feed:
-28V, 2 • 400Ω

parameters must be considered simultaneously: short loop SLIC power dissipation and vf signal amplitude at long loops.

The short circuit SLIC power dissipation, P_{ShTot}, caused by the loop current is

$$P_{ShTot} = I_{LSh} \bullet (|V_{Bat}| - I_{LSh} \bullet 2R_F) + P_3$$

where

V_{Bat} is the battery voltage connected to the SLIC at pin 10.

R_F is the fuse resistance, 40 Ω.

$$I_{LSh} = \frac{50}{(R_{DC1} + R_{DC2})/50 + 2R_F}$$

is the short circuit loop current

$(R_{DC1} + R_{DC2})/50$ is the feed resistance.

P_3 is the on-hook, active state power dissipation.

Note that a short circuited loop is not a normal operating condition. The terminating equipment will add some dc resistance (200 Ω to 300 Ω) even if the wire resistance is near 0 Ω.

If the total short circuit SLIC power dissipation, P_{ShTot}, exceeds the maximum allowable dissipation, P_{Max}, the short circuit loop current, I_{LSh}, must be limited. The maximum, safe short circuit current, I_{LShMax}, can be calculated from:

$$I_{LShMax} = \frac{V_{Bat}}{4R_F} - \left[\left(\frac{V_{Bat}}{4R_F}\right)^2 - \frac{P_{Max} - P_3}{2R_F}\right]^{1/2}$$

To comply with this requirement, the short circuit loop current can be limited by installing a diode (D_7 in figure 12) with its anode connected to ground and its cathode to the R_{DC1}, R_{DC2} common point. By clamping the voltage at R_{DC1}, the current flowing out of RSN (virtual ground) is limited and consequently the loop current is limited to $1000 \bullet (V_D/R_{DC1})$.

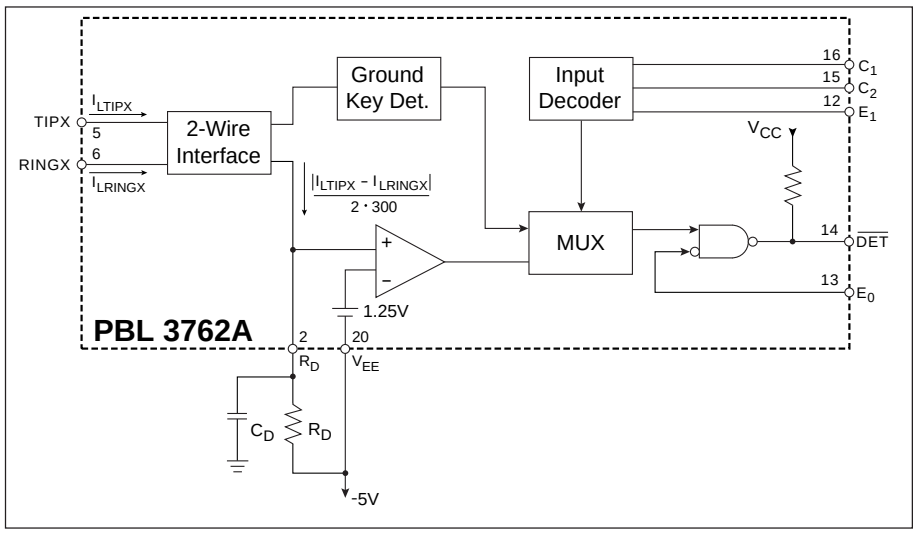


Figure 18. Loop current and ground key detectors.

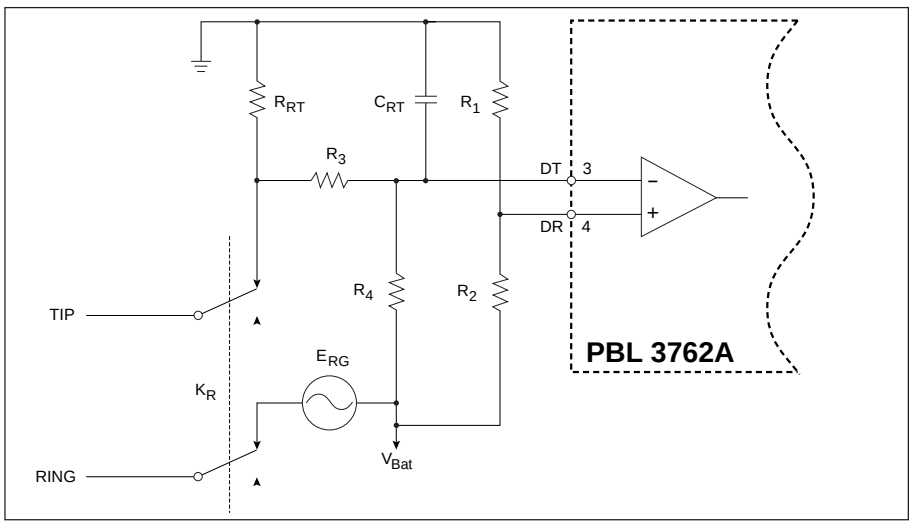


Figure 19. Ring trip network.

V_D is the voltage drop across the conducting diode; approximately 0.5V at the applicable current range. R_{DC1} and R_{DC2} can then be calculated from:

$$R_{DC1} = (1000 \bullet V_D)/I_{LShMax}$$

$$R_{DC2} = R_{Feed} \bullet 50 - R_{DC1}$$

Figure 16 illustrates a PBL 3762A battery feed curve with loop current limiting as described above. The battery feed is resistive for long loops and constant current for short loops.

To ensure that the maximum vf signal intended to be received/transmitted by the SLIC will not experience limiting in the TIPX (pin 5)/RINGX (pin 6) drive amplifiers at long loops, the saturation guard must be correctly programmed. Section "Battery Feed, Case 2" describes how to calculate a value for the saturation guard programming resistor R_{SG}.

Temperature Guard

A ring to ground short circuit fault condition as well as other improper operating conditions may cause excessive SLIC power dissipation. If junction temperature increases beyond 150°C, the temperature guard will trigger, causing the SLIC to be set to a high-impedance state. In this high-impedance state, power dissipation is reduced and the junction temperature will return to a safe value. Once below 150°C, the SLIC is returned back to its normal operating mode and will remain in that state, assuming the fault condition has been removed. As long as the temperature guard is triggered, the loop current detector will stay in active state.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status through a common output, $\overline{DET}$ (pin 14). The detector to be connected to $\overline{DET}$ is selected via the four bit wide control interface C1, C2, E0, E1. Please refer to section "Control Inputs" for a description of the control interface.

Loop Current Detector

The loop current value, at which the loop current detector changes state, is programmable by selecting the value of resistor R_D. R_D connects between pins RD (2) and VEE (20). Figure 18 shows a block diagram of the loop current detector. The two-wire interface produces

a current flowing out of pin RD (2):
$I_{RD} = |I_{LTIPX} - I_{LRINGX}|/600 = I_L/300$
where I_{LTIPX} and I_{LRINGX} are currents flowing into the TIPX and RINGX terminals and I_L is the loop current. The voltage generated by I_{RD} across the programming resistor R_D is compared to an internal 1.25 V reference. A logic low results at $\overline{DET}$ (pin 14), when I_{RD} exceeds the corresponding threshold current, $I_{RD} = I_{RDTh} = I_{LTh}/300$ and a logic high when $I_{RD} < I_{RDTh}$. The programming resistor can then be calculated as $R_D = 375/I_{LTh}$, when the desired threshold loop current I_{LTh} is known. R_D is in kΩ for I_{LTh} in mA. The filter capacitor is calculated according to $C_D = T_D/R_D$ with time constant $T_D = 0.5$ ms. Note that C_D may not be required if the $\overline{DET}$ output is software filtered.

Ground Key Detector

The ground key detector circuit examines the difference in TIPX and RINGX currents. Should the current difference exceed the threshold value, ΔI_{LOn}, the detector is triggered. As the current difference decreases the detector is reset at current threshold, $\Delta I_{LOff} . \Delta I_{LOn} > \Delta I_{LOff}$, i.e. the detector has hysteresis. The triggered detector results in a logic low at the $\overline{DET}$ (pin 14) output, assuming the ground key detector has been selected via the four-bit control input (C1, C2, E0, E1). For ΔI_{LOn} and ΔI_{LOff} numerical values please refer to table "Electrical Characteristics".

Ring Trip Detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT (pin 3) and DR (pin 4). The ringing source can be balanced or unbalanced superimposed on V_{Bat}. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no dc current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while the ring relay is energized, dc current flows and the comparator input voltage reverses polarity.

Figure 19 is an example of a ring-trip detection network. This network is applicable, when the ring voltage superimposed on V_{Bat} is injected on the ring lead of the two-wire port. The dc voltage across sense resistor R_{RT} is monitored by the ring trip comparator input DT via the network R_3, R_4 and C_{RT}. Input DR is set to a reference voltage by resistors R_1 and R_2. With the line on-hook (no dc current) DT is more positive than DR and the $\overline{DET}$ output will report logic level high, i.e. the detector is not tripped. When the line goes off-hook, while ringing, a dc current will flow through the loop, including the sense resistor, R_{RT}, and will cause input DT to become more negative than input DR. This changes output $\overline{DET}$ to logic level low, i.e. tripped detector condition. The system controller (or line card processor) responds by de-energizing the ring relay, i.e. ring trip.

Complete filtering of the 20 Hz ac component at terminal DT is not necessary. A toggling $\overline{DET}$ output can be examined by a software routine to determine the duty cycle. When the $\overline{DET}$ output is at logic level low for more than half the time, off-hook condition is indicated.

Relay Driver

The PBL 3762A SLIC incorporates a ring relay driver designed as open collector (npn) with a current sinking capability of 50 mA. The drive transistor emitter is connected to BGND. An external inductive kick-back clamp diode must be employed to protect the drive transistor.

Control Inputs

The PBL 3762A SLIC has two TTL compatible control inputs, C1 and C2. A decoder in the SLIC interprets the control input conditions and sets up the commanded operating state.

Open Circuit State (C1, C2 = 0, 0)

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum. No detectors are active.

Ringing State (C1, C2 = 1, 0)

The ring relay driver and the ring trip detector are activated. TIPX and RINGX

State	E0	E1	C1	C2	SLIC operating state	Active detector	$\overline{DET}$ Output
1	0	0	0	0	Open circuit	No active detector	Logic level high
2	0	0	0	1	Active	Ground key detector	Ground key status
3	0	0	1	0	Ringing	No active detector	Logic level high
4	0	0	1	1	Stand-by	Ground key detector	Ground key status
5	0	1	0	0	Open circuit	No active detector	Logic level high
6	0	1	0	1	Active	Loop current detector	Loop current status
7	0	1	1	0	Ringing	Ring trip detector	Ring trip status
8	0	1	1	1	Stand-by	Loop current detector	Loop current status
9	1	0	0	0	Open circuit	Note 1	Logic level high Note 1
10	1	0	0	1	Active		
11	1	0	1	0	Ringing		
12	1	0	1	1	Stand-by		
13	1	1	0	0	Open circuit		
14	1	1	0	1	Active		
15	1	1	1	0	Ringing		
16	1	1	1	1	Stand-by		

Table 1. SLIC operating states

Note 1 For operating states 9-16 active detectors are as for operating states 1-8. The $\overline{DET}$ output is, however, disabled and remains at logic level high regardless of detector status.

Note 2 For operating states 1-8 the $\overline{DET}$ output is enabled and will report the status of the active detector. Logic level low indicates a triggered detector.

are in the high impedance state and signal transmission is inhibited.

Active State (C1, C2 = 0, 1)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. Vf signal transmission is normal. Both the loop current and the ground key detectors are activated. Inputs E0 and E1 control the selection of one of these detectors to be gated to the $\overline{DET}$ output. Please, refer to section "Enable Inputs".

Stand-by State (C1, C2 = 1, 1)

In the stand-by state the line drive amplifiers are disconnected. The loop feed is converted to resistive form according to:

$$I_{Ldc} \approx \frac{V_{Bat} - 3\ V}{R_L + 1800\ \Omega}$$

where:

I_{Ldc} = the loop current (A)

V_{Bat} = the battery supply voltage (V)

R_L = the loop resistance (ohm)

The stand-by short circuit loop current (I_{LSh}) for V_{Bat} = -28 V is then limited to $I_{LSh} \approx 13.9$ mA.

Both the loop current and ground key detectors are activated in this operating state. Inputs E0 and E1 control the selection of one of these detectors to be gated to the $\overline{DET}$ output. Please, refer to section “Enable Inputs”.

Table 1 summarizes the above description of the control inputs.

Enable Inputs (E0, E1)

Two TTL-compatible enable inputs E0 (pin 13) and E1 (pin 12) control the function of the $\overline{DET}$ (pin 14) output.

E0, when set to logic level low, enables the $\overline{DET}$ output, which is a collector output with internal pull-up resistor (approx. 15 kΩ). A $\overline{DET}$ output at logic level low indicates triggered detector condition (loop current above threshold current, ground key depressed or telephone off-hook during the ringing cycle). A $\overline{DET}$ output at logic level high indicates a non triggered detector condition.

E0, when set to logic level high, disables the $\overline{DET}$ output; i.e. it appears as a resistor connected to V_{CC}.

E1, when set to logic level low, gates the ground key detector to the $\overline{DET}$ output.

E1, when set to logic level high, gates the loop or ring trip detector to the $\overline{DET}$ output.

Table 1 summarizes the above description of the enable inputs.

Overvoltage Protection

The PBL 3762A SLIC must be protected against overvoltages on the telephone line caused by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum allowable continuous and transient voltages that may be applied to the SLIC. The circuit shown in figure 12 utilizes series resistors together with a programmable overvoltage protector (e g Texas Instrument TISP PBL2), serving as a secondary protection.

The protection network in figure 12 is designed to meet requirements in ITU-T K20, Table 1.

The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i e the battery voltage,V_{Bat}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by an internal diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage on-state condition, clamping the overvoltage close to ground.

A gate decoupling capacitor, C_{TISP} is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. Without the capacitor even the low inductance in the track to the V_{Bat} supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F serve the dual purposes of being non- destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross. Ericsson Components AB offers a series of thick film resistors networks (e g PBR 51-series and PBR 53-series) designed for this application.

Also devices with a built in resetable fuse function is offered (e g PBR 52-series) including positive temperature coefficient (PTC) resistors, working as resetable fuses, in series with thick film resistors. Note that it is important to always use PTC´s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore the ability to protect the SLIC will be reduced.

If there is a risk for overvoltages on the V_{Bat} terminal on the SLIC, then this terminal should also be protected.

Power-up Sequence

The voltage at pin VBAT sets the substrate voltage, which must at all times be kept more negative than the voltage at any other pin to prevent possible latch-up. The optimal power-up sequence is ground and V_{Bat}, then other supplies and signal leads.

However, V_{CC} may be connected before V_{Bat}, and if the V_{Bat} supply voltage should be absent, a diode with a 2A current rating, connected with its cathode to V_{EE} and anode to V_{Bat} ,ensures the presence of the most-negative supply voltage at the VBAT pin. The VBAT pin should not be applied at a faster rate than corresponds to the time constant formed by a 5.1 Ω resistor in series with the VBAT pin and a 0.47 µF capacitor from the VBAT pin to ground. This RC network may be shared by several SLICs.

Printed Circuit Board Lay-out

Care in PCB lay-out is essential for proper PBL 3762A function. The components connecting to the RSN pin (19) should be in close proximity of that pin such that no interference is injected into the RSN terminal. Ground plane surrounding the RSN pin is advisable.

The two ground pins AGND and BGND should be connected together on the PCB at the device location.

Ordering Information

Package	Temp. Range	Part No.
Ceramic DIP	-40 to 85°C	PBL 3762AJ
Ceramic DIP	-40 to 85°C	PBL 3762A/4J
PLCC	-40 to 85°C	PBL 3762AQN
PLCC	-40 to 85°C	PBL3762A/4QN

Specifications subject to change without notice.

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