ERICSSON

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PBL 3798/6
Subscriber Line Interface Circuit

Description

PBL 3798/6 is an analog Subscriber Line Interface Circuit (SLIC), which is fabricated in a 75 V bipolar, monolithic process.

PBL 3798/6 has a programmable, constant current feed. A stand-by state reduces idle power dissipation, while allowing the supervisory functions to be active.

Tip-ring polarity is reversible without altering SLIC supervisory and voice frequency (vf) functions. Tip and ring outputs can be set to high impedance states. These and other operating states are activated via a parallel, four bit control word.

An external resistor controls the off-hook detector threshold current. The ring trip detector can operate with both balanced and unbalanced ringing systems. The two detectors are read via a shared output.

Ring and test relay drivers with internal clamp diodes are provided.

The complex or real two-wire impedance is set by a scaled, lumped element network.

Two- to four-wire and four- to two-wire signal conversion is provided by the SLIC in conjunction with either a conventional or a programmable CODEC/filter.

Longitudinal line voltages are suppressed by a control loop within the SLIC.

The PBL 3798/6 package is 32-pin plastic j-leaded chip carrier.

Key Features

- Programmable, constant current feed
- Tip-ring polarity reversal function
- Tip and ring open circuit state
- Detectors:
  - programmable loop current detector
  - ring trip detector
- Ring and test relay drivers
- Line terminating impedance, complex or real, set by a simple external network
- Hybrid function with conventional or programmable CODEC/filters
- 70 dB longitudinal to metallic balance
- Idle noise < 7 dBrnC; <-83 dBup
- Programmable open loop voltage

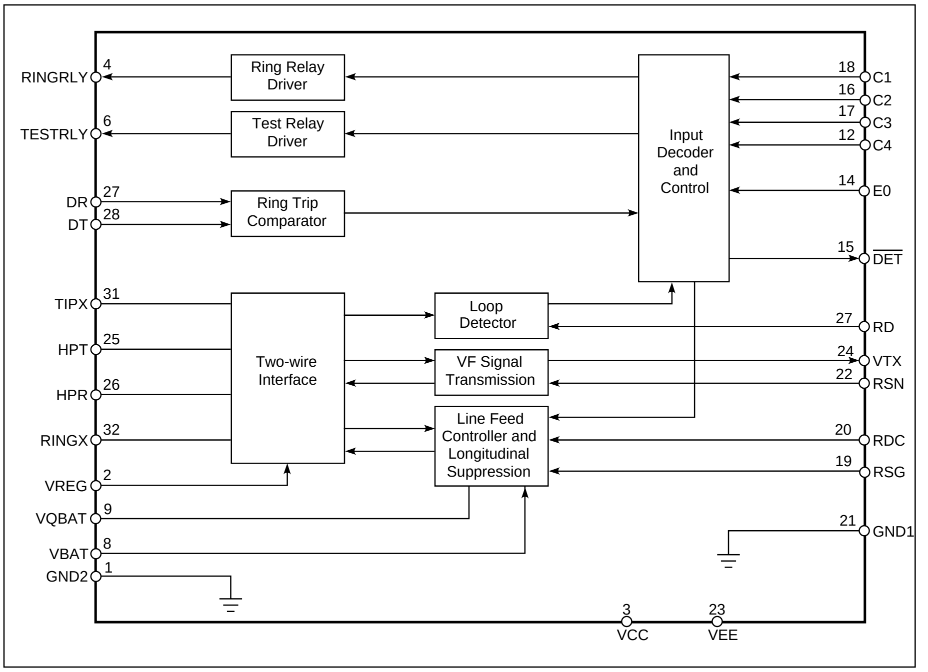
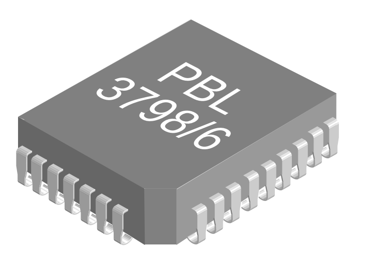


Figure 1. Block diagram.



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature and Humidity				
Storage temperature range	T_{Stg}	-55	+150	°C
Operating ambient temperature range	T_{Amb}	-40	+85	°C
Operating junction temperature range (Note 1)	T_j	-40	+135	°C
Power Supply				
V_{CC} with respect to ground	V_{CC}	-0.4	+6.5	V
V_{EE} with respect to ground	V_{EE}	-6.5	+0.4	V
V_{Bat} with respect to ground	V_{Bat}	-70	+0.4	V
Power Dissipation				
Continuous power dissipation at T_{Amb} = 70 °C				
32-pin, j-leaded chip carrier (RN)			1.7	W
Ground				
Voltage between GND1 and GND2 (Note 4)		-0.1	+0.1	V
Relay Drivers				
Test relay supply voltage	V_{TRly}	V_{Bat}	V_{CC}	V
Ring relay supply voltage	V_{RRly}	V_{Bat}	V_{CC}	V
Test relay current	I_{TRly}		80	mA
Ring relay current	I_{RRly}		80	mA
Ring Trip Comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	0	V
Input current, t_p = 10 ms	I_{DT}, I_{DR}	-2	+2	mA
Digital Inputs, Outputs C1 - C4, E0, $\overline{DET}$				
Input voltage	V_{ID}	-0.4	V_{CC}	V
Output voltage (DET not active)	V_{OD}	-0.3	V_{CC}	V
Output current	I_{OD}		3	mA
TIPX and RINGX Terminals				
TIPX or RINGX continuous voltage (Notes 5, 6)	V_T, V_R	-70	1	V
TIPX or RINGX, pulsed voltage, t_w < 10 ms and t_{rep} > 10 s (Notes 5, 6)	V_T, V_R	-70	5	V
TIPX or RINGX, pulsed voltage, t_w < 1 µs and t_{rep} > 10 s (Notes 5, 6)	V_T, V_R	-90	10	V
TIPX or RINGX, pulsed voltage, t_w < 250 ns and t_{rep} > 10 s (Notes 5, 6, 7)	V_T, V_R	-120	15	V
TIPX or RINGX current	I_{Ldc}	-105	105	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	0	70	°C
Case temperature	T_{Case}	0	90	°C
V_{CC} with respect to ground	V_{CC}	4.75	5.25	V
V_{EE} with respect to ground	V_{EE}	-5.25	-4.75	V
V_{Bat} with respect to ground (Notes 8, 9, 11)	V_{Bat}	-58	-40	V
GND2 with respect to GND1 (Note 10)	V_{G12}	0	0	V

Notes

1. The circuit includes thermal protection. Refer to section Over-temperature protection. Operation above 135 °C may degrade device reliability.
4. The GND1 and GND2 pins should be connected together via a direct printed circuit board trace.
5. V_T and V_R are referenced to ground. t_w is pulse width of a rectangular test pulse and t_{rep} is pulse repetition rate.
6. These voltage ratings require a diode to be installed in series with the VBAT pin as shown in figure 10 (D_7).
7. R_{F1}, $R_{F2} \geq 20$ ohms is also required. Pulse supplied to TIP and RING outside R_{F1}, R_{F2}.
8. The saturation guard reference voltage, V_{SGRef}, should be adjusted by calculating a value for resistor R_{SG} as described in the text.
9. V_{Bat} should be applied with a $\partial V_{Bat}/\partial t < 4$ V/µsec. A time constant of 2.6 µs is suggested (e.g. 5.6 ohms and 0.47 µF). The VBAT terminal must at all times be at a lower potential than any other terminal to maintain proper junction isolation. Refer to section Power-up sequence.
10. GND1 and GND2 must be connected before supply voltages.
11. A V_{Bat} of maximum -40 V may be used. However this requires that R_{SG} is set open circuit, otherwise the performance on long lines will degrade outside the specified limits.

Electrical Characteristics

0 °C ≤ T_{Amb} ≤ 70 °C, V_{CC} = +5 V ±5%, V_{EE} = -5V ±5%, -58 V ≤ V_{Bat} ≤ -46 V, GND1 = GND2, Z_{TR} (2-wire ac terminating impedance) = 600 Ω, Z_L (line impedance) = 600 Ω, R_{F1} = R_{F2} = 0 Ω, R_T = 60 kΩ, R_{RX} = 30 kΩ, R_{DC1} = R_{DC2} = 5 kΩ, R_{SG} = ∞, R_D = 57.5 kΩ, R_{Bat} = 10 Ω, C_{HP} = 0.22 µF, C_{DC} = 0.22 µF, C_D = 0.01 µF, C_{TC} = C_{RC} = 2200 pF, C_{Flt} = 0.47 µF, C_{Bat} = 0.47 µF, unless otherwise specified. The specifications are with respect to exact external component values.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
2-wire port						
Overload level, V_{TRO}	2	1% THD, E_L = 0, f = 1 kHz,	3.1	3.5		V_{Pk}
		(Note 1)	9.0	10.1		dBm
			9.0	10.1		dBu
Input impedance, Z_{TRX}						
Longitudinal impedance, Z_{LoT}, Z_{LoR}	3	f ≤ 100 Hz		25	40	Ω/wire
Longitudinal current limit, I_{LoT}, I_{LoR}		f ≤ 100 Hz				
		Active state	20	28		mA_{rms}/wire
		Stand-by state	8.5	19		mA_{rms}/wire
Longitudinal to metallic balance, B_{LM}		IEEE Standard 455-1985				
		0.2kHz < f < 3.4kHz, Note 4				
		Normal polarity	50	70		dB
		Reversed polarity		65		dB

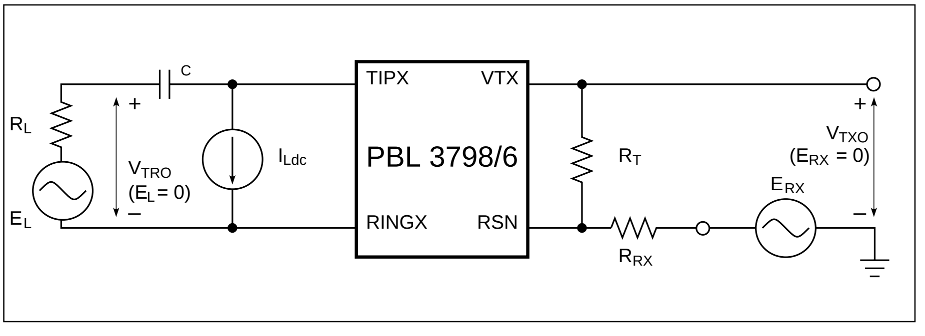


Figure 2. Overload level.
$1/\omega C \ll R_L$, R_L = 600 Ω,
R_T = 60 kΩ, R_{RX} = 30 kΩ.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Metallic to longitudinal balance, B_{ML}		FCC part 68 paragraph 68.310				
		0.2kHz < f < 4.0kHz	40			dB
		f = 1.0kHz		53		dB
Longitudinal to metallic balance, B_{LME}	4	0.2kHz < f < 3.4kHz, $B_{LME} = 20 \cdot \log \left\lvert \frac{E_{Lo}}{V_{TR}} \right\rvert$				
		Normal polarity	50	70		dB
		Reversed polarity		65		dB
Longitudinal to four wire balance, B_{LFE}	4	0.2kHz < f < 3.4kHz, $B_{LFE} = 20 \cdot \log \left\lvert \frac{E_{Lo}}{V_{TX}} \right\rvert$				
		Normal polarity	50	70		dB
		Reversed polarity		65		dB
Metallic to longitudinal balance, B_{MLE}	5	$B_{MLE} = 20 \cdot \log \left\lvert \frac{E_{TR}}{V_{Lo}} \right\rvert$, $E_{RX} = 0$				
		0.2kHz < f < 4.0kHz	40			dB
		f = 1.0 kHz		53		dB
Four wire to longitudinal balance, B_{FLE}	5	$B_{FLE} = 20 \cdot \log \left\lvert \frac{E_{RX}}{V_{Lo}} \right\rvert$, E_{TR} source removed				
		0.2kHz < f < 4.0kHz	40			dB
		f = 1.0 kHz		53		dB

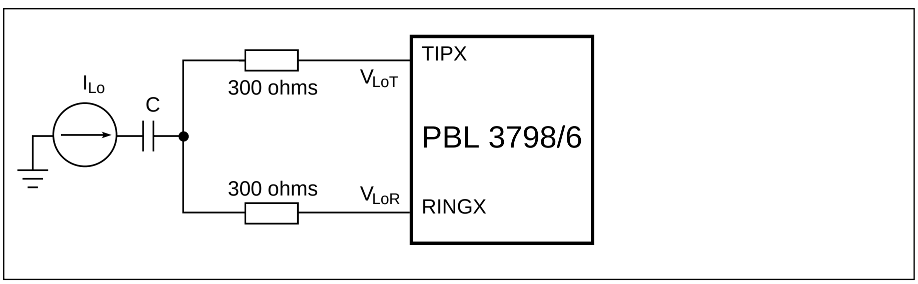


Figure 3. Longitudinal input impedance.

$$Z_{LoT} = Z_{LoR} = \frac{V_{LoT} + V_{LoR}}{I_{Lo}}$$

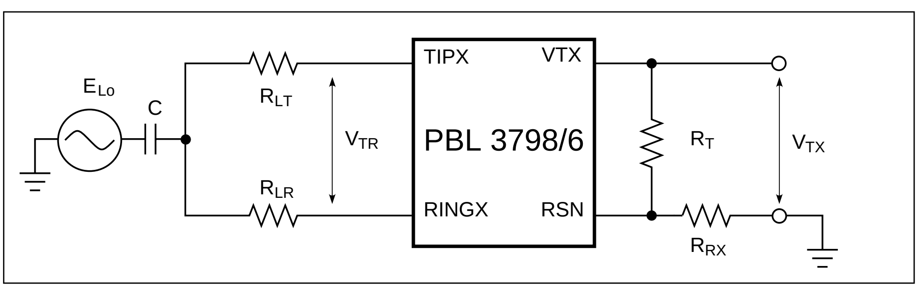


Figure 4. Longitudinal-to-metallic (B_{LME}) and Longitudinal-to-four-wire (B_{LFE}) balance.
$1/\omega C \ll 150\ \Omega$,
$R_{LT} = R_{LR} = 300\ \Omega$, $R_T = 60\ k\Omega$,
$R_{RX} = 30\ k\Omega$.

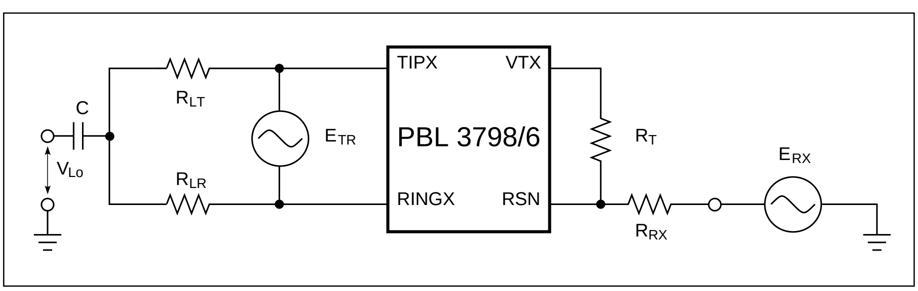


Figure 5. Metallic-to-longitudinal (B_{MLE}) and four-wire-to-longitudinal (B_{FLE}) balance.
$1/\omega C \ll 150\ \Omega$,
$R_{LT} = R_{LR} = 300\ \Omega$, $R_T = 60\ k\Omega$,
$R_{RX} = 30\ k\Omega$.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
2-wire return loss, r		$r = 20 \bullet \log \left\| \frac{Z_L + Z_{TR}}{Z_L - Z_{TR}} \right\|$, Note 5				
		$0.2kHz \le f < 0.5kHz$	30	32		dB
		$0.5kHz \le f < 1.0kHz$	25	27		dB
		$1.0kHz \le f \le 3.4kHz$	15	17		dB
Polarity reversal time, t_{pol}		Normal to reversed polarity or reversed to normal polarity		4	15	ms
TIPX idle voltage, V_{Ti}		Normal polarity, stand-by				
		V_{Bat} = -48V	-5.0	-3.5	-2.0	V
TIPX to RINGX idle voltage, V_{Tro}		Active and standby				
		V_{Bat} = -48V, R_l = open loop				
		Normal polarity	32	35	38	V
		Reversed polarity	-38	-35	-32	V
4-wire Transmit Port (VTX)						
Overload level, V_{TXO}	2	Load impedance > 20 kΩ,	3.1	3.5		V_{Pk}
		f = 1 kHz, 1% THD, E_{RX} = 0	9.0	10.1		dBu
		Note 7				
Output offset voltage, ΔV_{TX}			-50	±5	+50	mV
Output impedance, z_{TX}		$0.2kHz \le f \le 3.4kHz$		10	20	Ω
4-wire Receive Port (RSN)						
RSN dc voltage, V_{RSN}		I_{RSN} = 0	-10	0	+10	mV
RSN impedance, z_{RSN}		$0.2kHz \le f \le 3.4kHz$		3	20	Ω
RSN current (I_{RSN}) to metallic loop current (I_L) gain, α_{RSN}		$0.2kHz \le f \le 3.4kHz$, $\alpha_{RSN} = \frac{I_L}{I_{RSN}}$		40		dB
Frequency Response						
Two-wire to four-wire, g_{2-4}	6	$0.3kHz \le f \le 3.4kHz$ Relative to 1.0 kHz, 0 dBu E_{RX} = 0 V, (Notes 2, 8)	-0.1	±0.03	+0.1	dB
Four-wire to two-wire, g_{4-2}	6	$0.3kHz \le f \le 3.4kHz$ Relative to 1.0 kHz, 0 dBu E_L = 0 V, (Notes 2, 9)	-0.1	±0.03	+0.1	dB
Four-wire to four-wire, g_{4-4}	6	$0.3kHz \le f \le 3.4kHz$ Relative to 1.0 kHz, 0 dBu E_L = 0 V, (Notes 2, 9)	-0.1	±0.06	+0.1	dB
Insertion Loss						
Two-wire to four-wire, G_{2-4}	6	0 dBu, 1 kHz, E_{RX} = 0 (Notes 8, 10)	-0.15	±0.1	+0.15	dB
Four-wire to two-wire, G_{4-2}	6	0 dBu, 1 kHz, E_L = 0 (Notes 9, 10)	-0.15	±0.1	+0.15	dB
Four-wire to four-wire, G_{4-4}	6	0 dBu, 1 kHz, E_L = 0 (Notes 9, 10)	-0.15	±0.1	+0.15	dB

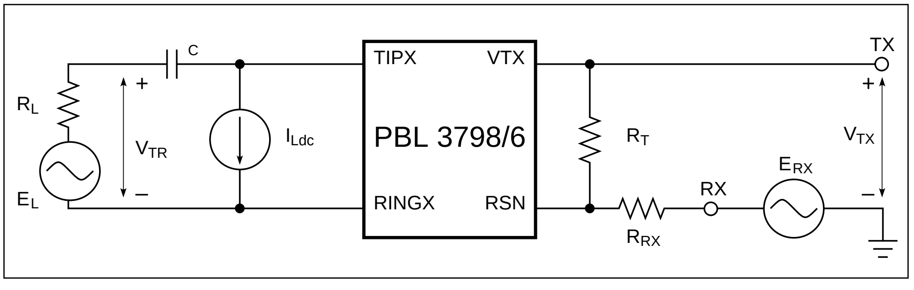


Figure 6. Frequency response, insertion loss, gain tracking, idle channel noise, THD, inter-modulation.
$1/\omega C \ll R_L$, R_L = 600 Ω, R_T = 60 kΩ, R_{RX} = 30 kΩ.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Gain Tracking						
Two-wire to four-wire (Note 8) and Four-wire to two-wire (Note 9)	6	Referenced to -10 dBu, 1 kHz				
		+3 dBu to -30 dBu	-0.1		+0.1	dB
		-30 dBu to -55 dBu		±0.1		dB
Noise						
Idle channel noise at two-wire (TIPX-RINGX) or four-wire (VTX) port	6	$E_{RX} = E_L = 0$, Notes 2, 11				
		C-msg weighting		7	10	dBrnC
		Psophometrical weighting		-83	-80	dBup
Total Harmonic Distortion						
Two-wire to four-wire, Four-wire to two-wire	6	$0.3kHz \leq f \leq 3.4kHz$ 0 dBu, 1 kHz test signal, Note 2		-64	-50	dB
Battery Feed Characteristics						
Loop current in constant current region, $\|I_{Ldc}\|$	14	$R_{DC1} = R_{DC2} = 5\ k\Omega$ Active state p = 1, Active polarity reversal state p = -1 $I_{Ldc} = p \bullet \frac{250}{R_{DC1} + R_{DC2}}$	22	25	28	mA
		Stand-by state p = 1 Stand-by polarity reversal state p = -1 $I_{Ldc} = p \bullet \frac{125}{R_{DC1} + R_{DC2}}$	10	12.5	15	mA
Loop current in constant current region at maximum loop resistance, $\|I_{Ldc}\|$	14	$R_{DC1} = R_{DC2} = 5\ k\Omega$ Active state $V_{Bat} = -48$ V, $R_{Lmax} = 1400\ \Omega$ Note 13	22			mA
Loop current outside constant current region, $\|I_{Ldc}\|$	14	$R_{DC1} = R_{DC2} = 5\ k\Omega$ Active state $V_{Bat} = -40{,}5$ V, $R_{Lmax} = 1880\ \Omega$ Note 13	18			mA
Loop Current Detector						
Loop current detector conversion factor On-hook to off-hook, K_{LThOff}		$I_{LThOff} = K_{LThOff}/R_D$ Active, standby, polarity reversal state (Note 14)	395	465	535	V
Loop current detector conversion factor Off-hook to on-hook, K_{LThOn}		$I_{LThOn} = K_{LThOn}/R_D$ Active, standby, polarity reversal state (Note 14)	348	410	472	V
Loop current detector conversion factor hysteresis, K_{LTh}		Active, standby and Polarity reversal state (Note 15)	20	55	90	V
Dial pulse distortion		10 pps, Off-hook: 600 Ω On-hook: ∞ Ω		1	5	%
Ring Trip Comparator Inputs (DT, DR)						
Offset voltage, ΔV_{DTR}	7	$V_{Bat} + 2\ V < V_{DT}, V_{DR} < -2\ V$				
		R = 0 Ω	-20	±10	20	mV
		R = 200 kΩ	-40	±10	40	mV
Input offset current, ΔI_B	7	$V_{Bat} + 2\ V < V_{DT}, V_{DR} < -2\ V$, R = 200 kΩ		0.05	1	µA
Input bias current, I_B	7	$V_{Bat} + 2\ V < V_{DT}, V_{DR} < -2\ V$, R = 200 kΩ $I_B = (I_{DT} + I_{DR})/2$		0.1	1	µA
Input resistance		$V_{Bat} + 2\ V < V_{DT}, V_{DR} < -2\ V$				
unbalanced, R_{DT}, R_{DR}			1			MΩ
balanced, R_{DTR}			3			MΩ
Common mode range, V_{DT}, V_{DR}			V_{Bat}+2		-2	V

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Relay Driver Outputs (RINGRLY, TESTRLY)						
On state voltage, V_{TRly}, V_{RRly}		I_{TRly}, I_{RRLy} = 25 mA				
		0°C < T_{Amb} < 25°C	V_{CC}-2.0	V_{CC}-1.8		V
		25°C < T_{Amb} < 70°C	V_{CC}-1.8	V_{CC}-1.6	V_{CC}-1.0	V
Off state leakage current, I_{TRly}, I_{RRLy}		V_{TRly}, V_{RRly} = V_{Bat}		5	100	µA
Clamp voltage		I_{TRly}, I_{RRLy} = 25 mA	V_{Bat}-3		V_{Bat}-1	V
Digital Inputs (C1-C4, E0)						
Input low voltage, V_{IL}					0.8	V
Input high voltage, V_{IH}			2.0			V
Input low current, I_{IL}		V_{IL} = 0.4 V	-0.4			mA
Input high current, I_{IH}		V_{IH} = 2.4 V			40	µA
Digital Output ($\overline{DET}$)						
Output low voltage, V_{OL}		I_{OL} = 1.0 mA			0.45	V
Output high voltage, V_{OH}		I_{OH} = -0.1 mA	2.4			V
Resistive pull-up			12	15	18	kΩ
Power Supply Rejection Ratio (PSRR)						
V_{CC} to two-wire port and V_{CC} to four-wire port rejection ratio, $PSRR_{CC}$		50 Hz < f < 4 kHz	35			dB
		4 kHz < f < 50 kHz	30			dB
		Note 17				
V_{EE} to two-wire port and V_{EE} to four-wire port rejection ratio, $PSRR_{EE}$		50 Hz < f < 4 kHz	10			dB
		4 kHz < f < 50 kHz	0			dB
		Note 17				
V_{Bat} to two-wire port and V_{Bat} to four-wire port rejection ratio, $PSRR_{Bat}$		50 Hz < f < 4 kHz	25			dB
		4 kHz < f < 50 kHz	20			dB
		Note 17				
Power Supply Currents (relay drivers off)						
V_{CC} supply current, I_{CC}		On- or off-hook, active state		8	12	mA
V_{EE} supply current, $\lvert I_{EE}\rvert$		On- or off-hook, active state		6	9	mA
V_{Bat} supply current, $\lvert I_{Bat}\rvert$		On-hook, active state		3.5	6	mA
Power Dissipation						
On-hook total dissipation, P_{OnOp}		V_{Bat} = -48 V, Open circuit state		60	100	mW
On-hook total dissipation, P_{OnSb}		V_{Bat} = -48 V, Stand-by state		190	260	mW
On-hook total dissipation, P_{OnAct}		V_{Bat} = -48 V, Active state		225	300	mW
Off-hook total dissipation, P_{Off68}		V_{Bat} = -48 V, Active state			1200	mW
		R_L = 600 Ω, R_{DC1} = R_{DC2} = 5 kΩ				
		Note 18, Note 20				
Temperature Guard						
Junction temperature at threshold, T_{JG}				140		°C
Temperature guard hysteresis, ∂T_{JG}				10		°C

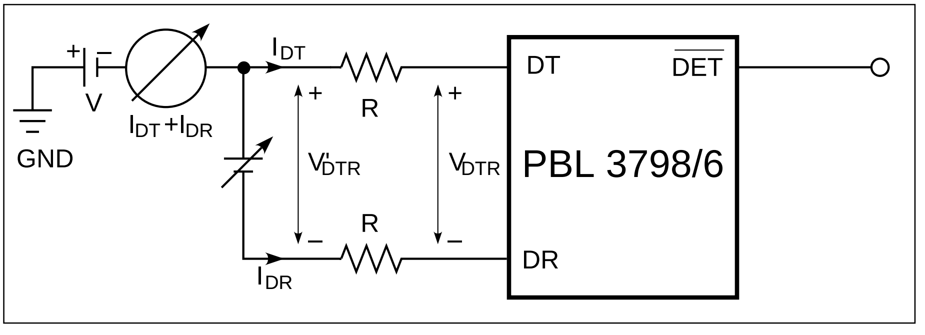


Figure 7. Ring trip comparator.

$2V < V < |V_{Bat} + 2|$,

$$\frac{I_{DT} + I_{DR}}{2} = I_B$$

$$V_{DTR} = \Delta V_{DTR}$$

$$\Delta I_B = \frac{V'_{DTR} - V_{DTR}}{R}$$

Notes

1. The overload level is specified at the two-wire port with the signal source at the four-wire receive port, i.e. $E_L = 0$ in figure 2.
2. dBm is the ratio between power level P and a 1 mW reference power level, expressed in decibels, i.e.

   $$dBm = 10 \bullet \log_{10} \frac{P}{1\ mW}$$

   dBu is the ratio between voltage Vrms and a 0.775 Vrms reference, expressed in decibels, i.e.

   $$dBu = 20 \bullet \log_{10} \frac{Vrms}{0.775\ Vrms}$$

   dBu = dBm at impedance level 600 Ω

   dBv is the ratio between voltage V and a 1 V reference, expressed in decibels, i.e.

   $$dBv = 20 \bullet \log_{10} \frac{V}{1\ V}$$

   dBup is the ratio between voltage V_p, measured via a psophometrical filter and a 0.775 Vrms reference, expressed in decibels, i.e.

   $$dBup = 20 \bullet \log_{10} \frac{V_p}{0.775\ Vrms}$$

   dBrnC is the ratio between power level P_C, measured via a C-message filter and a 1 pW reference power level, expressed in decibels, i.e.

   $$dBrnC = 10 \bullet \log_{10} \frac{P_C}{1\ pW}$$

3. The two-wire impedance, Z_{TRX}, is programmable by selection of external component values according to:

   $Z_{TRX} = Z_T / (G_{2-4} \bullet \alpha)$

   where:

   Z_{TRX} = impedance between the TIPX and RINGX terminals

   Z_T = programming network between the VTX and RSN terminals

   G_{2-4} = TIPX-RINGX to V_{TA} gain, nom. = 1 (0 dB ±0.15 dB)

   α = receive current gain, nominally = 100 (40 dB ±0.15 dB)

   The fuse resistors R_F add to the impedance presented by the SLIC at terminals TIPX and RINGX for a total two-wire impedance of $Z_{TR} = Z_{TRX} + 2R_F$.
4. Normal polarity is defined as the tip lead being at a more positive potential than the ring lead. Reversed polarity is defined as the ring lead being at a more positive potential than the tip lead.
5. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistor, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground. For R_T = 60 kΩ the capacitance value is approximately 330 pF.
7. The overload level, V_{TXO}, is specified at the four-wire transmit port, VTX, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2-4} = 1$.
8. The level is specified at the two-wire port.
9. The level is specified at the four-wire receive port (RX).
10. Fuse resistors R_{F1} and R_{F2} impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for $R_{F1} = R_{F2} = 0\ \Omega$.
11. The two-wire idle noise is specified with the port terminated in 600 Ω (R_L) and with the four-wire receive port grounded ($E_{RX} = 0$, $E_L = 0$; see figure 6).

    The four-wire idle noise at VTX is specified with the two-wire port terminated in 600 Ω (R_L). The four-wire receive port is grounded ($E_{RX} = 0$, $E_L = 0$; see figure 6).

    The idle channel noise degrades by approximately 5 dB when the saturation guard is active. Refer to section Battery feed for a description of the saturation guard.
13. Refer to section Battery Feed, Case 2.
14. Refer to Loop Monitoring Function, Loop current detector-active state.
15. The loop current detector threshold hysteresis is a function of the R_D value. Refer to note 14 above.
17. Power supply rejection ratio test signal is 100 mVrms (sinusoidal).
18. Fuse resistor $R_{F1} = R_{F2} = 0\ \Omega$.

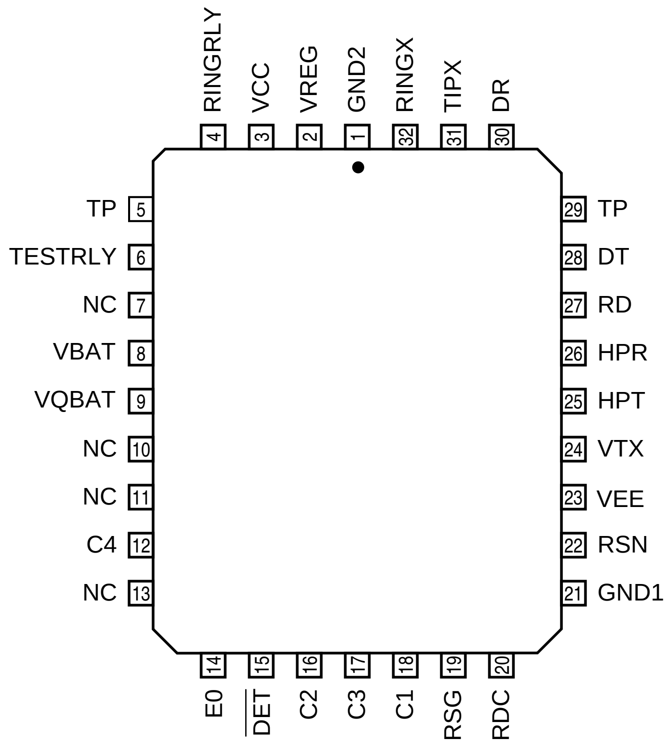


Figure 8. Pin configuration, 32-pin j-leaded chip carrier, Top view.

Pin Description

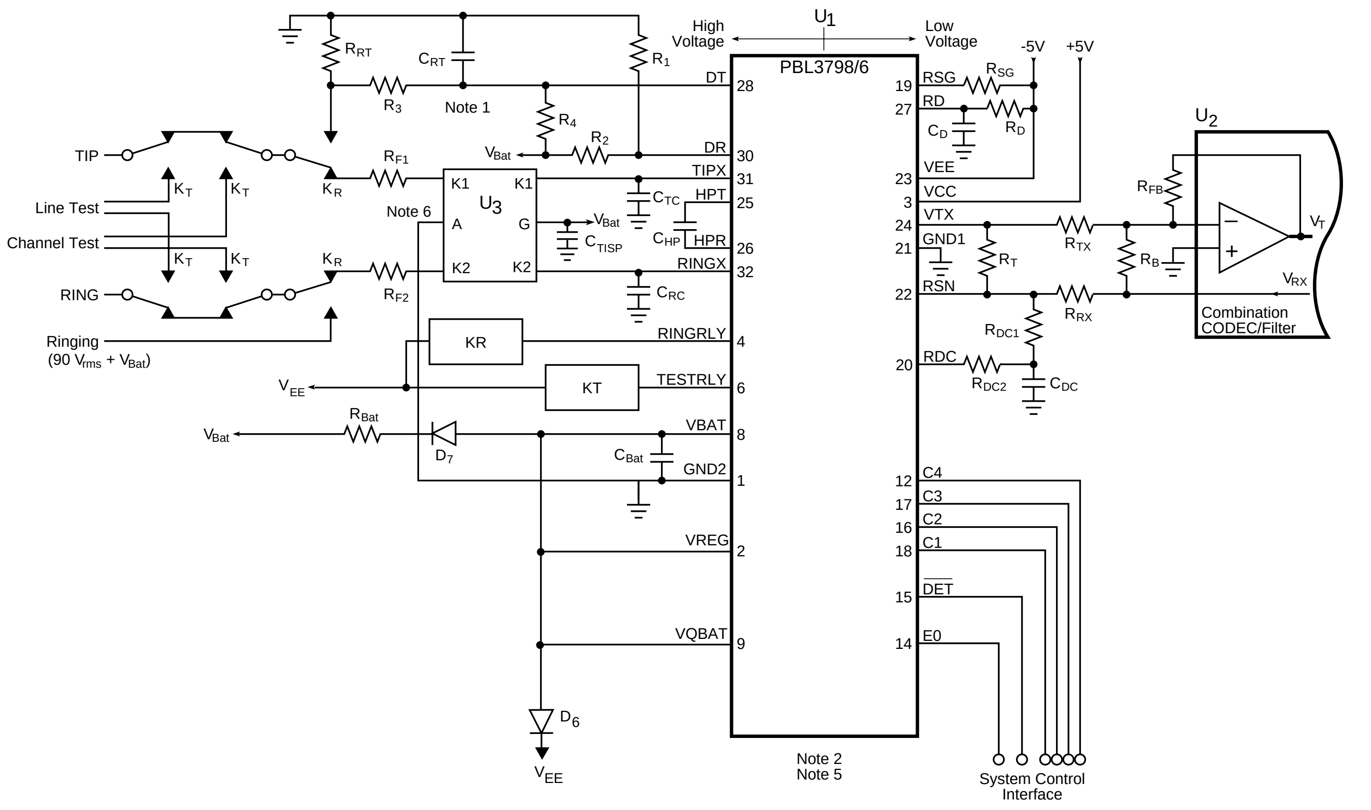
PLCC: 32-pin, j-leaded chip carrier. Refer to figure 8.

32PLCC	Symbol	Description
1	GND2	Ground. No internal connection to GND1. Note 1.
2	VREG	Negative voltage for power amplifiers.
3	VCC	+5 V power supply.
4	RINGRLY	Ring relay driver output. Sources up to 80 mA from VCC.
5	TP	TP is a thermal conduction pin tied to substrate (V_{QBat}). Note 2.
6	TESTRLY	Test relay driver output. Sources up to 80 mA from VCC.
7	NC	Must be left open
8	VBAT	Battery supply voltage. Negative with respect to GND2.
9	VQBAT	Quiet battery. An external filter capacitor connects between this pin and GND1 to provide filtered battery supply to signal processing circuits.
10	NC	Must be left open.
11	NC	Should be shorted to GND.
12	C4	C1 , C2 , C3 and C4 are TTL compatible decoder inputs controlling the SLIC operating states.
13	NC	Must be shorted to GND.
14	E0	Detector output enable. A logic high level enables the $\overline{\text{DET}}$ output. A logic low level disables the $\overline{\text{DET}}$ output. TTL compatible input.
15	$\overline{\text{DET}}$	Detector output. Inputs C1...C3 select the detector to be connected to this output. When $\overline{\text{DET}}$ is enabled via E0 a logic low level indicates that the selected detector is tripped. The $\overline{\text{DET}}$ output is open collector with internal pull-up resistor (15 kohms) to VCC. When disabled, $\overline{\text{DET}}$ thus appears to be a resistor connected to V_{CC}.
16	C2	Refer to pin C4 description.

32PLCC	Symbol	Description
17	C3	Refer to pin C4 description.
18	C1	Refer to pin C4 description.
19	RSG	Saturation guard programming input. A resistor, R_{SG}, between pins RSG and VEE adjusts the saturation guard for operation with V_{Bat} from -58 V to -46 V.
20	RDC	The constant dc loop current is programmed by two resistors connected in series from this pin to the receive summing node (RSN). The resistor junction point is decoupled to GND1 to filter noise and other disturbances before reaching the RSN input. V_{RDC} polarity is negative for normal tip-ring polarity and positive for reversed tip-ring polarity. $\|V_{RDC}\|$ = 2.5V in the constant current region.
21	GND1	Ground. No internal connection to GND2. Note 1.
22	RSN	Receive summing node. 100 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing between the TIPX and RINGX terminals. Programming networks for constant loop current, 2-wire impedance, and receive gain connect to the receive summing node.
23	VEE	-5 V power supply.
24	VTX	Transmit vf output. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced as an unbalanced GND1 referenced signal at VTX with a gain of one. The two-wire impedance programming network connects between VTX and RSN.
25	HPT	Tip side (HPT) of ac/dc separation capacitor.
26	HPR	Ring side (HPR) of ac/dc separation capacitor.
27	RD	Loop current detector programming resistor, R_D, connects from RD to VEE. A filter capacitor C_D may be connected from RD to GND1.
28	DT	Inverting ring trip comparator input.
29	TP	TP is a thermal conduction pin tied to substrate (V_{QBat}). Note 2.
30	DR	Non-inverting ring trip comparator input.
31	TIPX	The TIPX pin connects to the tip lead of the 2-wire line interface via overvoltage protection components, ring and test relays.
32	RINGX	The RINGX pin connects to the ring lead of the 2-wire line interface via overvoltage protection components, ring and test relays.

Notes

1. The GND1 and GND2 pins should be connected together via a direct printed circuit board trace.
2. For 32 pin PLCC, these pins (5 and 29) should be connected to V_{QBat}, serving as a heatsink.



U1	PBL 3798/6 Subcriber Line Interface Circuit (SLIC)			
U2	Combination CODEC/Filter, e.g. National Semiconductor TP3054			
U3	Secondary protection (e.g. Texas Instruments TISP PBL1)			
R_B	Resistor	33.2 kΩ	1%	1/4 W
R_{RX}	Resistor	26.1 kΩ	1%	1/4 W
R_T	Resistor	51.1 kΩ	1%	1/4 W
R_{TX}	Resistor	33.2 kΩ	1%	1/4 W
R_1, R_3	Resistor	200 kΩ	5%	1/4 W
R_2	Resistor	909 kΩ	5%	1/4 W
R_4	Resistor	1.21 MΩ	5%	1/4 W
R_D	Resistor	57.6 kΩ	5%	1/4 W
R_{DC1}, R_{DC2}	Resistor	4.99 kΩ	5%	1/4 W
R_{SG}	Resistor	Note 3	5%	1/4 W
R_{RT}	Resistor	150 Ω	5%	2 W
R_{Bat}	Resistor	Note 4		
R_{F1}, R_{F2}	Resistor	40 Ω 1% R_{F1}/R_{F2} ratio match (e.g. Ericsson Components PBR 51-series)		
C_{Bat}	Capacitor	0.47 µF	20%	100V

C_D	Capacitor	10 nF	20%	10V
C_{TISP}	Capacitor	220 nF	20%	100V
C_{DC}	Capacitor	330 nF	20%	10V
C_{HP}	Capacitor	220 nF	20%	100V
C_{RT}	Capacitor	0.39 µF	20%	100V
C_{TC}, C_{RC}	Capacitor	2200 pF	10%	100V
D_6	Diode	Note 7		
D_7	Diode	100 V	500 mA	
K_T	Relay, test		4C contacts	
K_R	Relay, ring		2C contacts	

Notes

1. The ringtrip network may alternatively be located on the RING lead side. The ringtrip network may also be configured for balanced ringing as shown in figure 16.
2. Pin 5 and 29 should be connected to VQBAT, serving as a heatsink.
3. RSG is open circuit for V_{Bat} = -48 V and shorted to V_{EE} for V_{Bat} = -63 V. For intermediate battery voltages, calculate as described in the section, "Battery feed, Case 2".
4. R_{Bat} for one line is recommended to be 5,6Ω 5% 1/4W. However the resistor can be shared between several lines, for instance 1 Ω 5% 1W for eight lines.
5. Pin 7 and 10 must be left open. Pin 11 should be shorted to ground. Pin 13 must be shorted to ground.
6. The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferrable a groundplane.
7. For diode type, refer to section "Power-Up Sequence".

Figure 9. PBL 3798/6 application example.

Functional Description and Applications Information Transmission

Overview

A simplified ac model of the transmission circuits is shown in figure 10. Neglecting the impact of the filters in figure 10 for frequencies from 300 Hz to 3.4 kHz (i.e. filter gain = 1), circuit analysis yields:

$$V_{TR} = V_{TX} + I_L \bullet 2R_F \quad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{100} \quad (2)$$

$$V_{TR} = E_L - I_L \bullet Z_L \quad (3)$$

where:

- V_{TX} is the ground referenced, unity gain version of the ac metallic (transversal) voltage between the TIPX and RINGX terminals, i.e. $V_{TX} = 1 \bullet V_{TRX}$.
- V_{TR} is the ac metallic voltage between tip and ring.
- E_L is the line open circuit ac metallic voltage.
- I_L is the ac metallic current.
- R_F is the overvoltage protection current limiting resistor.
- Z_L is the line impedance.
- Z_T is the programming network for the TIPX to RINGX impedance.
- Z_{RX} controls the four-wire to two-wire gain.
- V_{RX} is the analog ground referenced receive signal.

From equations (1), (2) and (3) expressions for two-wire impedance, two-wire to four-wire gain, four-wire to two-wire gain and four-wire to four wire gain may be derived.

Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the 2-wire line by the SLIC, including the resistors R_F, let $V_{RX} = 0$.

From (1) and (2):

$$Z_{TR} = \frac{Z_T}{100} + 2R_F$$

Since Z_{TR} and R_F are known Z_T may be calculated from

$$Z_T = 100 \bullet (Z_{TR} - 2R_F)$$

Example: calculate Z_T to make the terminating impedance Z_{TR} = 900 Ω in series with 2.16 µF. R_F = 40 Ω.

Using the expression above

$$Z_T = 100 \bullet \left(900 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 40\right)$$

$$= 82 \bullet 10^3 + \frac{1}{j\omega \bullet 21.6 \bullet 10^{-9}}$$

i.e. Z_T = 82 kΩ in series with 21.6 nF.

It is always necessary to have a high ohmic resistor in parallel with the capacitor. This gives a DC-feedback loop for low frequency which ensure stability and reduces noise.

Two-Wire to Four-Wire Gain

The two-wire to four-wire gain, G_{2-4}, can be obtained from (1) and (2) with $V_{RX} = 0$:

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/100}{Z_T/100+2R_F}$$

Four-Wire to Two-Wire Gain

The four-wire to two-wire gain, G_{4-2}, is derived from (1), (2) and (3) with $E_L = 0$:

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L}{Z_T/100 + 2R_F + Z_L}$$

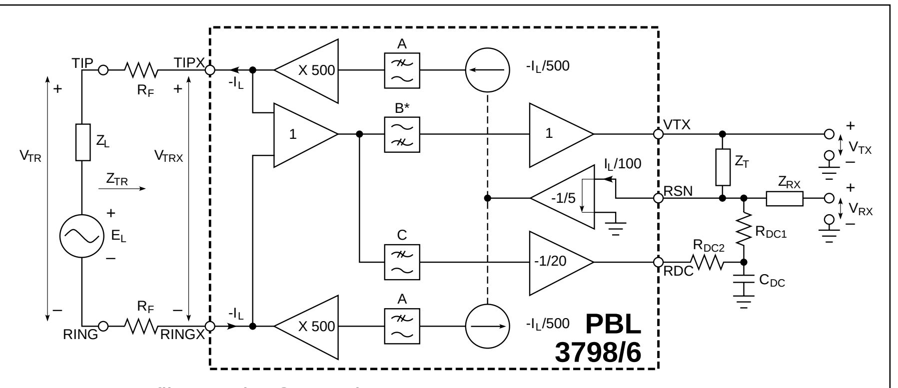
Four-Wire to Four-Wire Gain

The four-wire to four-wire gain, G_{4-4}, is derived from (1), (2) and (3) with $E_L = 0$:

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L + 2R_F}{Z_T/100 + 2R_F + Z_L}$$

Hybrid Function

The PBL 3798/6 SLIC forms a particularly flexible and compact line interface when used together with Siemens Codec Filter circuit (SiCoFi) or other similar programmable CODEC/filter. The SiCoFi allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. The SiCoFi also permits the system controller to adjust transmit and receive gains as well as terminating impedance. Refer to SiCoFi or similar programmable CODEC/filter data sheets for design information.



A: Lowpass filter, -3dB @ ≈ 34 kHz
B: Highpass filter, -3dB @ ≈ 1.8 Hz
C: Lowpass filter, -3dB @ ≈ 1.8 Hz
* ac-dc separation filter frequency is set by C_{HP}

Figure 10. Simplified ac transmission circuit.

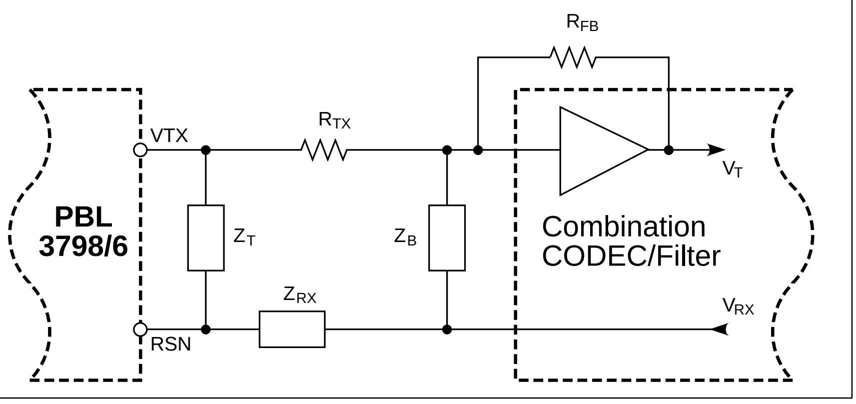


Figure 11. Hybrid function.

The hybrid function in an implementation utilizing the uncommitted amplifier in a conventional CODEC/filter combination is shown in figure 11. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned at VTX. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel each other by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \qquad (E_L = 0)$$

Substituting the four-wire to four-wire gain expression, G_{4-4}, for V_{RX}/V_{TX} yields the formula for the balance network:

$$Z_B = - R_{TX} \bullet \frac{V_{RX}}{V_{TX}} =$$

$$= R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{Z_T/100 + 2R_F + Z_L}{Z_L + 2R_F}$$

Example: $Z_{TR} = Z_L = 900\ \Omega$ (R_L) in series with 2.16 µF (C_L) $R_F = 40\ \Omega$, $R_{TX} = 27.4\ k\Omega$, $G_{4-2} = -1$. Calculate Z_B.

Using the Z_B formula above:

$$Z_B = \{Z_L = Z_{TR}\} = R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{2Z_L}{Z_L + 2R_F} =$$

$$= \{G_{4-2} = -1\} = R_{TX} \bullet \frac{Z_L}{Z_L + 2R_F} =$$

$$= R_{TX} \bullet \frac{1 + j\omega \bullet R_L \bullet C_L}{1 + j\omega \bullet (R_L + 2R_F) \bullet C_L}$$

A network consisting of R_{B1} in series with the parallel combination of R_B and C_B has the same form as the required balance network, Z_B. Basic algebra yields:

$$R_{B1} = R_{TX} \bullet \frac{R_L}{R_L + 2R_F} = 25.2\ k\Omega$$

$$R_B = R_{TX} \bullet \frac{2R_F}{R_L + 2R_F} = 2237\ \Omega$$

$$C_B = \frac{(R_L + 2R_F)^2 \bullet C_L}{R_{TX} \bullet 2R_F} = 0.95\ \mu F$$

Longitudinal Impedance

A feedback loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Therefore longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions well within the SLIC common mode range. This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal reference voltage, V_{LoRef}. As shown below, the SLIC appears as 20 Ω to ground per wire to longitudinal disturbances. It should be noted, that longitudinal currents may exceed the dc loop current without disturbing the vf transmission. From figure 12 the longitudinal impedance can be calculated:

$$\frac{V_{Lo}}{I_{Lo}} = \frac{R_{Lo}}{100} = 20\ \Omega$$

where:

V_{Lo} is the longitudinal voltage

I_{Lo} is the longitudinal current

$R_{Lo} = 2\ k\Omega$ sets the longitudinal impedance

Capacitors C_{TC} and C_{RC}

The capacitors designated C_{TC} and C_{RC} in figure 9, connected between TIPX and ground as well as between RINGX and ground, are recommended as an addition to the overvoltage protection network. Very fast transients, appearing on tip and ring, may pass by the diode and SCR clamps in the overvoltage protection network, before these devices have had time to activate and could damage the SLIC. C_{TC} and C_{RC} short such very fast transients to ground. The recommended value for C_{TC} and C_{RC} is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss. C_{TC} and C_{RC} contribute a metallic impedance of $1/(\pi \cdot f \cdot C_{TC}) \approx 1/(\pi \cdot f \cdot C_{RC})$, a TIPX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{RC})$.

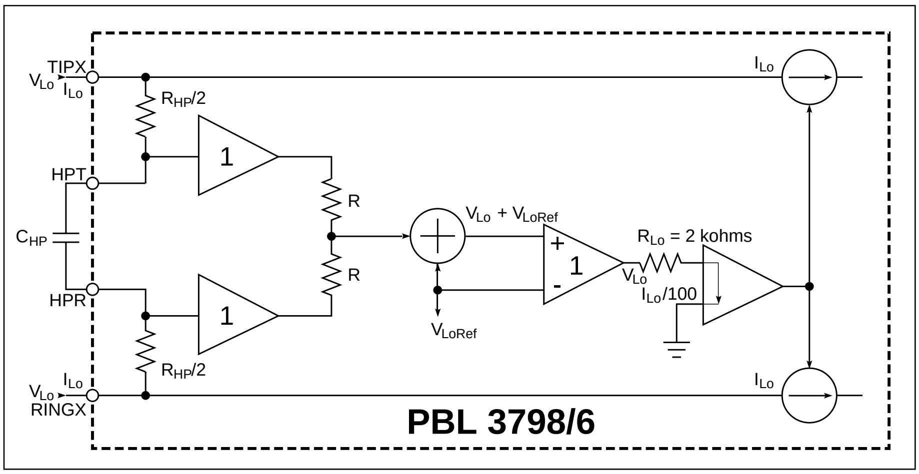


Figure 12. Longitudinal feedback loop. $V_{LoRef} = (V_{Tip} + V_{Ring})/2$ (without any longitudinal voltage component).

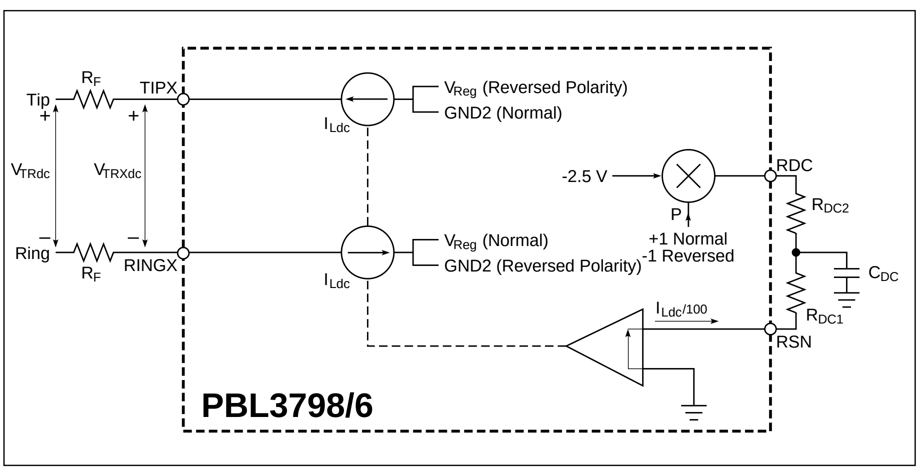


Figure 13. Battery feed.

Ac - dc Separation Capacitor

The high pass filter capacitor connected between terminals HPT and HPR provides separation between circuits sensing TIPX-RINGX dc conditions and circuits processing vf signals. The recommended C_{HP} capacitance value of 220 nF will position the 3 dB break point at 1.8 Hz.

Battery Feed

Overview

The PBL 3798/6 SLIC synthesizes a constant current feed system.

The magnitude of the constant loop current is set by two external resistors.

The battery feed polarity can be set to either normal or reversed polarity via the SLIC digital control inputs.

With the SLIC set to the stand-by state, power is further conserved by limiting the short circuit loop current to 50% of the active state short circuit current.

The following paragraphs describe the battery feed circuit in detail. At the end of this section a paragraph, Battery feed circuit programming procedure, summarizes the few simple calculations necessary to program the battery feed.

Case 1: SLIC in the Active or Active Polarity Reversal State; $|V_{TRdc}| < V_{SGRef}$

In the active state C3, C2, C1 = 0, 1, 0 and in the active polarity reversal state C3, C2, C1 = 1, 1, 0.

The battery feed control loop is shown in block diagram form in figure 13. For tip to ring dc voltages less than the saturation guard reference voltage, V_{SGRef} (refer to case 2) the following expression is obtained from the block diagram for R_F = 0.

$$I_{Ldc} = p \bullet \frac{250}{R_{DC1} + R_{DC2}}$$

where:

I_{Ldc} is the constant dc loop current

R_{DC1}, R_{DC2} are the external constant current programming resistors

p = 1 for normal polarity, -1 for reversed polarity

In figure 14, curve segment AB is described by case 1.

Case 2: SLIC in the Active or Active Polarity Reversal State; $|V_{TRdc}| > V_{SGRef}$

In the active state C3, C2, C1 = 0, 1, 0 and in the active polarity reversal state C3, C2, C1 = 1, 1, 0.

When the tip to ring dc voltage approaches the V_{Bat} supply voltage, a circuit named saturation guard limits the two-wire voltage to a small additional increase beyond the saturation guard threshold, V_{SGref}. This is to maintain distortion free vf transmission through the line drive amplifiers. The saturation guard feature makes on-hook transmission possible.

The tip to ring voltage at which the saturation guard becomes active, V_{SGRef}, can be calculated from

$$V_{SGRef} = \frac{30}{1 - \dfrac{0,95}{R_{SG} + 2,86}}$$

where

V_{SGRef} is in volts for R_{SG} in kohms

R_{SG} is a resistor connected between terminal RSG and -5 V.

R_{SG} = open circuit yields V_{SGRef} = 30 V

R_{SG} = 0 ohm yields V_{SGRef} = 44.9V

The loop current, I_{Ldc}, as a function of the loop voltage, V_{TRdc}, for $V_{TRdc} > V_{SGRef}$ is described by

$$I_{Ldc} = \frac{50 + 50 \bullet (V_{SGRef} - V_{TRdc})}{(R_{DC1} + R_{DC2}) / 5}$$

from which the open loop voltage (I_L = 0) is calculated to

$$V_{TRdc} = V_{SGRef} + 1.0$$

The open circuit voltage is then 31 V for R_{SG} = open circuit and 45.9 V for R_{SG} = 0.

In figure 14, PBL 3798/6 battery feed examples, curve segments CD and BJ are described by Case 2.

Case 3: SLIC in the stand-by or stand-by polarity reversal state; $|V_{TRdc}| < V_{SGRef}$

The stand-by operating states reduce power dissipation.

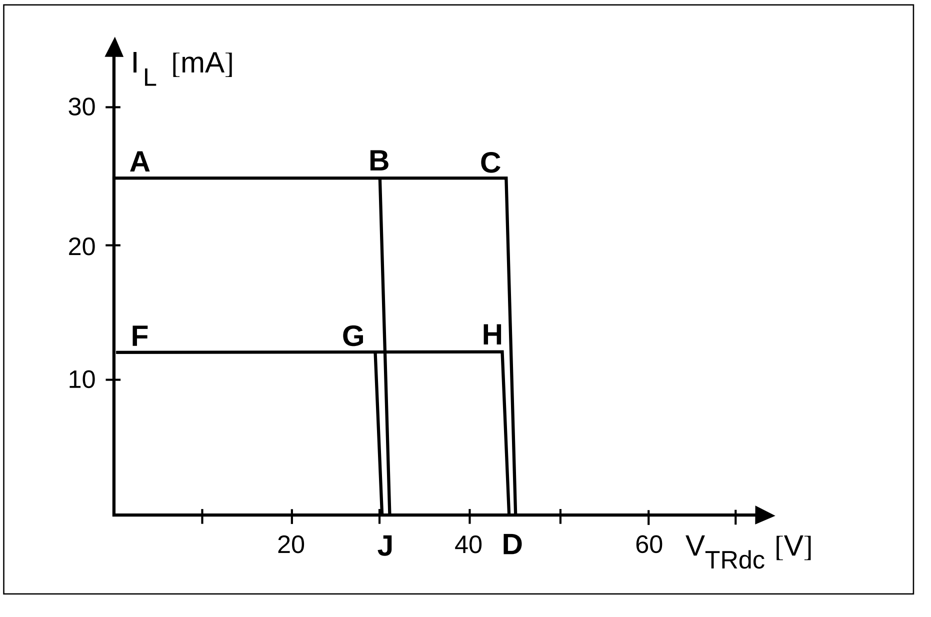
The loop feed in the stand-by state (C3, C2, C1 = 0, 1, 1) and in the stand-by polarity reversal state (C3, C2, C1 = 1, 1, 1) is constant current according to:

$$I_{Ldc} = p \bullet \frac{125}{R_{DC1} + R_{DC2}}$$

In figure 14, PBL 3798/6 battery feed examples, this corresponds to curve segments FG and FH.

Figure 14. PBL 3798/6 battery feed examples.

$R_{DC1} = R_{DC2}$ = 5.0 kΩ, I_{Ldc} = 25 mA.
Curve ABJ: active state. PBL 3798/6 with $R_{SG} = \infty$ Ω and V_{Bat} = -48 V.
Curve ACD: active state. PBL 3798/6 with R_{SG} = 0 Ω and V_{Bat} = -58 V.
Curve FGJ: stand-by state. PBL 3798/6 with $R_{SG} = \infty$ Ω and V_{Bat} = -48 V.
Curve FHD: stand-by state. PBL 3798/6 with R_{SG} = 0 Ω and V_{Bat} = -58 V.



Case 4: SLIC in the Stand-by or Stand-by Polarity Reversal State; $|V_{TRdc}| > V_{SGRef}$

In the stand-by state C3, C2, C1 = 0, 1, 1 and in the stand-by polarity reversal state C3, C2, C1 = 1, 1, 1.

When the tip-to-ring dc voltage exceeds the saturation guard reference voltage, V_{SGRef}, the loop feed is described by:

$$I_{Ldc} = \frac{50 + 50 \cdot (V_{SGRef} - V_{TRdc})}{(R_{DC1} + R_{DC2}) / 2.5}$$

In figure 14, this corresponds to curve segments HD and GJ.

C_{DC} Capacitor

Refer to the battery feed block diagram, figure 13. The battery feed programming resistors R_{DC1} and R_{DC2} together with capacitor C_{DC} form a low pass filter, which removes noise and vf signals from the battery feed control loop. The recommended 3 db break point frequency is 160 Hz < f_{3dB} < 240 Hz. The C_{DC} capacitance value is then calculated from:

$$C_{DC} = \frac{1}{2\pi \cdot f_{3dB}} \cdot \left[\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}} \right]$$

Note that $R_{DC1} = R_{DC2}$ yields minimum C_{DC} capacitance value.

Battery Feed Circuit Programming Procedure

Extracting the key elements from the preceeding description results in the following step-by-step procedure.

1. Establish the battery feed requirements.

   Constant loop current, I_{Ldc} = ?

   Maximum loop resistance, including fuse resistors R_{F1} and R_{F2}, R_{LMax} = ?

   Loop resistance, above which it is permissible for the loop feed to change from constant current feed to resistive feed, R_{LSGRef} = ?

   Loop current at the maximum loop resistance (applies if $I_{Ldc} \cdot R_{LMax} > V_{SGRef}$) I_{LMin} = ?

   SLIC supply voltage, VBAT = ?

2. Calculate the constant current programming components R_{DC1} and R_{DC2} from

$$R_{DC1} = R_{DC2} = \frac{250}{I_{Ldc}} \cdot \frac{1}{2}$$

3. Calculate C_{DC} from

$$C_{DC} = \frac{1}{2\pi \cdot f_{3dB}} \cdot \left[\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}} \right]$$

   where $f_{3dB} \approx 200$ Hz

4. Calculate the saturation guard programming resistor, R_{SG}.

   RSG terminal open circuit: V_{SGRef} = 30 V.

   RSG terminal shorted to V_{EE}: V_{SGRef} = 44.9 V.

   For intermediate V_{SGRef} values calculate R_{SG} according to

$$R_{SG} = \frac{1{,}9}{\frac{14{,}9}{44{,}9 - V_{SGRef}} - 1}$$

   where R_{SG} is in kohms for V_{SGRef} in volts.

   The minimum required battery voltage to maintain distortion free vf transmission is $|V_{Batmin}| = V_{SGRef} + 12$ V. For loop voltages greater than V_{SGRef}, $|V_{Batmin}| = V_{TRdc} + 12$ V.

5. Calculate the loop resistance at which the saturation guard becomes active, R_{LSGRef}:

$$R_{LSGRef} = \frac{V_{SGRef}}{I_{Ldc}}$$

   Confirm compatibility with requirements.

6. If $I_{Ldc} \cdot R_{LMax} > V_{SGRef}$, calculate loop current at maximum loop resistance:

$$I_{Ldcmin} = \frac{50 + 50 \cdot V_{SGRef}}{(R_{DC1} + R_{DC2})/5 + 50 \cdot R_{LMax}}$$

   Confirm compatibility with requirements.

Loop Monitoring Functions

Overview

The PBL 3798/6 SLIC contains two detectors: the loop current and the ring trip detector. These two detectors report their status via the shared $\overline{DET}$ output. The detector to be connected to the $\overline{DET}$ output is selected according to the logic states at the control inputs C1, C2, C3 and enable input E0. Enable input E0 sets the $\overline{DET}$ output to either active or high impedance state.

Loop Current Detector - Active State and Standby State

Active state (C3, C2, C1 = 0, 1, 0) and active polarity reversal state (C3, C2, C1 = 1, 1, 0) as well as standby state (C3,C2, C1 = 0, 1,1) and standby polarity reversal state (C3, C2, C1 = 1, 1, 1)

The loop current value at which the loop current detector changes state is programmable by calculating a value for resistor R_D. R_D connects between terminals RD and VEE.

Figure 15 shows a block diagram for the loop current detector. The two-wire interface produces a current, I_{RD}, flowing out of pin RD:

$$I_{RD} = 0.5 \cdot \frac{|I_{LT} - I_{LR}|}{300} = \frac{|I_L|}{300}$$

where I_{LT} and I_{LR} are currents flowing into the TIPX and RINGX terminals and I_L is the loop current. The voltage generated across the programming resistor R_D by I_{RD} is applied to an internal comparator with hysteresis. The comparator reference voltage for transition on-hook to off-hook is 1.55 V. The reference voltage for a transition off-hook to on-hook is 1.37 V. A logic low level results at the $\overline{DET}$ output, when the comparator reference voltage is exceeded.

For a specified on-hook to off-hook loop current threshold, I_{LThOff}, R_D is calculated from

$$R_D = \frac{1.55 \cdot 300}{|I_{LThOff}|}$$

The calculated R_D value corresponds to an off-hook to on-hook loop current threshold, I_{LThOn}, of

$$|I_{LThOn}| = \frac{1.37 \cdot 300}{R_D}$$

Loop Current Detector - Filter Capacitor

It is recommended to filter the signal at the RD pin with a capacitor C_D connected between terminal RD and ground.

A suggested value for C_D is:

$$C_D = \frac{1}{2\pi \cdot R_D \cdot f_{3dB}}, \text{ where } f_{3dB} = 500 \text{ Hz}$$

Note that C_D may not be required if $\overline{DET}$ is software filtred.

Ring Trip Detector

Ring trip detection is accomplished by monitoring the two-wire line for presence of dc current while ringing is applied. When the subscriber goes off-hook with ringing applied, dc loop current starts to flow. The comparator in the SLIC with inputs DT and DR detects this current flow via an interface network. The result of the comparison is presented at the $\overline{DET}$ output. The ring trip comparator is automatically connected to the $\overline{DET}$ output, when the SLIC control inputs are set to the ringing state (C3, C2, C1 = 0, 0, 1). When off-hook during ringing is detected, the line card or system controller will proceed to disconnect the ringing source (software ringtrip) by re-setting the control input logic states. Alternatively, the $\overline{DET}$ output may be monitored by circuits on the line card, which perform the ringtrip function (hardware ringtrip).

The ringing source may be balanced or unbalanced, superimposed on the V_{Bat} supply voltage. The unbalanced ringing source may be applied to either the tip lead or the ring lead with return on the other wire. A ring relay, energized by the SLIC ring relay driver, connects the ringing source to tip and ring. For unbalanced ringing systems the loop current sensing resistor may be placed either in series with the ringing generator or in series with the return lead to ground.

Figures 16 and 17 show examples of balanced and unbalanced ringing systems. For either ringing system the ringtrip detection function is based on a polarity change at the inputs DT and DR of the ringtrip comparator.

In the unbalanced case the dc voltage drop across resistor R_{RT} is zero as long as the telephone remains on-hook. With the telephone off-hook during ringing, dc loop current will flow, causing a voltage drop across R_{RT}. The R_{RT} voltage is applied to the comparator input DT via resistor R_3. R_4 shifts the voltage level to be within the comparator common mode range. C_{RT} removes the ac component of the ringing signal. R_1 and R_2 establish a bias voltage at comparator input DR, which is more negative than DT when the telephone is on-hook and is more positive than DT when the telephone goes off-hook during ringing.

Complete removal of the ringing signal ac component at the DT input may not be necessary. Some residual ac component at the DT input may under certain operating conditions cause the $\overline{DET}$ output to toggle between the on-hook and off-hook states at the ringing frequency. However, with the telephone off-hook the $\overline{DET}$ output will be at logic low level for more than half the time. Therefore, by sampling the $\overline{DET}$ output, a software routine can discriminate between on-hook and off-hook through examination of the duty cycle. Full removal of the ringing frequency from the DT input while maintaining ringtrip within required time limits (approximately < 100 ms) usually mandates a second order filter rather than the first order shown in figure 17. The software approach minimizes the number of line card components.

In the balanced ringing system shown in figure 16, R_1 and R_2 are the loop current sensing resistors. With the telephone on-hook, no dc loop current flows to cause a dc voltage drop across resistors R_1 and R_2. Voltage dividers R_{B2}, R_4 and R_{B1}, R_3 bias the ringtrip comparator input DT to be more positive than DR. With the telephone off-hook during ringing dc loop current will flow, causing a voltage drop across resistors R_1 and R_2, which in turn will make comparator input DT more negative than DR, setting the $\overline{DET}$ output to logic low level, indicating ringtrip condition. Capacitors C_{RT1} and C_{RT2} filter the ring voltage at the comparator inputs. For 20 Hz ringing it is suitable to calculate these capacitors for a time constant of T = 50 ms, i. e.

$$C_{RT1} = T \cdot \left(\frac{1}{R_{B2}} + \frac{1}{R_4}\right)$$

Detector Output, $\overline{DET}$

The loop current detector and ringtrip comparator share a common output, $\overline{DET}$. The $\overline{DET}$ output is open collector with internal pull-up resistor to V_{CC}. Via control inputs C1 through C3 one of the two detectors is selected to be connected to the $\overline{DET}$ output. With enable input E0 set to logic high level the $\overline{DET}$ output is activated. In the $\overline{DET}$ active state a logic low level indicates a triggered detector condition and a logic high level reports a non-triggered detector. With E0 set to logic low level, the $\overline{DET}$ output is set to its high impedance state, i.e. connected to V_{CC} via the internal pull-up resistor.

Relay Drivers

The PBL 3798/6 SLIC contains two identical drivers for test and ring relays. The drivers are pnp transistors in open collector configuration, sourcing up to 80 mA from the V_{CC} supply. Each driver has an internal inductive kick-back clamp diode. The relay coil may be connected to negative supply voltages ranging from ground to V_{Bat}. Control input C4 activates the test relay driver. Control inputs C1, C2 and C3 are used to operate the ring relay.

Control Inputs

Overview

The PBL 3798/6 SLIC has four TTL compatible control inputs, C1 through C4. A decoder in the SLIC interprets the control input logic conditions and sets up the commanded operating state. C1 through C3 allow for eight operating states. The C4 control input acts directly on the test relay driver.

The control inputs interface with programmable CODEC/filters, e.g. SLAC, SiCoFi, Combo II without any interface components. Via serial I/O ports on the programmable CODEC/filter devices a microprocessor can communicate with the SLIC. In designs utilizing conventional CODEC/filters without control latches, the line card logic must contain the neccessary latches for inputs C1 through C4.

Table 1 contains a summary description of the Control Inputs.

Test Relay Control (C4)

With C4 set to logic low level the test relay driver (TESTRLY) is activated. The active driver can source up to 80 mA from the V_{CC} supply. C4 set to logic high level causes the relay driver to be de-energized. The test relay driver is controlled exclusively by C4 and is independent of the C1, C2 and C3 logic levels.

Open Circuit State (C3, C2, C1 = 0, 0, 0)

In the Open Circuit State both the TIPX and RINGX power amplifiers present a high impedance to the line. The loop current detector is not active in this state.

Ringing State (C3, C2, C1 = 0, 0, 1)

The ring relay driver (RINGRLY) is activated and the ring trip comparator is connected to the detector output ($\overline{DET}$). The TIPX and RINGX terminals are in the high impedance state and signal transmission is inhibited.

Active State (C3, C2, C1 = 0, 1, 0)

TIPX is the terminal closest to ground potential and sources loop current, while RINGX is the more negative terminal and sinks loop current. Signal transmission is normal and the loop current is gated to the $\overline{DET}$ output.

Stand-by State (C3, C2, C1 = 0, 1, 1)

In the stand-by state the short circuit loop current is reduced to:

$I_{Ldc} = 125 / (R_{DC1} + R_{DC2})$.

The loop current is connected to the $\overline{DET}$ output.

Reserved State (C3, C2, C1 = 1, 0, 1) and (C3, C2, C1 = 1, 0, 0)

These states has no assigned function.

Active Polarity Reversal State (C3, C2, C1 = 1, 1, 0)

TIPX and RINGX polarity is reversed from the Active State: RINGX is the terminal closest to ground and sources loop current while TIPX is the more negative terminal and sinks current. Polarity reversal transition time is 4 msec. The loop current is connected to the $\overline{DET}$ output. Signal transmission is normal.

Stand-by Polarity Reversal State (C3, C2, C1 = 1, 1, 1)

Polarity Reversal as described under state C3, C2, C1 = 1, 1, 0 and Stand-by as described under state C3, C2, C1 = 0, 1, 1.

Enable Inputs

The PBL 3798/6 SLIC has a TTL compatible enable inputs, E0.

E0 sets the $\overline{DET}$ output to active state, when at logic high level and to high impedance state when at logic low level.

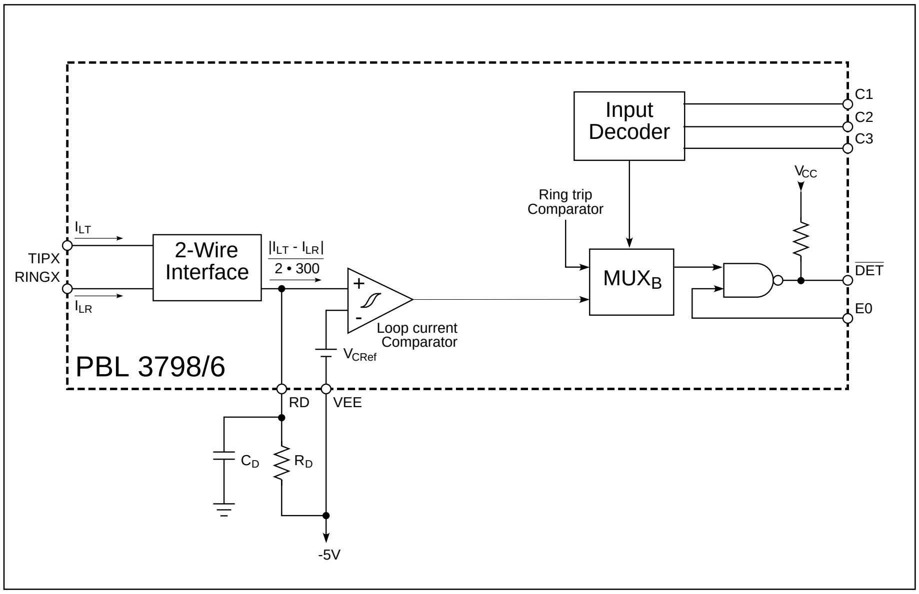


Figure 15. Loop current detector.

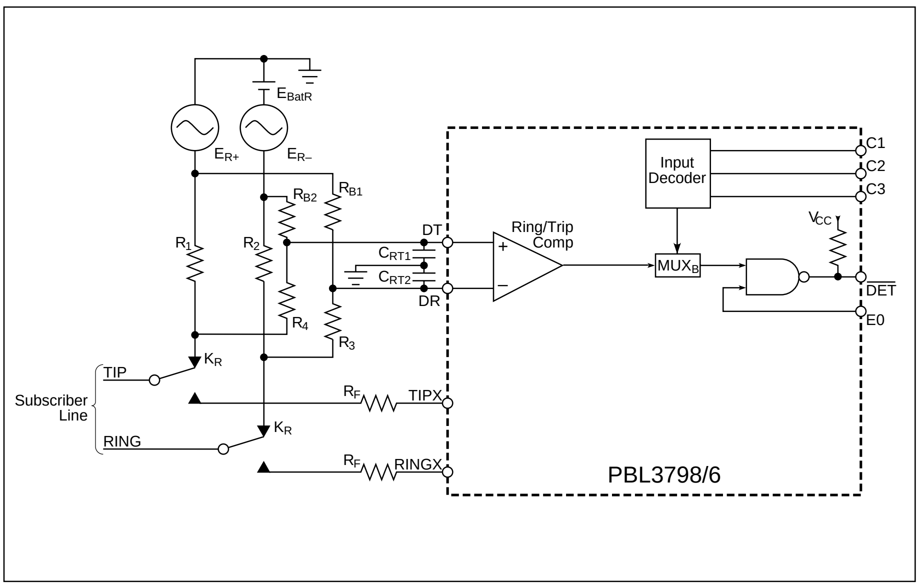


Figure 16. Ring trip network, balanced ringing.

Overvoltage Protection

The PBL 3798/6 SLIC must be protected against overvoltages on the telephone line caused by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum allowable continuous and transient voltages that may be applied to the SLIC.

The circuit shown in figure 9 utilizes series resistors together with a programmable overvoltage protector (e g Texas Instrument TISP PBL1), serving as a secondary protection.

The protection network in figure 9 is designed to meet requirements in ITU-T K20, table 1.

The TISP PBL1 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i e the battery voltage,V_{Bat}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by an internal diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage on-state condition, clamping the overvoltage close to ground.

A gate decoupling capacitor, C_{TISP} is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. Without the capacitor even the low inductance in the track to the V_{Bat} supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F serve the dual purposes of being non- destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross. Ericsson Components AB offers a series of thick film resistors networks (e g PBR 51-series and PBR 53-series) designed for this application.

Also devices with a built in resetable fuse function is offered (e g PBR 52-series) including positive temperature coefficient (PTC) resistors, working as resetable fuses, in series with thick film resistors. Note that it is important to always use PTC´s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore the ability to protect the SLIC will be reduced.

If there is a risk overvoltages on the V_{Bat} terminal on the SLIC, then this terminal should also be protected.

Over-Temperature Protection

A ring lead to ground short circuit fault condition, as well as other improper operating modes, may cause excessive SLIC power dissipation. If junction temperature increases beyond 140°C, the temperature guard will trigger, causing the SLIC to be set to a high impedance state. In this high impedance state power dissipation is reduced and the junction temperature will return to a safe value. Once below 130 °C junction temperature the SLIC is returned back to its normal operating mode and will remain in that state assuming the fault condition has been removed.

Power-Up Sequence

The voltage at pin VBAT sets the sub-strate voltageVQBAT (supplied internally from V_{Bat} through a resistor), which must at all times be kept more negative than the voltage at any other terminal. This is to maintain correct junction isolation between devices on the chip. To prevent possible latch-up, the optimal power-up sequence is to connect ground and V_{Bat}, then other supply voltages and signal leads. Should the V_{Bat} supply voltage be absent or if VEE or VCC must for other reasons be connected before V_{Bat}, a diode with low forward voltage drop (Schottky diode or a diode with a 1 A current rating), connected with its cathode to V_{EE} and anode to VQBAT, ensures the presence of the most negative supply voltage at the VQBAT pin.

The V_{Bat} voltage should not be applied at a faster rate than $dV_{Bat}/dt = 4$ V/µsec, e.g. a time constant formed by a 5.1 ohm resistor in series with the VBAT pin and a 0.47 microfarad capacitor from the VBAT pin to ground. One resistor may be shared by several SLICs.

Printed Circuit Board Layout

Care in PCB layout is essential for proper function. The components connecting to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the RSN terminal. A ground plane surrounding the RSN pin is advisable. The C_{HP} capacitor should be placed close to terminals HPT and HPR to avoid unwanted disturbances.

Ground terminals GND1 and GND2 should be connected via a direct PCB trace at the device location.

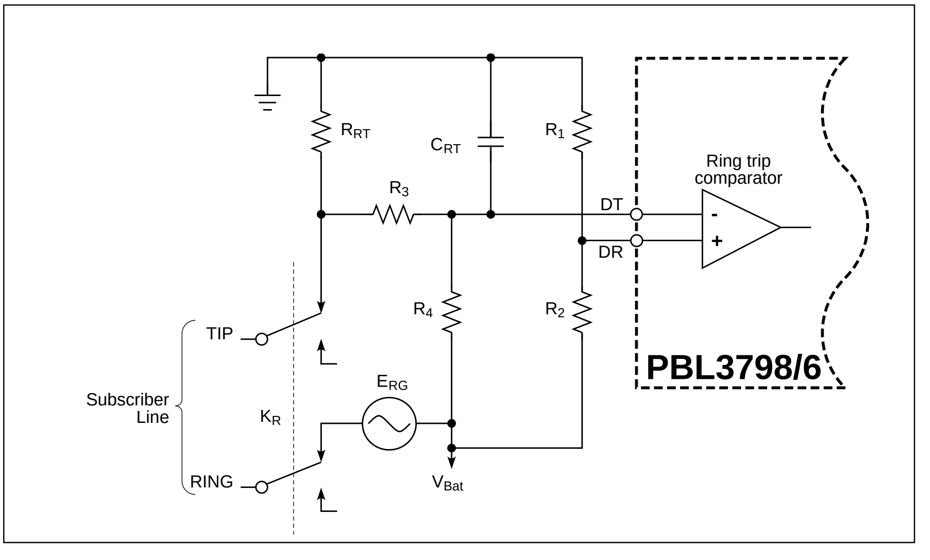


Figure 17. Ring trip network, unbalanced ringing.

State #	C4 Note 1	C3	C2	C1	Operating State	Active detector
1	X	0	0	0	Open circuit	Ring trip
2	X	0	0	1	Ringing	Ring trip
3	X	0	1	0	Active	Loop current
4	X	0	1	1	Stand-by	Loop current
5	X	1	0	0	Reserved	None
6	X	1	0	1	Reserved	None
7	X	1	1	0	Active polarity reversal	Loop current
8	X	1	1	1	Stand-by polarity reversal	Loop current

Notes

1. Control input C4 logic state (X) affects only the test relay driver and does not change the SLIC operating state. C4 at logic low level activates the test relay driver. C4 at logic high level turns the test relay driver off.

Table 1. PBL 3798/6 operating states.

Enable state #	E0	$\overline{DET}$ output state	Active detector
1	0	High impedance	None
2	1	Active	Loop current or ringtrip. Note 1

Notes

1. The loop current detector or the ring trip comparator is selected via C3, C2, C1 (state# 2 selects the ringtrip comparator.)

Table 2. Enable inputs E0.

Ordering Information

Package	Temp. Range	Part No.
PLCC 32 pin	0 to 70°C	PBL 3798/6RN

1522-PBL 3798/6 Uen Rev. A

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