PBL 386 21/1 Subscriber Line Interface Circuit

Description

The PBL 386 21/1 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in DAML, FITL and other telecommunications equipment. The PBL 386 21/1 has been optimized for low total line interface cost and a high degree of flexibility in different applications.

The PBL 386 21/1 emulates resistive loop feed, programmable between 2x25 Ω and 2x900 Ω, with short loop current limiting adjustable to max 30 mA.

A second lower battery voltage may be connected to the device to reduce short loop power dissipation. The SLIC automatically switches between the two battery supply voltages without need for external components or external control.

The SLIC incorporates loop current, ground key and ring trip detection functions. The PBL 386 21/1 is compatible with loop start signaling.

Two- to four-wire and four- to two-wire voice frequency (VF) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter, e.g. SLAC, SiCoFi, Combo II. The programmable the two-wire impedance, complex or real, is set by a simple external network.

Longitudinal voltages are suppressed by a feedback loop in the SLIC and the longitudinal balance specifications meet Bellcore TR909 requirements.

The PBL 386 21/1 package options are 24-pin SOIC or 28-pin PLCC.

Key Features

- High and low battery with automatic switching
- 60 mW on-hook power dissipation in active state
- On-hook transmission
- Long loop battery feed tracks Vbat for maximum line voltage
- Only +5 V feed in addition to battery
- Selectable transmit gain (1x or 0.5x)
- No power-up sequence
- 44V open loop voltage @ -48V battery feed
- Tertiary protection
- Full longitudinal current capability during on-hook state
- Analog over temperature protection permits transmission while the protection circuit is active
- Polarity reversal
- Integrated Ring Relay driver
- Ground key detector
- Programmable signal headroom
- -40 °C to +85 °C ambient temperature range

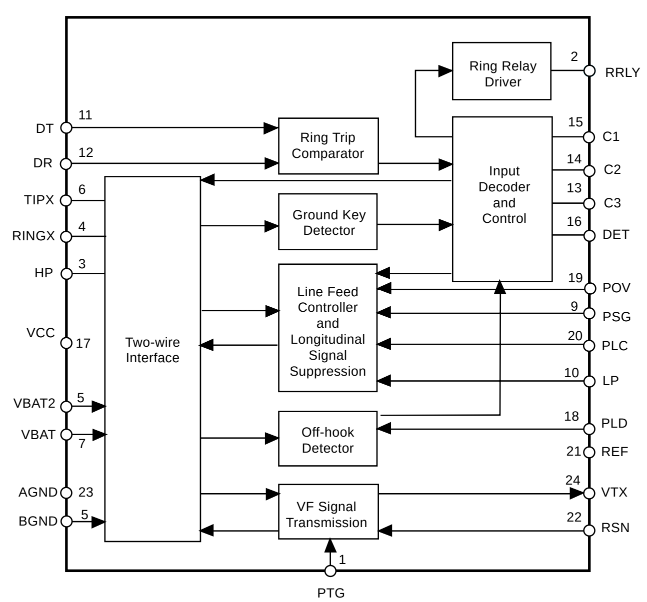
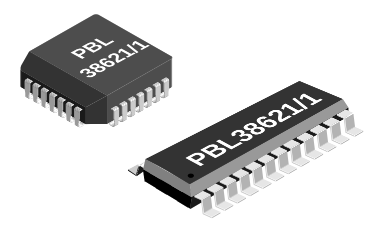


Figure 1. Block diagram 24 SOIC.



24-pin SOIC, 28-pin PLCC

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-55	+150	°C
Operating temperature range	T_{Amb}	-40	+110	°C
Operating junction temperature range, Note 1	T_J	-40	+140	°C
Power supply, -40 °C ≤ T_{Amb} ≤ +85 °C				
V_{CC} with respect to A/BGND	V_{CC}	-0.4	6.5	V
V_{BAT2} with respect to A/BGND	V_{Bat2}	V_{Bat}	0.4	V
V_{Bat} with respect to A/BGND, continuous	V_{Bat}	-75	0.4	V
V_{Bat} with respect to A/BGND, 10 ms	V_{Bat}	-80	0.4	V
Power dissipation				
Continuous power dissipation at T_{Amb} ≤ +85 °C	P_D		1.5	W
Ground				
Voltage between AGND and BGND	V_G	-3	3	V
Relay Driver				
Ring relay supply voltage			BGND+14	V
Ring trip comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	AGND	V
Input current	I_{DT}, I_{DR}	-5	5	mA
Digital inputs, outputs (C1, C2, C3, DET)				
Input voltage	V_{ID}	-0.4	V_{CC}	V
Output voltage	V_{OD}	-0.4	V_{CC}	V
TIPX and RINGX terminals, -40 °C < T_{Amb} < +85 °C				
TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-100	+100	mA
TIPX or RINGX current, pulse < 10 ms, t_{Rep} > 10 s	I_{TIPX}, I_{RINGX}	-2	2	A
TIPX or RINGX current, pulse < 1 ms, t_{Rep} > 10 s	I_{TIPX}, I_{RINGX}	-5	5	A
TIPX or RINGX current, pulse < 10 µs, t_{Rep} > 10 s	I_{TIPX}, I_{RINGX}	-15	15	A
TIPX or RINGX current, pulse < 1 µs, t_{Rep} > 10 s,	I_{TIPX}, I_{RINGX}	-20	20	A
TIP or RING current, pulse < 250 ns, t_{Rep} > 10 s	I_{TIPX}, I_{RINGX}	-20	20	A

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	-40	+85	°C
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{Bat} with respect to AGND	V_{Bat}	-58	-8	V
AGND with respect to BGND	V_G	-100	100	mV

Notes

1. The circuit includes thermal protection. Operation at or above 140°C junction temperature may degrade device reliability.

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ +85 °C, PTG = open (see pin description), V_{CC} = +5V ±5 %, V_{Bat} = -58V to -40V, V_{Bat2} = -17V, R_{LC}=38.3 kΩ, I_L = 22 mA. R_L = 600 Ω, R_{F1}= R_{F2}= R_{P1}= R_{P2}=0, R_{Ref} = 49.9 kΩ, C_{HP} = 47 nF, C_{LP}=0.15 µF, R_T = 120 kΩ, R_{SG} = 0 kΩ, R_{RX} = 60 kΩ, R_R = 52.3 kΩ R_{OV} = ∞ unless otherwise specified. All pin number references in the text and figures refer to the 24-pin SOIC unless otherwise specified. Current definition: current is positive if flowing into a pin.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	2	Active state				
		1% THD	1.1			V_{Peak}
On-Hook, $I_{Ldc} \leq$ 5mA		Note 1, R_{OV} = ∞	1.1			V_{Peak}
Input impedance, Z_{TR}		Note 2		Z_T/200		
Longitudinal impedance, Z_{LoT}, Z_{LoR}		0 < f < 100 Hz		20	35	Ω/wire
Longitudinal current limit, I_{LoT}, I_{LoR}		active state	10			mA_{rms}/wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985, Z_{TRX}=736Ω				
		0.2 kHz < f < 1.0 kHz	53			dB
		1.0 kHz < f < 3.4 kHz	53			dB
		Reverse polarity 0.2 kHz < f < 3.4 kHz	50			dB
Longitudinal to metallic balance, B_{LME}	3					
		0.2 kHz < f < 1.0 kHz	53			dB
$B_{LME}=20 \bullet \text{Log}\left\|\frac{E_{LO}}{V_{TR}}\right\|$		1.0 kHz < f < 3.4 kHz	53			dB
		Reverse polarity 0.2 kHz < f < 3.4 kHz	50			dB
Longitudinal to four-wire balance, B_{LFE}	3					
		0.2 kHz < f < 1.0 kHz	53			dB
$B_{LFE} = 20 \bullet \text{Log}\left\|\frac{E_{Lo}}{V_{TX}}\right\|$		1.0 kHz < f < 3.4 kHz	53			dB
Metallic to longitudinal balance, B_{MLE}	4	0.2 kHz < f < 3.4 kHz	40	50		dB
$B_{MLE} = 20 \bullet \text{Log}\left\|\frac{E_{TR}}{V_{Lo}}\right\|$; $E_{RX} = 0$						

Figure 2. Overload level, V_{TRO}, two-wire port

$\frac{1}{\omega C} << R_L$, R_L= 600 Ω

R_T = 120 kΩ, R_{RX} = 60 kΩ

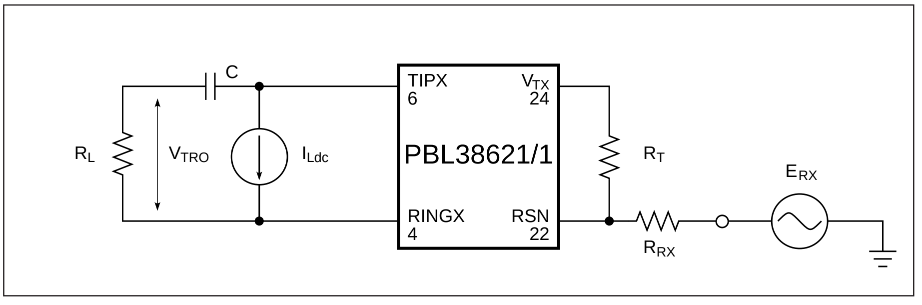
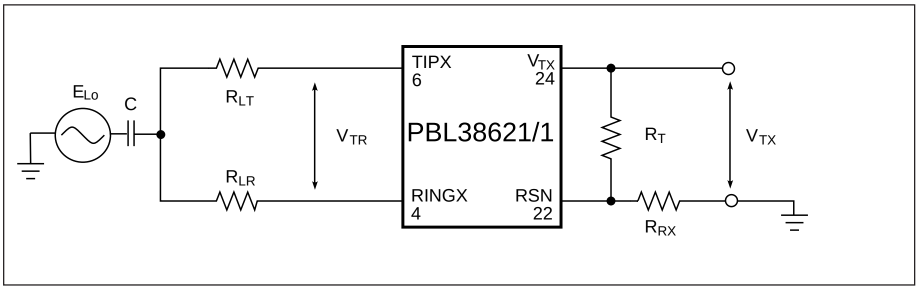


Figure 3. Longitudinal to metallic (B_{LME}) and Longitudinal to four-wire (B_{LFE}) balance

$\frac{1}{\omega C}$ << 150 Ω, R_{LR} =R_{LT} =R_L /2=300Ω

R_T = 120 kΩ, R_{RX} = 60 kΩ



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to longitudinal balance, B_{FLE}	4	0.2 kHz < f < 4.0 kHz	40			dB
		$B_{FLE} = 20 \bullet \text{Log} \left\| \frac{E_{RX}}{V_{Lo}} \right\|$				
		E_{TR} source removed				
Two-wire return loss, r		$r = 20 \bullet \text{Log} \frac{\|Z_{TR} + Z_L\|}{\|Z_{TR} - Z_L\|}$				
		0.2 kHz < f < 1.0 kHz	27	35		dB
		1.0 kHz < f < 3.4 kHz, Note 3	20	22		dB
TIPX idle voltage, V_{Ti}		active, I_L = 0 mA		- 1.1		V
RINGX idle voltage, V_{Ri}		active, I_L = 0 mA		V_{Bat}+2.5		V
V_{TR}		active, I_L = 0 mA		V_{Bat}-3.6		V
Four-wire transmit port (V_{TX})						
Overload level, V_{TXO}	5	Load impedance > 20 kΩ, 1% THD, Note 4	1.1			V_{Peak}
On-hook, $I_L \leq$ 5mA			1.1			V_{Peak}
Four-wire transmit port (VTX) DC voltage			-100	0	100	mV
Output impedance, z_{TX}		0.2 kHz < f < 3.4 kHz		15	50	Ω
Four-wire receive port (RSN)						
Receive summing node (RSN) DC voltage		I_{RSN} = -55 µA	1.15	1.25	1.35	V
Receive summing node (RSN) impedance		0.2 kHz < f < 3.4 kHz		5	20	Ω
Receive summing node (RSN) current (I_{RSN}) to metallic loop current (I_L) gain, α_{RSN}		0.3 kHz < f < 3.4 kHz		200		ratio
Frequency response						
Two-wire to four-wire, g_{2-4}	6	relative to 0 dBm, 1.0 kHz. E_{RX} = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.20		0.10	dB
		f = 8.0 kHz, 12 kHz, 16 kHz	-1.0		0.1	dB

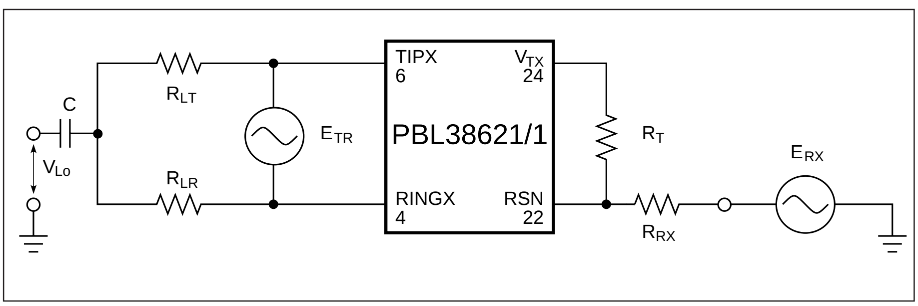


Figure 4. Metallic to longitudinal and four-wire to longitudinal balance

$\frac{1}{\omega C}$ << 150 Ω, $R_{LT} = R_{LR} = R_L/2 = 300Ω$

R_T = 120 kΩ, R_{RX} = 60 kΩ

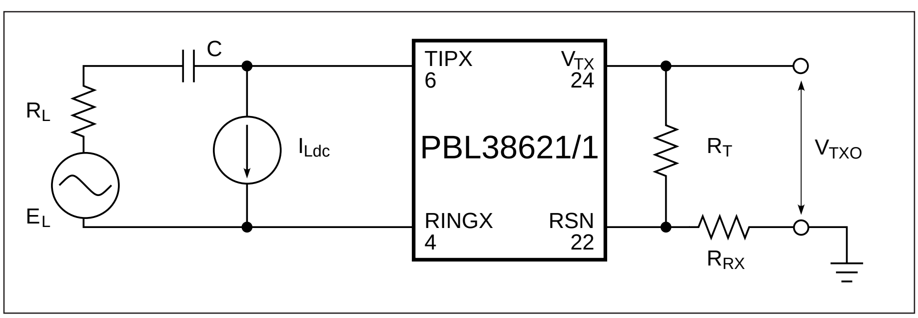


Figure 5. Overload level, V_{TXO}, four-wire transmit port

$\frac{1}{\omega C}$ << R_L, R_L = 600 Ω

R_T = 120 kΩ, R_{RX} = 60 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to two-wire, g_{4-2}	6	relative to 0 dBm, 1.0 kHz. E_G=0 V				
		0.3 kHz < f < 3.4 kHz	-0.2		0.1	dB
		f = 8 kHz, 12 kHz,	-1.0		0	dB
		16 kHz	-2.0		0	dB
Four-wire to four-wire, g_{4-4}	6	relative to 0 dBm, 1.0 kHz, E_G=0 V 0.3 kHz < f < 3.4 kHz	-0.2		0.1	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	6	0 dBm, 1.0 kHz, Note 5				
$G_{2-4} = 20 \bullet \text{Log}\left\|\frac{V_{TX}}{V_{TR}}\right\|; E_{RX} = 0$			-0.2		0.2	dB
		PTG = AGND	-6.22	-6.02	-5.82	dB
Four-wire to two-wire, G_{4-2}	6	0 dBm, 1.0 kHz, Note 6				
$G_{4-2} = 20 \bullet \text{Log}\left\|\frac{V_{TR}}{E_{RX}}\right\|; E_G = 0$			-0.2		0.2	dB
Gain tracking						
Two-wire to four-wire	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +0 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Four-wire to two-wire	6	Ref. -10 dBm, 1.0 kHz,				
		-40 dBm to +0 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Noise						
Idle channel noise at two-wire		C-message weighting			12	dBrnC
(TIPX-RINGX) or four-wire (V_{TX}) output		Psophometrical weighting Note 8			-78	dBmp
Harmonic distortion						
Two-wire to four-wire	6	0 dBm		-67	-50	dB
Four-wire to two-wire		0.3 kHz < f < 3.4 kHz		-67	-50	dB
Battery feed characteristics						
Constant loop current, I_{LC}		$I_{LC} = \frac{1\,000}{R_{LC}} - 4$ (mA)				
		R_{LC} in kΩ				
		18mA ≤ I_{LC} ≤ 30 mA	0.92 I_{LC}	I_{LC}	1.08 I_{LC}	mA
Open circuit state loop current, I_{LOC}		R_L = 0Ω	-100	0	100	µA

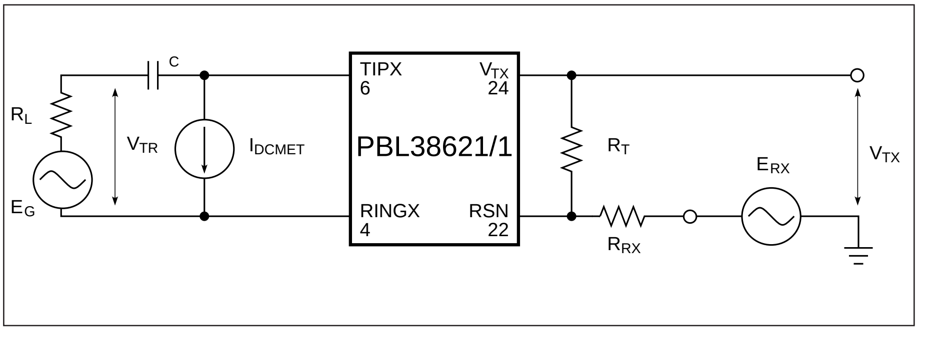


Figure 6.
Frequency response, insertion loss, gain tracking.

$\frac{1}{\omega C} << R_L$, R_L = 600 Ω

R_T = 120 kΩ, R_{RX} = 60 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Loop current detector						
Programmable threshold, I_{LTh}		$I_{LTh} = \frac{500}{R_{LD}}$ R_{LD} in kΩ, I_{LThmin} = 5 mA	$0.9 \cdot I_{LTh}$	I_{LTh}	$1.1 \cdot I_{LTh}$	mA
Ground key detector						
Ground key detector threshold $(I_{RINGX}-I_{TIPX})/2$			5	8	11	mA
Ring trip comparator						
Offset voltage, ΔV_{DTR}		Source resistance, R_S = 0 Ω	-20	0	20	mV
Input bias current, I_B		$I_B = (I_{DT} + I_{DR})/2$	-50	-20	200	nA
Input common mode range, V_{DT}, V_{DR}			V_{Bat}+1		-1	V
Ring relay driver						
Saturation voltage, V_{OL}		I_{OL} = 50 mA		0.3	0.5	V
Off state leakage current, I_{Lk}		V_{OH} = 12 V			10	µA
Digital inputs (C1, C2, C3)						
Input low voltage, V_{IL}			0		0.8	V
Input high voltage, V_{IH}			2.5		V_{CC}	V
Input low current, I_{IL}		V_{IL} = 0.8			-50	µA
Input high current, I_{IH}		V_{IH} = 2.5 V			50	µA
Detector output (DET)						
Output low voltage		I_{OL} = 0.5 mA			0.5	V
Internal pull-up resistor				5		kΩ
Power dissipation (V_{Bat} = -48V, V_{BAT2} = -17V)						
P_1		Open circuit state, C1, C2, C3 = 0, 0, 0		10		mW
P_2		Active state, C1, C2, C3 = 0, 1, 0 Longitudinal current = 0 mA, I_L=0 mA (on-hook)		60		mW
P_3		R_L = 300 Ω (off-hook)		290		mW
P_4		R_L = 500 Ω (off-hook)		145		mW
Power supply currents (V_{Bat} = -48V)						
V_{CC} current, I_{CC}		Open circuit state		0.95		mA
V_{Bat} current, I_{Bat}				-0.1		mA
V_{CC} current, I_{CC}		Active state		2.4		mA
V_{Bat} current, I_{Bat}		On-hook, Long Current = 0 mA		-1.0		mA
Power supply rejection ratios						
V_{CC} to 2- or 4-wire port		Active State	30	42		dB
V_{Bat} to 2- or 4-wire port		f = 1 kHz, V_n = 100mV	36	45		dB
V_{Bat2} to 2- or 4-wire port			40	60		dB
RFI rejection	7	50 kHz ≤ f ≤ 100 MHz		t.b.d		
Temperature guard						
Junction threshold temperature, T_{JG}				145		°C

Notes

1. The overload level can be adjusted with the resistor R_{OV} for higher levels e.g. min 3.1 V and is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:
   $Z_{TRX} = Z_T/|G_{2-4}\,\alpha_{RSN}|$ where:
   Z_{TRX} = impedance between the TIPX and RINGX terminals
   Z_T = programming network between the V_{TX} and RSN terminals
   G_{2-4S} = transmit gain, nominally = 1 (or 0.5 see pin 1)
   α_{RSN} = receive current gain, nominally = -200 (current defined as positive flowing into the receivesumming node, RSN, and when flowing from tip to ring).
3. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground.
4. The overload level can be adjusted with the resistor R_{OV} for higher levels e.g. min 3.1 V and is specified at the four-wire transmit port, V_{TX}, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2-4} = 1$ (or 0.5 see pin 1)
5. Pin 1 = Open sets transmit gain to nom. 0.0dB
   Pin 1 = AGND sets transmit gain to nom. -6.02 dB
   Secondary protection resistors R_F and tertiary protection resistors R_P impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for $R_F = R_P = 0$.
6. The specified insertion loss tolerance does not include errors caused by external components.
7. The level is specified at the two-wire port.
8. The two-wire idle noise is specified with the port terminated in 600 ohms (R_L) and with the four-wire receive port grounded ($E_{RX} = 0$; see figure 6).
   The four-wire idle noise at V_{TX} is specified with the two-wire port terminated in 600 Ω (R_L). The noise specification is referenced to a 600 Ω impedance level at V_{TX}. The four-wire receive port is grounded ($E_{RX} = 0$).

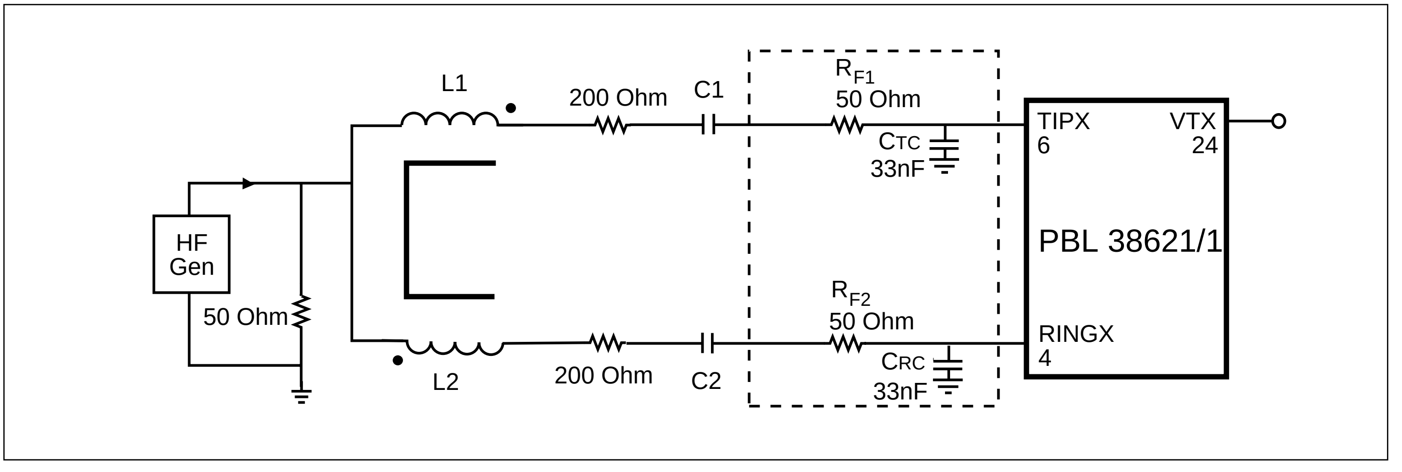


Figure 7. RFI Test Circuit.

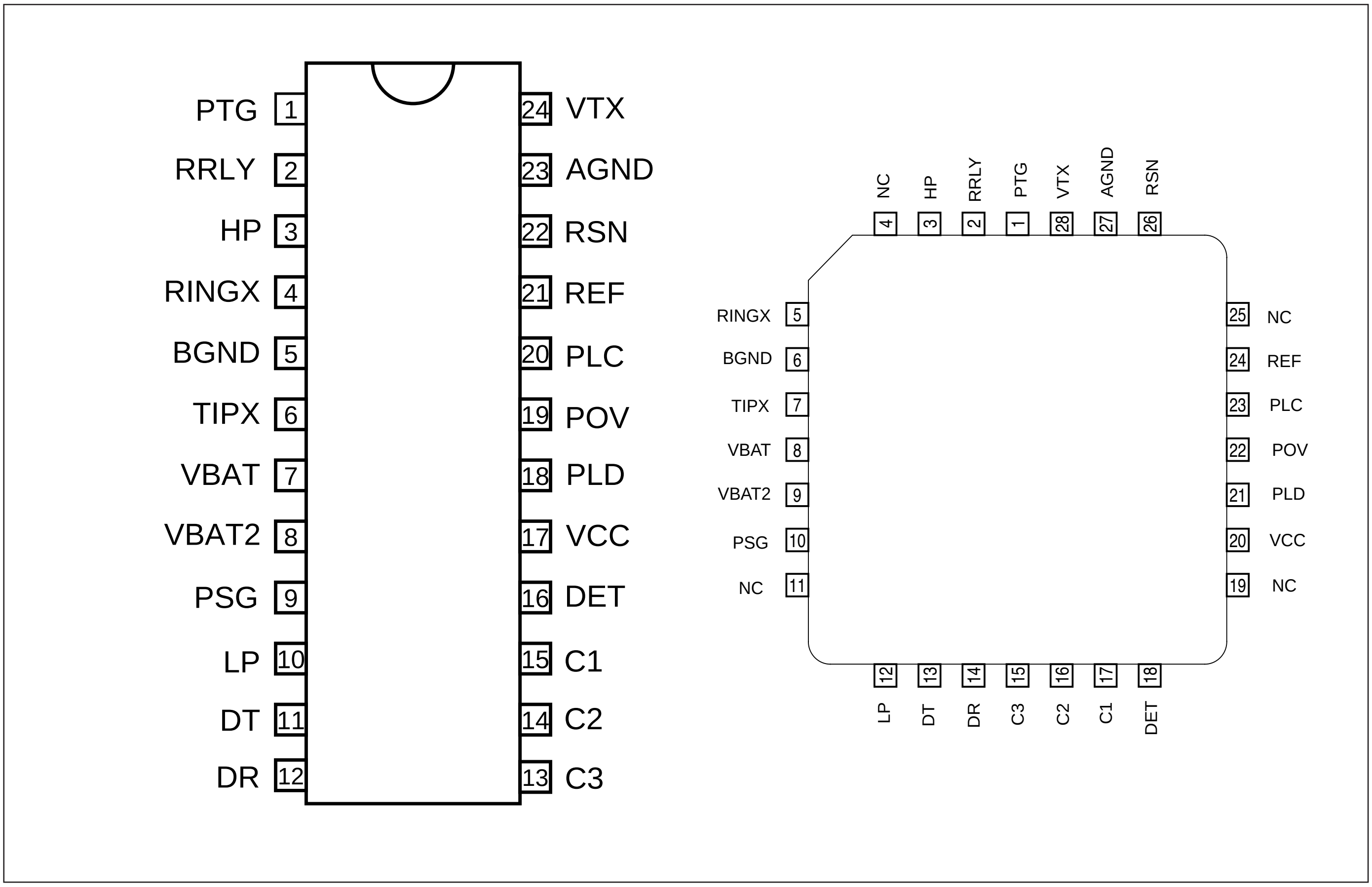


Figure 8. Pin configuration, 24-pin SOIC and 28 pin PLCC package, top view.

Pin Description

Refer to figure 8. Note: All pin number references in the text and figures refer to the 24-pin SOIC unless otherwise specified.

SOIC	Symbol	Description
1	PTG	**P**rog. **T**ransmit **G**ain. Left open transmit gain = 0.0 dB, connected to AGND transmit gain = -6.02 dB.
2	RRLY	**R**ing **R**elay driver output. The relay coil may be connected to maximum +14V.
3	HP	Connection for **H**igh **P**ass filter capacitor, CHP. Other end of CHP connects to TIPX (pin 6).
4	RINGX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relay).
5	BGND	**B**attery **G**rou**nd**, should be tied together with AGND (pin 23).
6	TIPX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relay).
7	VBAT	**Bat**tery supply **V**oltage. Negative with respect to GND (pins 5 and 23).
8	VBAT2	An optional second (2) **Bat**tery **V**oltage connects to this pin via an external diode.
9	PSG	**P**rogrammable **S**aturation **G**uard. The resistive part of the DC feed characteristic is programmed by a resistor connected from this pin to VBAT.
10	LP	Connection for **L**ow **P**ass filter capacitor, CLP. Other end of CLP connects to VBAT (pin 7).
11	DT	Input to the ring trip comparator. With DR more positive than DT the detector output, DET (pin 16), is at logic level low, indicating off-hook condition. The external ring trip network connects to this two inputs.
12	DR	Input to the ring trip comparator. With DR more positive than DT the detector output, DET (pin16), is at logic level low, indicating off-hook condition. The external ring trip network connects to this input.
13 14 15	C3 C2 C1	C1, C2 and C3 are TTL compatible digital inputs (internal pull-up) controlling the SLIC operating states. Refer to section "Operating states" for details.

16	DET	**Det**ector output. Active low when indicating loop detection and ring trip, active high when indicating ground key detection.
17	VCC	+5 V power supply.
18	PLD	**P**rogrammable **L**oop **D**etector threshold. The loop detection threshold is programmed by a resistor connected from this pin to AGND (pin 23).
19	POV	**P**rogrammable **O**verhead **V**oltage. If pin is left open: The overhead voltage is internally set to 1.1 V in off- and on-hook. If a resistor is connected between this pin and AGND: the overhead voltage can be set to higher values.
20	PLC	**P**rog. **L**ine **C**urrent, the constant current part of the DC feed characteristic is programmed by a resistor connected from this pin to AGND (Pin 23)
21	REF	A **Ref**erence, 49.9 kΩ, resistor should be connected from this pin to AGND (Pin 23).
22	RSN	**R**eceive **S**umming **N**ode. 200 times the AC-current flowing into this pin equals the metallic (transversal) AC-current flowing from RINGX (pin 4) to TIPX (pin 6). Programming networks for two-wire impedance and receive gain connect to the receive summing node. A resistor should be connected from this pin to AGND (pin 23).
23	AGND	Analog Ground, should be tied together with BGND (pin 5).
24	VTX	Transmit vf output. The AC voltage difference between TIPX (pin 6) and RINGX (pin 4), the AC metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of one (or one half, see pin 1). The two-wire impedance programming network connects between VTX and RSN (pin 22).

SLIC Operating States

State	C3	C2	C1	SLIC operating state	Active detector
0	0	0	0	Open circuit	-
1	0	0	1	Ringing state	Ring trip detector (active low)
2	0	1	0	Active state	Loop detector (active low)
3	0	1	1	Not applicable	-
4	1	0	0	Not applicable	-
5	1	0	1	Active state	Ground key detector (active high)
6	1	1	0	Active reverse	Loop detector (active low)
7	1	1	1	Active reverse	Ground key detector (active high)

Table 1. SLIC operating states.

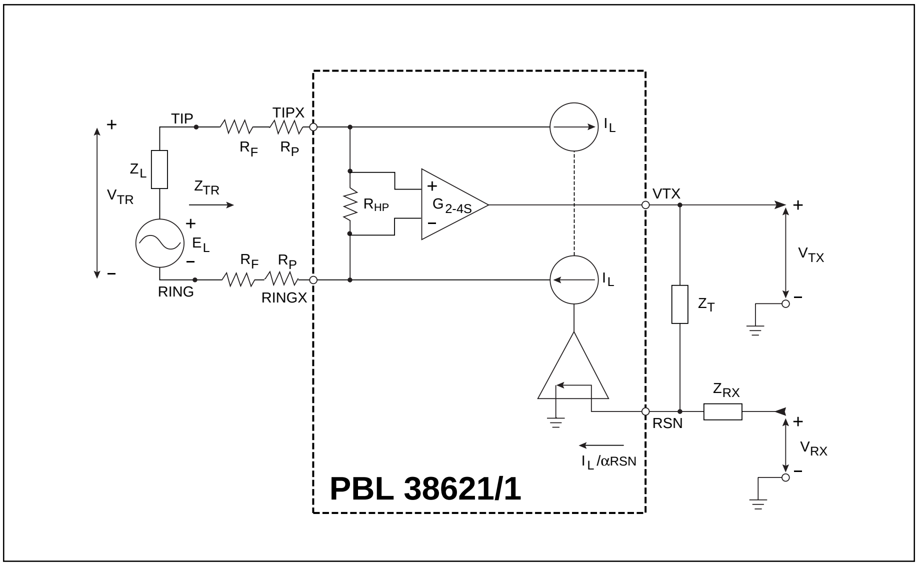


Figure 9. Simplified ac transmission circuit.

Functional Description and Applications Information

Transmission

General

A simplified ac model of the transmission circuits is shown in figure 9. Circuit analysis yields:

$$V_{TR} = \frac{V_{TX}}{G_{2-4S}} + I_L \cdot (2R_F + 2R_P) \quad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{\alpha_{RSN}} \quad (2)$$

$$V_{TR} = E_L - I_L \cdot Z_L \quad (3)$$

where:

- V_{TX} is a ground referenced version of the ac metallic voltage between the TIPX and RINGX terminals.
- $G_{2\text{-}4S}$ is the programmable SLIC two-wire to four-wire gain (transmit direction). See note below.
- V_{TR} is the ac metallic voltage between tip and ring.
- E_L is the line open circuit ac metallic voltage.
- I_L is the ac metallic current.
- R_F is a fuse resistor.
- R_P is part of the SLIC tertiary protection.
- Z_L is the line impedance.
- Z_T determines the SLIC TIPX to RINGX impedance at voice frequencies.
- Z_{RX} controls four- to two-wire gain.
- V_{RX} is the analog ground referenced receive signal.
- α_{RSN} is the receive summing node current to metallic loop current gain.

Note that the SLICs two-wire to four-wire gain, $G_{2\text{-}4S}$, is user programmable between two fix values. Refer to the datasheets for values on $G_{2\text{-}4S}$.

Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse and protection resistors R_F and R_P let:

$V_{RX} = 0$.

From (1) and (2):

$$Z_{TR} = \frac{Z_T}{\alpha_{RSN} \cdot G_{2-4S}} + 2R_F + 2R_P$$

Thus with Z_{TR}, α_{RSN}, $G_{2\text{-}4S}$, R_P and R_F known:

$$Z_T = \alpha_{RSN} \cdot G_{2-4S} \cdot (Z_{TR} - 2R_F - 2R_P)$$

Two-Wire to Four-Wire Gain

From (1) and (2) with $V_{RX} = 0$:

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T / \alpha_{RSN}}{\dfrac{Z_T}{\alpha_{RSN} \cdot G_{2-4S}} + 2R_F + 2R_P}$$

Four-Wire to Two-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{\dfrac{Z_T}{\alpha_{RSN}} + G_{2-4S} \cdot (Z_L + 2R_F + 2R_P)}$$

For applications where $Z_T/(\alpha_{RSN} \bullet G_{2\text{-}4S}) + 2R_F + R_P$ is chosen to be equal to Z_L the expression for $G_{4\text{-}2}$ simplifies to:

$$G_{4-2} = -\frac{Z_T}{Z_{RX}} \cdot \frac{1}{2G_{2-4S}}$$

Four-Wire to Four-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{G_{2-4S} \cdot (Z_L + 2R_F + 2R_P)}{\dfrac{Z_T}{\alpha_{RSN}} + G_{2-4S} \cdot (Z_L + 2R_F + 2R_P)}$$

Hybrid Function

The hybrid function can easily be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 10. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 (E_L = 0)$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from: *Figure 10. Hybrid function.*

$$Z_B = -R_{TX} \cdot \frac{V_{RX}}{V_{TX}} = R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{\dfrac{Z_T}{\alpha_{RSN}} + G_{2-4S} \cdot (Z_L + 2R_F + 2R_P)}{G_{2-4S} \cdot (Z_L + 2R_F + 2R_P)}$$

When choosing R_{TX}, make sure the out-put load of the VTX terminal is >20 kΩ.

If calculation of the Z_B formula above yields a balance network containing an inductor, an alternate method is recommended. Contact Ericsson Components for assistance.

The PBL 38621/1 SLIC may also be used together with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accom-modate different line impedances without change of hardware. In addition, the transmit and receive gain may be ad-justed. Please, refer to the programm-able CODEC/filter data sheets for design information.

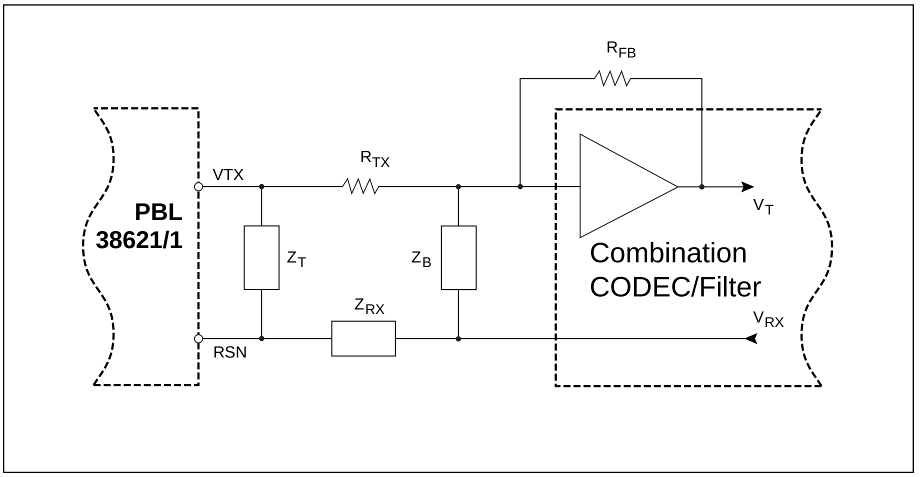


Figure 10. Hybrid function.

Longitudinal Impedance

A feed back loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase.

Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.

The SLIC longitudinal impedance per wire, Z_{LoT} and Z_{LoR}, appears as typically 20 Ω to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission.

Capacitors C_{TC} and C_{RC}

The capacitors designated C_{TC} and C_{RC} in figure 11, connected between TIPX and ground as well as between RINGX and ground, are recommended as an addition to the overvoltage protection network. Very fast transients, appearing on tip and ring, may pass by the active components in the overvoltage protection network before they have had time to activate and could damage the SLIC. C_{TC} and C_{RC} short such very fast transients to ground. The recommended value for C_{TC} and C_{RC} is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss. C_{TC} and C_{RC} contribute to a metallic impedance of $1/(\pi \bullet f \bullet C_{TC}) = 1/(\pi \bullet f \bullet C_{RC})$, a TIPX to ground impedance of $1/(2 \bullet \pi \bullet f \bullet C_{TC})$ and a RINGX to ground impedance of $1/(2 \bullet \pi \bullet f \bullet C_{RC})$.

AC - DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between terminals HP and TIPX provides the separation of the ac signal from the dc part. C_{HP} positions the low end frequency response break point of the ac loop in the SLIC. Refer to table 1 for a recommended value of C_{HP}.
Example: A C_{HP} value of 47 nF will position the low end frequency response 3dB break point of the ac loop at 5,6 Hz (f_{3dB}) according to $f_{3dB} = 1/(2 \cdot \pi \cdot R_{HP} \cdot C_{HP})$ where $R_{HP} = 600$ kΩ.

High-Pass Transmit Filter

The capacitor C_{TX} in figure 11 connected between the VTX output and the CODEC/filter forms, together with R_{TX} and/or the input impedance of a pro-grammable CODEC/filter, a high-pass RC filter. It is recommended to position the 3 dB break point of this filter between 30 and 80 Hz to get a faster response for the dc steps that may occur at DTMF signalling.

Capacitor C_{LP}

The capacitor C_{LP}, which connects between the terminals CLP and VBAT, positions the high end frequency break point of the low pass filter in the dc loop in the SLIC. C_{LP} together with C_{HP} and Z_T (see section Two-Wire Impedance) forms the total two wire output impedance of the SLIC. The choise of these programmable components have an influence on the power supply rejection ratio (PSRR) from VBAT to the two wire side at sub-audio frequencies. At these frequencies capacitor C_{LP} also influences the transversal to longitudinal balance in the SLIC. Table 1 suggests a suitable value on C_{LP}. The typical value of the transversal to longitudinal balance (T-L bal.) at 200Hz is given in table 1 for the chosen value on C_{LP}.

R_{FEED} (Ω)	***R_{SG} (kΩ)***	***C_{LP} (nF)***	***T-L bal. (dB)***	***C_{HP} (nF)***
2•25	0	150	-46	47

Table 1. R_{SG}, C_{LP} and C_{HP} values for constant current feeding characteristics.

For values outside table 1, please contact Ericsson Components for assistance.

Battery Feed

The PBL 38621/1 SLIC emulate a battery characteristic with current limitation adjustable between 18 mA and 30 mA.The open loop voltage measured between the TIPX and RINGX terminals is tracking the battery voltage VBAT. The signalling headroom, or overload level V_{TRO}, is programmable with a resistor R_{OV} conected between terminal POV on the SLIC and ground. Please contact Ericsson Components for values on R_{OV}.
The battery voltage overhead, V_{OH}, depends on the programmed signal overload level. V_{OH} defines the TIPX to RINGX voltage at open loop conditions according to V_{TR}(at I_L = 0 mA) = $|V_{Bat}| - V_{OH}$.
Refer to table 2 for the typical value on V_{OH}.

SLIC	***V_{OH}(typ) [V]***
PBL 38621/1	$3,6+V_{TROprog}$

Table 2. Battery overhead.

The current limit (reference C in figure 12) is adjusted by connecting a resistor, R_{LC}, between terminal PLC and ground according to the equation:

$$R_{LC} = \frac{1000}{I_{Lprog} + 4}$$

where R_{LC} is in kΩ for I_{Lprog} in mA.

A second, lower battery voltage may be connected to the device at terminal VBAT2 to reduce short loop power dissipation. The SLIC automatically switches between the two battery supply voltages without need for external control. The silent battery switching occurs when the line voltage passes the value

$|VB2| - 40 \bullet I_L - V_{TROProg} - 3.6.$

For correct functionality it is important to connect the terminal VBAT2 to the second power supply via the diode D_{VB2} in figure 11. A diode D_{BB} connected between terminal VB and the VB2 power supply, see figure 11, will make sure that the SLIC continues to work on the second battery even if the first battery voltage disappears.

If a second battery voltage is not used, VBAT2 is connected to VBAT on the SLIC and D_{BB} and D_{VB2} are removed.

CODEC Receive Interface

The PBL 38621/1 SLIC have got a completely new receive interface at the four wire side which makes it possible to reduce the number of capacitors in the applications and to fit both single and dual battery feed CODECs. The RSN terminal, connecting to the CODEC receive output via the resistor R_{RX}, is dc biased with +1,25V. This makes it possible to compensate for currents floating due to dc voltage differences between RSN and the CODEC output without using any capacitors. This is done by connecting a resistor R_R between the RSN terminal and ground. With current directions defined as in figure 13, current summation gives:

$$-I_{RSN} = I_{RT} + I_{RRX} + I_{RR} =$$

$$\frac{1{,}25}{R_T} + \frac{1{,}25 - V_{CODEC}}{R_{RX}} + \frac{1{,}25}{R_R}$$

where V_{CODEC} is the reference voltage of the CODEC at the receive output.

From this equation the resistor R_R can be calculated as

$$R_R = \frac{1{,}25}{-I_{RSN} - \frac{1{,}25}{R_T} - \frac{1{,}25 - V_{CODEC}}{R_{RX}}}$$

For the value on I_{RSN}, see table 3.
The resistor R_R has no influence on the ac transmission.

SLIC	***I_{RSN} [µA]***
PBL 38621/1	-55

Table 3. The SLIC internal bias current with the direction of the current defined as positive when floating into the terminal RSN.

Analog Temperature Guard

The widely varying environmental conditions in which SLICs operate may lead to the chip temperature limitations being exceeded. The PBL 38621/1 SLIC reduce the dc line current when the chip temperature reaches approximately 145°C and increases it again automatically when the temperature drops. Accordingly transmission is not lost under high ambient temperature conditions.

The detector output, DET, is forced to a logic low level when the temperature guard is active.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status through a common output, DET. The detector to be connected to DET is selected via the three bit wide control interface C1, C2 and C3. Please refer to section Control Inputs for a description of the control interface.

Loop Current Detector

The loop current detector is indicating that the telephone is off hook and that current is flowing in the loop by putting the output DET to a logical low level when selected. The loop current threshold value, I_{LTh}, at which the loop current detector changes state is programmable by selecting the value of resistor R_{LD}. R_{LD} connects between pin PLD and ground and is calculated according to

$$R_{LD} = \frac{500}{I_{LTh}}$$

The current detector is internally filtered and is not influenced by the ac signal at the two wire side.

Ground Key Detector

The ground key detector is indicating when the ground key is pressed (active) by putting the output pin DET to a logical high level when selected. The ground key detector circuit senses the difference in TIPX and RINGX currents. When the current at the RINGX side exceeds the current at the TIPX side with the threshold value the detector is triggered. For threshold current values, please refer to the datasheet.

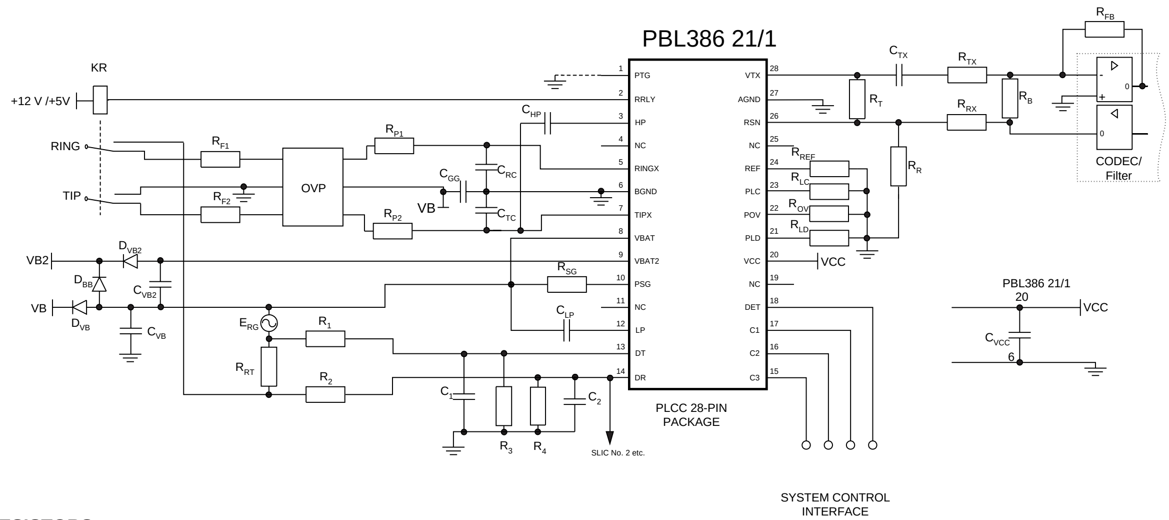
Ring Trip Detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR. The ringing source can be balanced or unbalanced superimposed on V_{Bat}. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no dc current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while the ring relay is energized, dc current flows and the comparator input voltage reverses polarity.

Figure 11 gives an example of a ring trip detection network. This network is applicable, when the ring voltage superimposed on V_{Bat} is injected on the ring lead of the two-wire port. The dc voltage across sense resistor R_{RT} is monitored by the ring trip comparator input DT and DR via the network R_1, R_2, R_3, R_4, C_1 and C_2. With the line on-hook (no dc current) DT is more positive than DR and the DET output will report logic level high, i.e. the detector is not tripped. When the line goes off-hook, while ringing, a dc current will flow through the loop including sense resistor R_{RT} and will cause input DT to become more negative than input DR. This changes output DET to logic level low, i.e. tripped detector condition. The system controller (or line card processor) responds by de-energizing the ring relay, i.e. ring trip.

Complete filtering of the 20 Hz ac component at terminal DT and DR is not necessary. A toggling DET output can be examined by a software routine to determine the duty cycle. When the DET out-put is at logic level low for more than half the time, off-hook condition is indicated.



RESISTORS:

R_{SG} = 0 Ω 1% 1/4 Ω
R_{LD} = 49,9 kΩ 1% 1/4 Ω
R_{OV} = User programmable
R_{LC} = 32,4 kΩ 1% 1/4 Ω
R_{REF} = 49,9 kΩ 1% 1/4 Ω
R_{R} = 64,9 kΩ 1% 1/4 Ω
R_{T} = 105 kΩ 1% 1/4 Ω
R_{TX} = 24,9 kΩ 1% 1/4 Ω
R_{B} = 22,1 kΩ 1% 1/4 Ω
R_{RX} = 52,3 kΩ 1% 1/4 Ω
R_{FB} Depending on CODEC/filter
R_{1} = 604 kΩ 1% 1/4 Ω
R_{2} = 604 kΩ 1% 1/4 Ω
R_{3} = 249 kΩ 1% 1/4 Ω
R_{4} = 280 kΩ 1% 1/4 Ω
R_{RT} = 330 Ω 5% 2 Ω
R_{P1} = 0 Ω 1% 1/4 Ω
R_{P2} = 0 Ω 1% 1/4 Ω
R_{F1}, R_{F2}= Line resistor, 40 Ω 1% match, e. g.
Ericsson Components PBR 51XX

CAPACITORS:

C_{VB} = 100 nF 100 V 10%
C_{VB2} = 150 nF 100 V 10%
C_{VCC} = 100 nF 10 V 10%
C_{TC} = 2,2 nF 100 V 10%
C_{RC} = 2,2 nF 100 V 10%
C_{HP} = 150 nF 100 V 10%
C_{LP} = 150 nF 100 V 10%
C_{TX} = 100 nF 10 V 10%
C_{GG} = 220 nF 100 V 10%
C_{1} = 330 nF 63 V 10%
C_{2} = 330 nF 63 V 10%

DIODES:

D_{VB} = 1N4448
D_{VB2} = 1N4448
D_{BB} = 1N4448

OVP:

Secondary protection (e. g. TI/Power Innovations TISP PBL1). The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferable a groundplane.

Figure 11. single-channel subscriber line interface with PBL 386 21/1 and combination CODEC/filter.

Relay driver

The PBL 38621/1 SLIC incorporates a ring relay driver designed as open collector (npn) with a current sinking capability of 50 mA. The drive transistor emitter is connected to BGND. The relay driver has an internal zener diode clamp for inductive kick-back voltages.

Control Inputs

The PBL 38621/1 SLIC have three TTL compatible digital control inputs, C1, C2 and C3.
A decoder in the SLIC interprets the control input condition and sets up the commanded operating state.
C1 to C3 are internal pull-up inputs.

Open Circuit State

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum and no detectors are active.

Ringing State

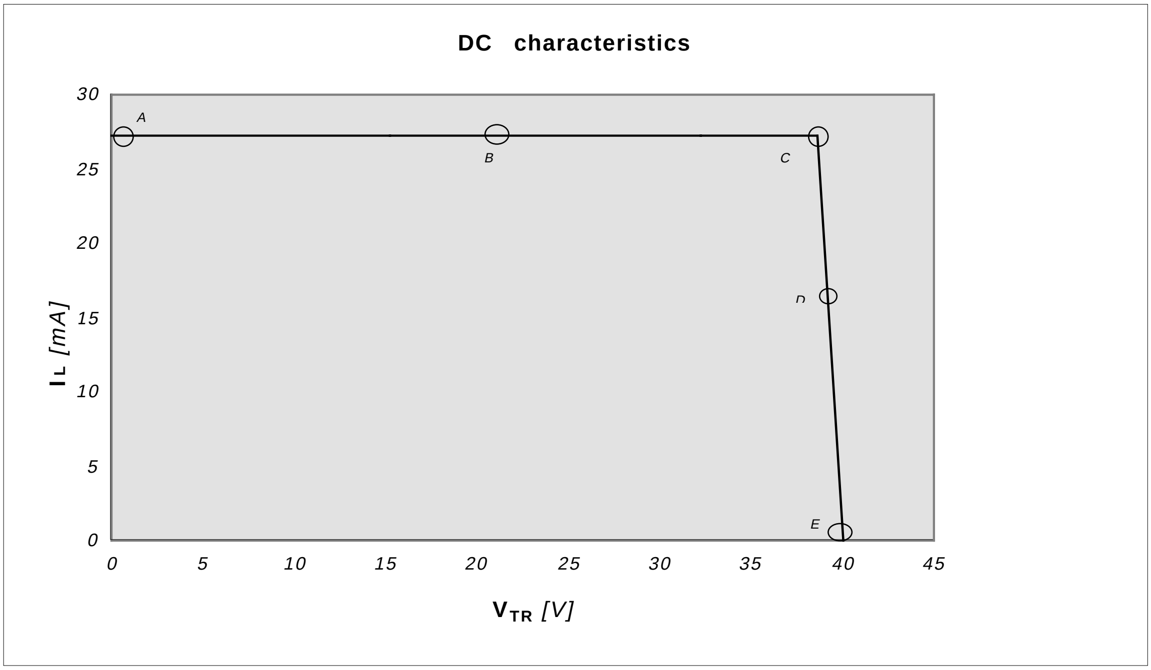
The ring relay driver and the ring trip detector are activated and the ring trip detector is indicating off hook with a logic low level at the detector output.
As the SLIC do not have any stand by state the SLIC will remain in the active normal state.

Active States

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. Vf signal transmission is normal. The loop current or the ground key detector is activated. The loop current detector is indicating off hook with a logic low level and the ground key detector is indicating active ground key with a logic high level present at the detector output.

Active Polarity Reversal State

TIPX and RINGX polarity is reversed from the Active State: RINGX is the terminal closest to ground and sources loop current while TIPX is the more negative terminal and sinks current. Vf signal transmission is



A: $I_L(@V_{TR}=0V)=I_{Lprog}$

B: Constant current

C: $V_{TR}=|V_{Bat}|-V_{OH}-50 \cdot I_{Lprog}$

D: $R_{FEED}=2 \cdot 25\ \Omega$

E: $V_{TROpen}=|V_{Bat}|-V_{OH}$

Figure 12. Battery feed characteristics (without the protection resistors on the line).

normal. The loop current or the ground key detector is activated. The loop current detector is indicating off hook with a logic low level and the ground key detector is indicating active ground key with a logic high level present at the detector output.

Overvoltage Protection

The PBL 38621/1 SLIC must be protected against overvoltages on the telephone line caused by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum allowable continuous and transient currents that may be applied to the SLIC.

Secondary Protection

The circuit shown in figure 11 utilizes series resistors together with a programmable overvoltage protector (e g TI/Power Innovations TISP PBL1), serving as a secondary protection.

The TISP PBL1 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i e the battery voltage, V_{Bat}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor, C_{GG}, is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. C_{GG} shall be placed close to the overvoltage protec-tion device. Without the capacitor even the low inductance in the track to the V_{Bat} supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F serve the dual purposes of being non- destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross.

Ericsson Components AB offers a series of thick film resistors networks (e g PBR 51-series and PBR 53-series) designed for this application.

Also devices with a built in resetable fuse function is offered (e g PBR 52-series) including positive temperature coefficient (PTC) resistors, working as resetable fuses, in series with thick film resistors.

Note that it is important to always use PTC´s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore will not protect the SLIC.

Tertiary Protection

The PBL 38621/1 SLIC features a tertiary two wire protection scheme. If the secondary protection device and the SLIC do not have their respective grounds shorted together on the printed circuit board, the protection resistors R_{P1} and R_{P2} (see figure 11) together with the SLIC's internal tertiary protection circuitry, will handle the ground voltage difference that may occur when the secondary protection circuitry is activated. This voltage difference arises due to the ground lead inductance.

Power-up Sequence

No special power-up sequence is necessary except that ground has to be present before all other power supply voltages.

Printed Circuit Board Layout

Care in PCB layout is essential for proper function. The components connecting to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the RSN pin. Ground plane surrounding the RSN pin is advisable.

Analog ground (AGND) should be connected to battery ground (BGND) on the PCB in one point.

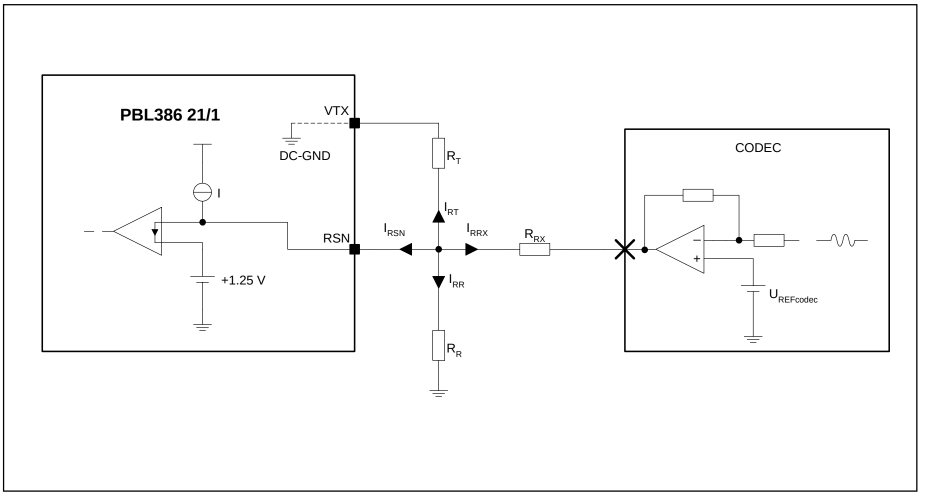


Figure 13. CODEC receive interface.

Ordering Information

Package	Temp. Range	Part No.
24 pin SOIC	-40° - +85° C	PBL 386 21/1 SO
28 pin PLCC	-40° - +85° C	PBL 386 21/1 QN

Specifications subject to change without notice.
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