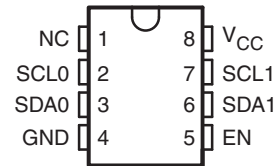


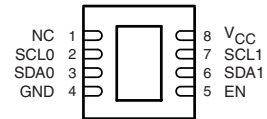
## FEATURES

- Two-Channel Bidirectional Buffers
- I<sup>2</sup>C Bus and SMBus Compatible
- Active-High Repeater-Enable Input
- Open-Drain I<sup>2</sup>C I/O
- 5.5-V Tolerant I<sup>2</sup>C I/O and Enable Input Support  
Mixed-Mode Signal Operation
- Lockup-Free Operation
- Accommodates Standard Mode and Fast Mode  
I<sup>2</sup>C Devices and Multiple Masters
- Supports Arbitration and Clock Stretching  
Across the Repeater
- Powered-Off High-Impedance I<sup>2</sup>C Pins
- Latch-Up Performance Exceeds 100 mA Per  
JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

D, DCT, DGK, OR PW PACKAGE  
(TOP VIEW)



DRG PACKAGE  
(TOP VIEW)



NC – No internal connection

## DESCRIPTION/ORDERING INFORMATION

This dual bidirectional I<sup>2</sup>C buffer is operational at 2.3-V to 3.6-V  $V_{CC}$ .

The PCA9515A is a BiCMOS integrated circuit intended for I<sup>2</sup>C bus and SMBus systems applications. The device contains two identical bidirectional open-drain buffer circuits that enable I<sup>2</sup>C and similar bus systems to be extended without degradation of system performance. Both buffers specifically are designed to support the standard low-level-contention arbitration of the I<sup>2</sup>C bus and support clock stretching.

The PCA9515A buffers both the serial data (SDA) and serial clock (SCL) signals on the I<sup>2</sup>C bus, while retaining all the operating modes and features of the I<sup>2</sup>C system. This enables two buses of 400-pF bus capacitance to be connected in an I<sup>2</sup>C application.

The I<sup>2</sup>C bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9515A enables the system designer to isolate two halves of a bus, accommodating more I<sup>2</sup>C devices or longer trace lengths.

The PCA9515A has an active-high enable (EN) input with an internal pullup, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It never should change state during an I<sup>2</sup>C operation, because disabling during a bus operation hangs the bus, and enabling part way through a bus cycle could confuse the I<sup>2</sup>C parts being enabled. The EN input should change state only when the global bus and the repeater port are in an idle state, to prevent system failures.

The PCA9515A also can be used to run two buses: one at 5-V interface levels and the other at 3.3-V interface levels, or one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated when the 400-kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz, because of the delays that are added by the repeater.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
–40°C to 85°C	MSOP – DGK	Reel of 2500	PCA9515ADGKR	7B_
		Tube of 75	PCA9515AD	PD515A
	SOIC – D	Reel of 2500	PCA9515ADR	
		Reel of 250	PCA9515ADT	
	SON – DRG	TBD	PCA9515ADRGR	
	SSOP – DCT	Reel of 3000	PCA9515ADCTR	7BG_ _ _
		Reel of 250	PCA9515ADCTT	
	TSSOP – PW	Tube of 150	PCA9515APW	PD515A
		Reel of 2000	PCA9515APWR	
		Reel of 250	PCA9515APWT	

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.  
 DGK: The actual top-side marking has one additional character that designates the assembly/test site.

The output low levels for each internal buffer are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV or more below the output low level, when the output internally is driven low. This prevents a lockup condition from occurring when the input low condition is released.

Two or more PCA9515A devices cannot be used in series. The PCA9515A design does not allow this configuration. Because there is no direction pin, slightly different valid low-voltage levels are used to avoid lockup conditions between the input and the output of each repeater. A valid low applied at the input of a PCA9515A is propagated as a buffered low with a slightly higher value on the enabled outputs. When this buffered low is applied to another PCA9515A-type device in series, the second device does not recognize it as a valid low and does not propagate it as a buffered low again.

The device contains a power-up control circuit that sets an internal latch to prevent the output circuits from becoming active until V<sub>CC</sub> is at a valid level (V<sub>CC</sub> = 2.3 V).

As with the standard I<sup>2</sup>C system, pullup resistors are required to provide the logic high levels on the buffered bus. The PCA9515A has standard open-collector configuration of the I<sup>2</sup>C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard Mode and Fast Mode I<sup>2</sup>C devices in addition to SMBus devices. Standard Mode I<sup>2</sup>C devices only specify 3 mA in a generic I<sup>2</sup>C system where Standard Mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.

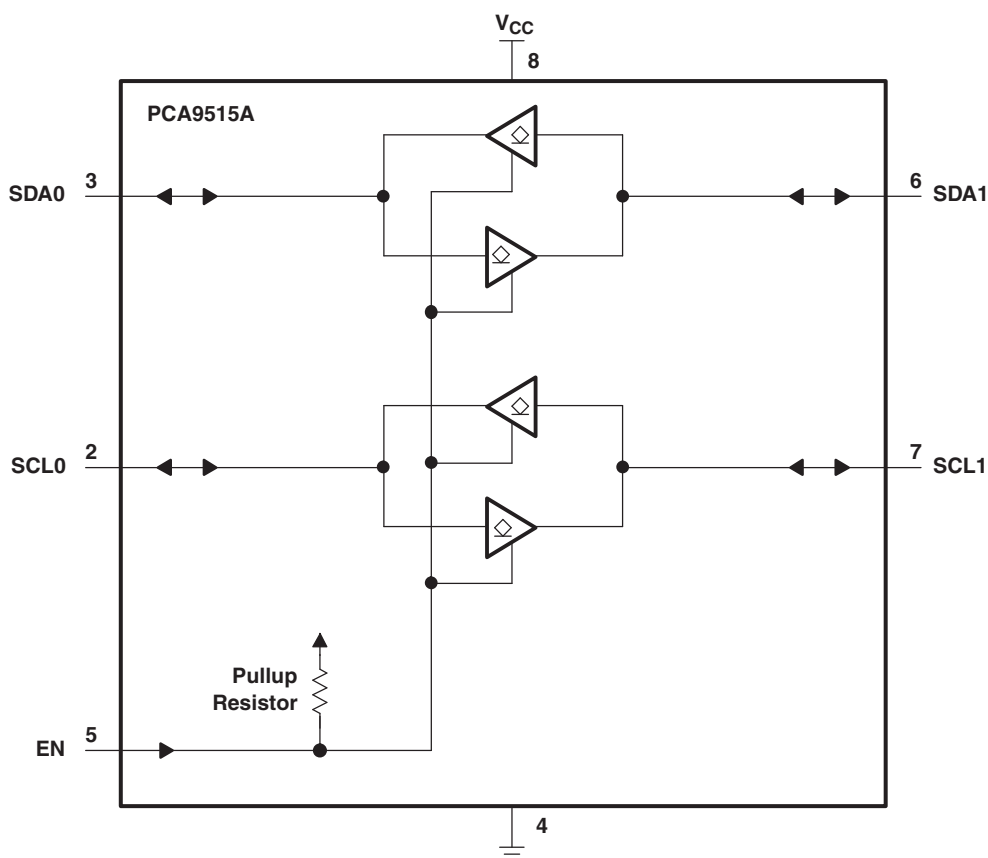
### TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	NC	No internal connection
2	SCL0	Serial clock bus 0
3	SDA0	Serial data bus 0
4	GND	Supply ground
5	EN	Active-high repeater enable input
6	SDA1	Serial data bus 1
7	SCL1	Serial clock bus 1
8	V <sub>CC</sub>	Supply power

### FUNCTION TABLE

INPUT EN	FUNCTION
L	Outputs disabled
H	SDA0 = SDA1, SCL0 = SCL1

### LOGIC DIAGRAM (POSITIVE LOGIC)



# PCA9515A DUAL BIDIRECTIONAL I<sup>2</sup>C BUS AND SMBus REPEATER

SCPS150B–DECEMBER 2005–REVISED OCTOBER 2007

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	–0.5	7	V
V <sub>I</sub>	Enable input voltage range <sup>(2)</sup>	–0.5	7	V
V <sub>I/O</sub>	I <sup>2</sup> C bus voltage range <sup>(2)</sup>	–0.5	7	V
I <sub>IK</sub>	Input clamp current		–50	mA
I <sub>OK</sub>	Output clamp current		–50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	D package	97	°C/W
		DCT package	220	
		DGK package	172	
		DRG package	TBD	
		PW package	149	
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	3.6	V
V <sub>IH</sub>	High-level input voltage	SDA and SCL inputs	0.7 × V <sub>CC</sub>	5.5
		EN input	2	5.5
V <sub>IL</sub> <sup>(1)</sup>	Low-level input voltage	SDA and SCL inputs	–0.5	0.3 × V <sub>CC</sub>
		EN input	–0.5	0.8
V <sub>ILc</sub> <sup>(1)</sup>	SDA and SCL low-level input voltage contention	–0.5	0.4	V
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V	6	mA
		V <sub>CC</sub> = 3 V	6	
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

- (1) V<sub>IL</sub> specification is for the EN input and the first low level seen by the SDAx and SCLx lines. V<sub>ILc</sub> is for the second and subsequent low levels seen by the SDAx and SCLx lines. V<sub>ILc</sub> must be at least 70 mV below V<sub>OL</sub>.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA		2.3 V to 3.6 V			-1.2	V	
V <sub>OL</sub>	Low-level output voltage	SDAx, SCLx	I <sub>OL</sub> = 20 μA or 6 mA	2.3 V to 3.6 V	0.47	0.52	0.6	V	
V <sub>OL</sub> - V <sub>ILc</sub>	Low-level input voltage below low-level output voltage	SDAx, SCLx	I <sub>I</sub> = 10 μA	2.3 V to 3.6 V			70	mV	
I <sub>CC</sub>	Quiescent supply current	Both channels high, SDAx = SCLx = V <sub>CC</sub>		2.7 V		0.5	3	mA	
				3.6 V		0.5	3		
		Both channels low, SDA0 = SCL0 = GND and SDA1 = SCL1 = open; or SDA0 = SCL0 = open and SDA1 = SCL1 = GND		2.7 V		1	4		
				3.6 V		1	4		
In contention, SDAx = SCLx = GND		2.7 V		1	4				
		3.6 V		1	4				
I <sub>I</sub>	Input current	SDAx, SCLx	V <sub>I</sub> = 3.6 V	2.3 V to 3.6 V				±1	μA
			V <sub>I</sub> = 0.2 V					3	
		EN	V <sub>I</sub> = V <sub>CC</sub>					±1	
			V <sub>I</sub> = 0.2 V					-10	
I <sub>off</sub>	Leakage current	SDAx, SCLx	V <sub>I</sub> = 3.6 V	0 V				0.5	μA
			V <sub>I</sub> = GND					0.5	
I <sub>I(ramp)</sub>	Leakage current during power up	SDAx, SCLx	V <sub>I</sub> = 3.6 V	0 V to 2.3 V				1	μA
C <sub>in</sub>	Input capacitance	EN	V <sub>I</sub> = 3 V or GND	3.3 V		7	9	pF	
		SDAx, SCLx		EN = H	3.3 V		7		9

(1) All typical values are at nominal supply voltage (V<sub>CC</sub> = 2.5 V or 3.3 V) and T<sub>A</sub> = 25°C.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t <sub>su</sub>	Setup time, EN↑ before Start condition	100		100		ns
t <sub>h</sub>	Hold time, EN↓ after Stop condition	130		100		ns

## Switching Characteristics

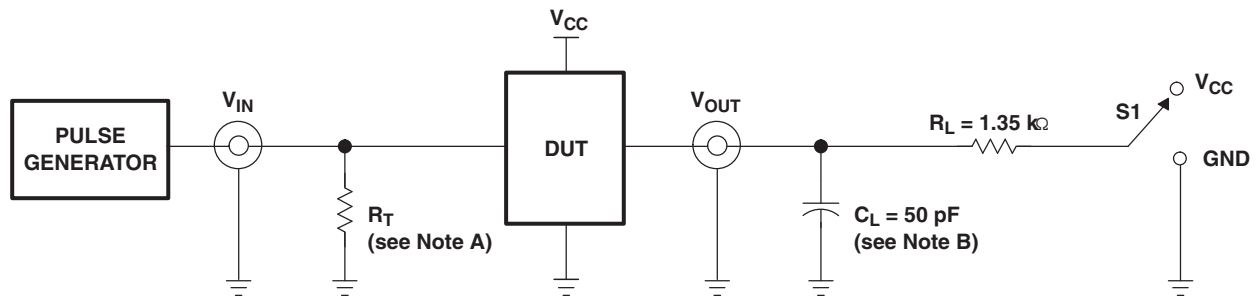
over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V			V <sub>CC</sub> = 3.3 V ± 0.3 V			UNIT
				MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
t <sub>PZL</sub>	Propagation delay time <sup>(2)</sup>	SDA0, SCL0 or SDA1, SCL1	SDA1, SCL1 or SDA0, SCL0	45	82	130	45	68	120	ns
t <sub>PLZ</sub>				33	113	190	33	102	180	
t <sub>tHL</sub>	Output transition time <sup>(2)</sup> (SDAx, SCLx)	80%	20%	57			58			ns
t <sub>tLH</sub>		20%	80%	148			147			

(1) All typical values are at nominal supply voltage (V<sub>CC</sub> = 2.5 V or 3.3 V) and T<sub>A</sub> = 25°C.

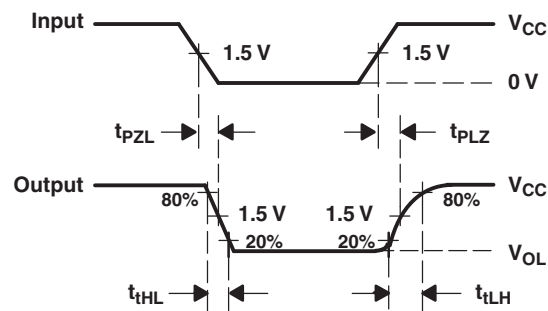
(2) Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLZ</sub> /t <sub>pZL</sub>	V <sub>CC</sub>

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- A. R<sub>T</sub> termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.
- B. C<sub>L</sub> includes probe and jig capacitance.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, slew rate ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
- F. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- G. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

Figure 1. Test Circuit and Voltage Waveforms

## APPLICATION INFORMATION

A typical application is shown in Figure 2. In this example, the system master is running on a 3.3-V bus, while the slave is connected to a 5-V bus. Both buses run at 100 kHz, unless the slave bus is isolated, and then the master bus can run at 400 kHz. Master devices can be placed on either bus.

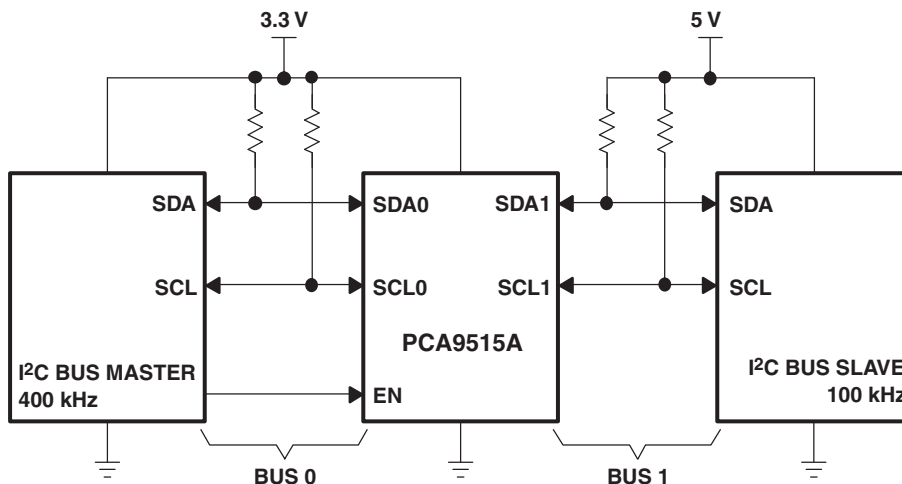


Figure 2. Typical Application

The PCA9515A is 5.5-V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9515A is pulled low by a device on the I<sup>2</sup>C bus, a CMOS hysteresis-type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side also to go low. The side driven low by the PCA9515A typically is at  $V_{OL} = 0.5$  V.

Figure 3 and Figure 4 show the waveforms that are seen in a typical application. If the bus master in Figure 2 writes to the slave through the PCA9515A, Bus 0 has the waveform shown in Figure 3. This looks like a normal I<sup>2</sup>C transmission until the falling edge of the eighth clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it low through the PCA9515A. Because the  $V_{OL}$  of the PCA9515A typically is around 0.5 V, a step in the SDA is seen. After the master has transmitted the ninth clock pulse, the slave releases the data line.

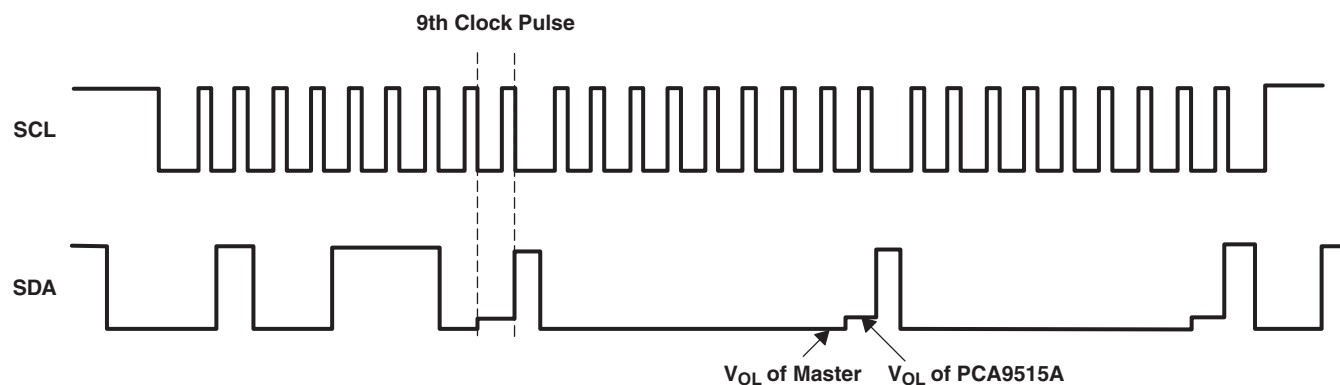


Figure 3. Bus 0 Waveforms

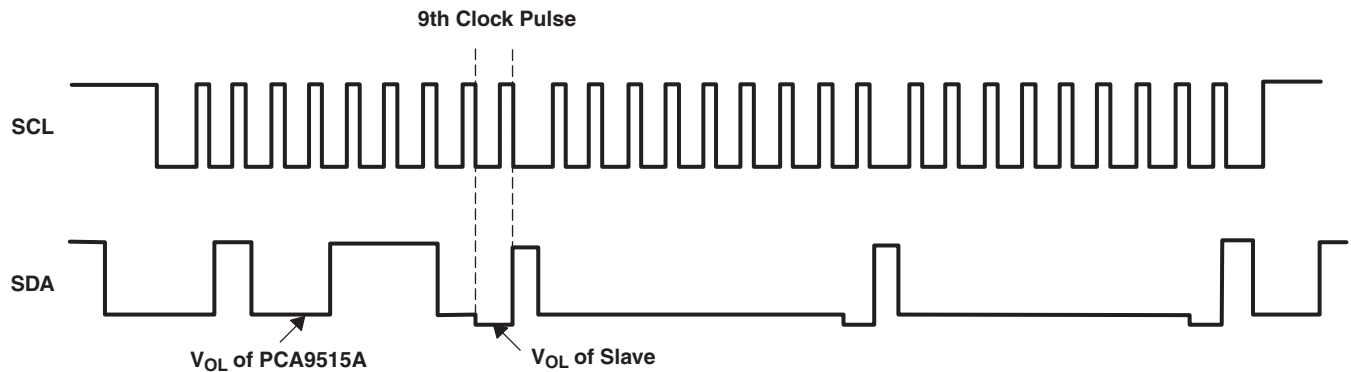


Figure 4. Bus 1 Waveforms

On the Bus 1 side of the PCA9515A, the clock and data lines have a positive offset from ground equal to the  $V_{OL}$  of the PCA9515A. After the eighth clock pulse, the data line is pulled to the  $V_{OL}$  of the slave device, which is very close to ground in the example.

It is important to note that any arbitration or clock-stretching events on Bus 1 require that the  $V_{OL}$  of the devices on Bus 1 be 70 mV below the  $V_{OL}$  of the PCA9515A (see  $V_{OL} - V_{ILC}$  in *Electrical Characteristics*) to be recognized by the PCA9515A and transmitted to Bus 0.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PCA9515AD	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515ADG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515ADGKR	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7BA ~ 7BE)	
PCA9515ADGKRG4	NRND	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7BA ~ 7BE)	
PCA9515ADGKT	NRND	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7BA ~ 7BE)	
PCA9515ADGKTG4	NRND	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7BA ~ 7BE)	
PCA9515ADR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515ADRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515ADRGR	NRND	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVD	
PCA9515ADT	NRND	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515ADTG4	NRND	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515AP	NRND	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PCA9515AP	
PCA9515APW	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515APWG4	NRND	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515APWR	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515APWRG4	NRND	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	
PCA9515APWT	NRND	TSSOP	PW	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PCA9515APWTG4	NRND	TSSOP	PW	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD515A	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9515ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PCA9515ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9515ADGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PCA9515ADGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9515ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
PCA9515ADRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PCA9515ADT	SOIC	D	8	250	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
PCA9515APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9515ADGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
PCA9515ADGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
PCA9515ADGKT	VSSOP	DGK	8	250	220.0	205.0	50.0
PCA9515ADGKT	VSSOP	DGK	8	250	358.0	335.0	35.0
PCA9515ADR	SOIC	D	8	2500	367.0	367.0	35.0
PCA9515ADRGR	SON	DRG	8	3000	367.0	367.0	35.0
PCA9515ADT	SOIC	D	8	250	367.0	367.0	35.0
PCA9515APWR	TSSOP	PW	8	2000	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

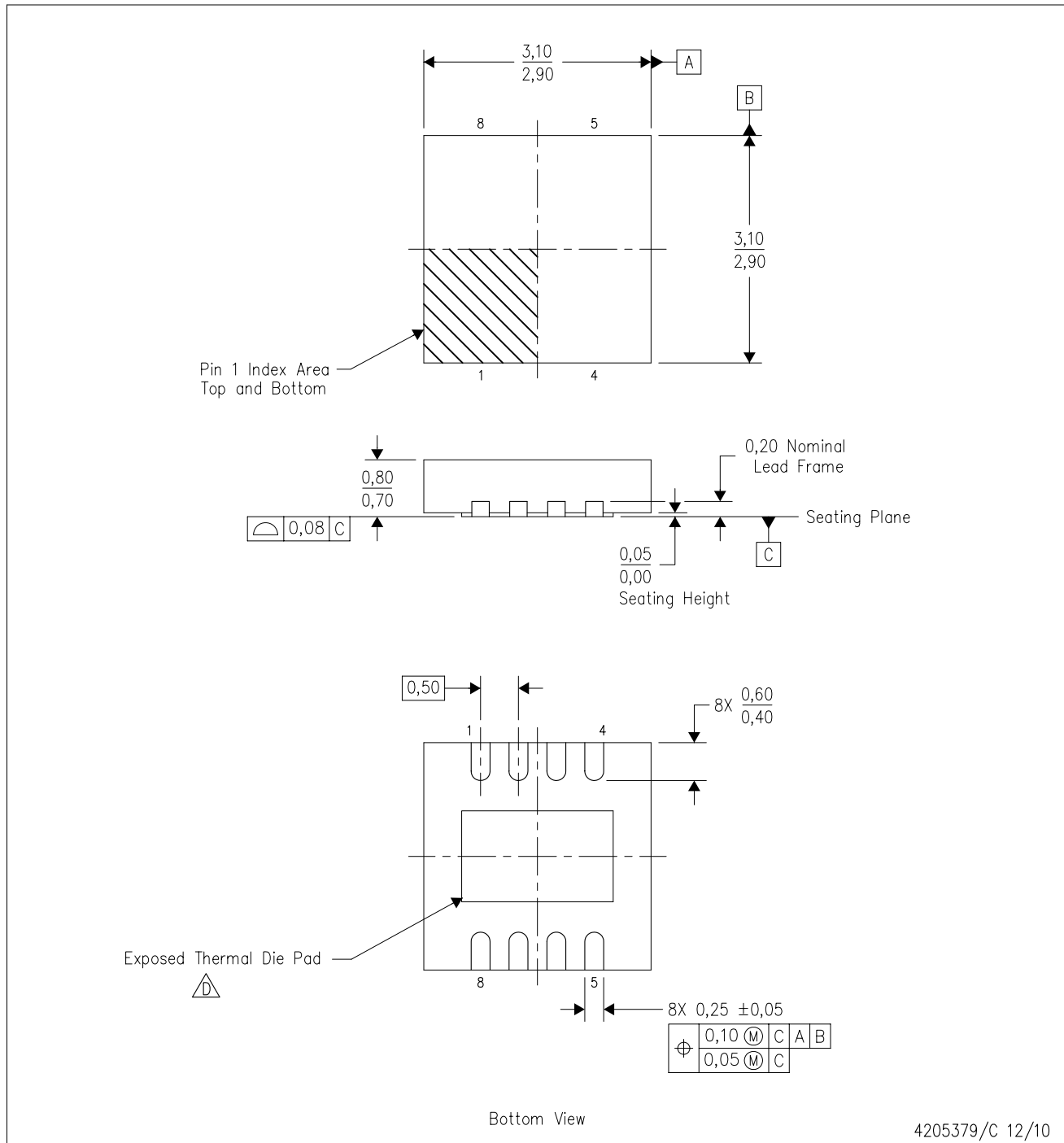
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. JEDEC MO-229 package registration pending.

# THERMAL PAD MECHANICAL DATA

DRG (S-PWSON-N8)

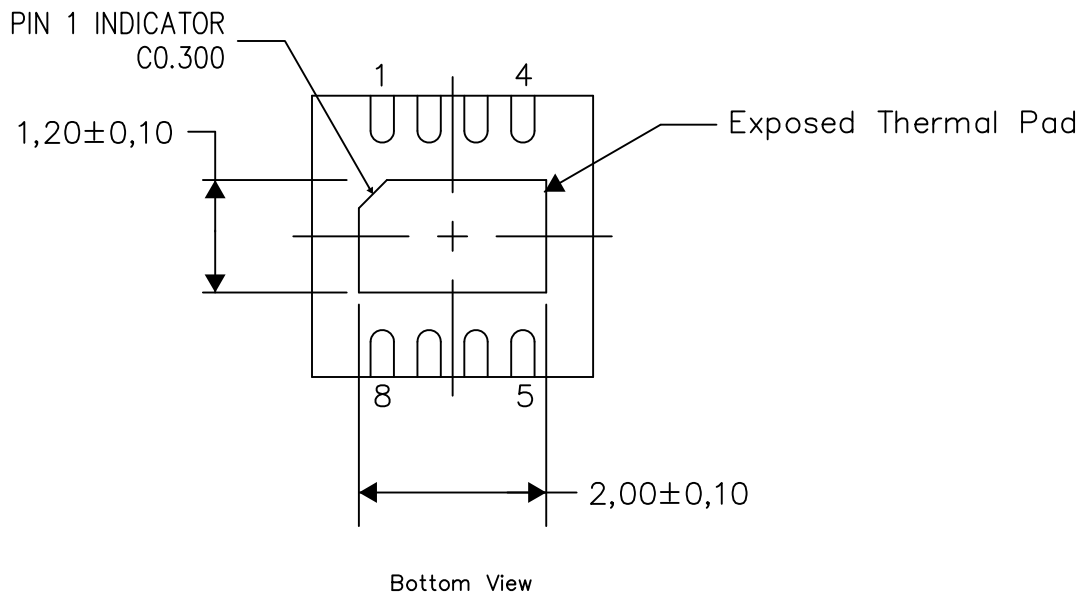
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

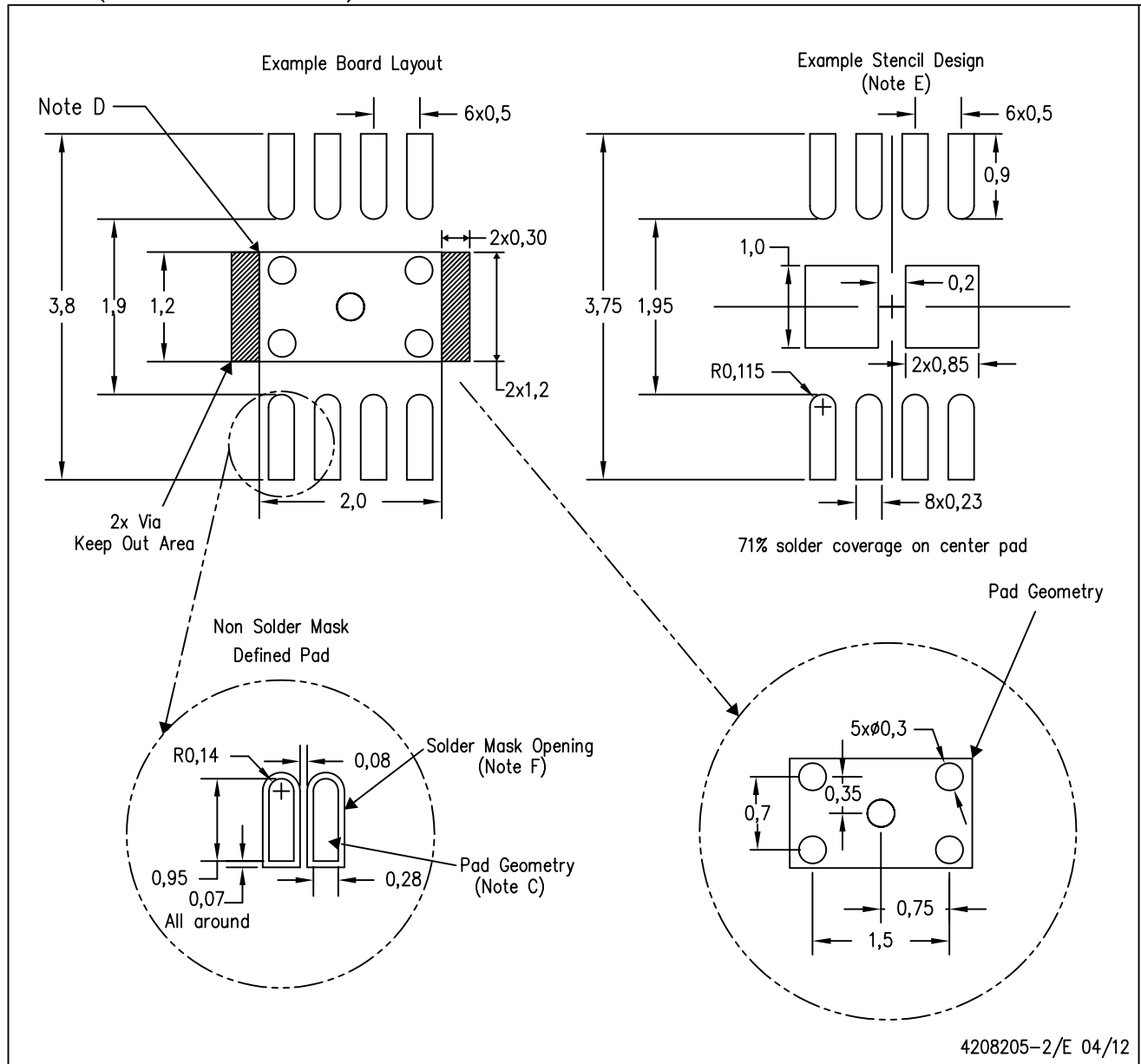
4206881-2/G 04/12

NOTE: All linear dimensions are in millimeters



DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

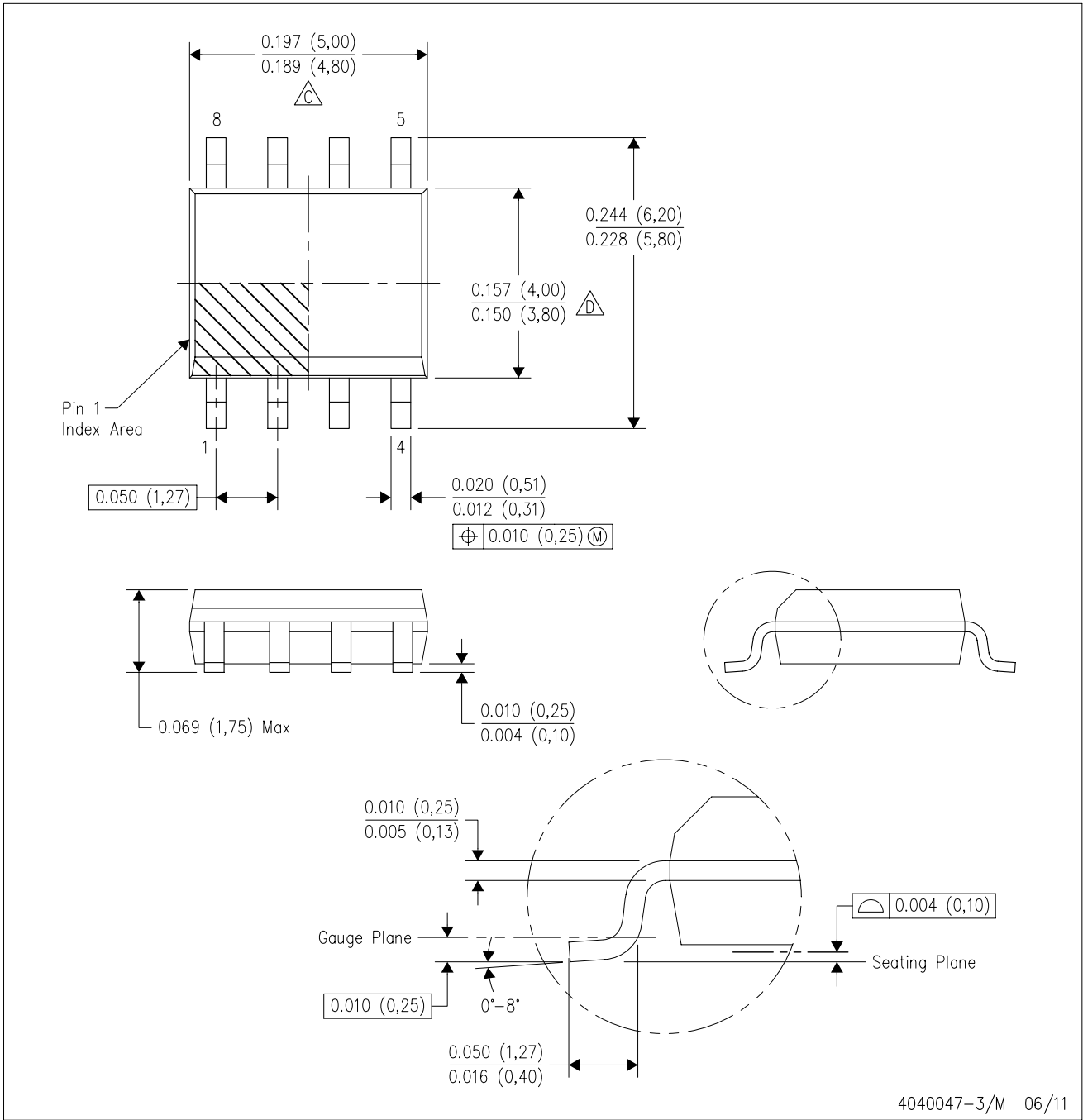


4208205-2/E 04/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-SM-782 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

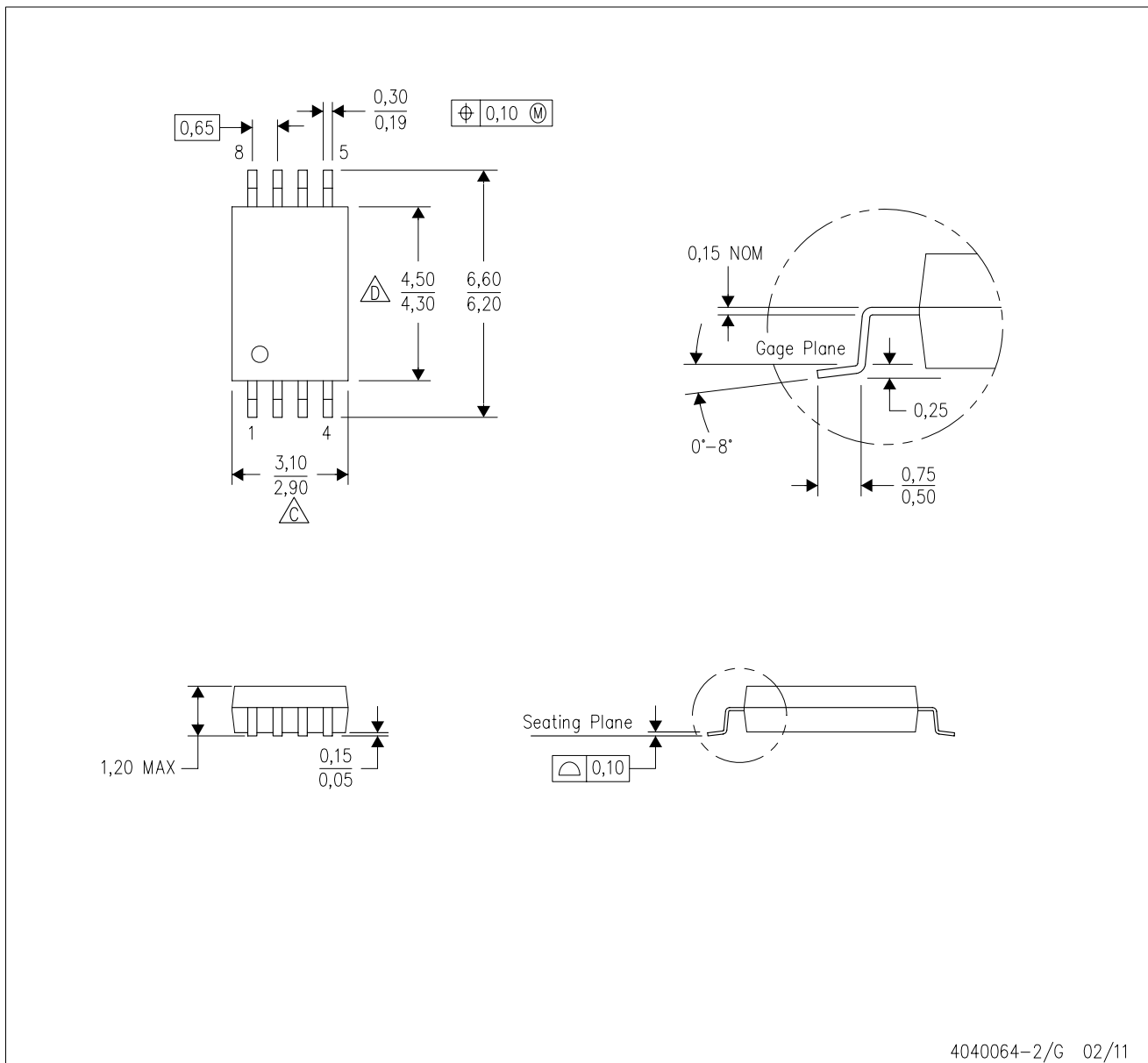
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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