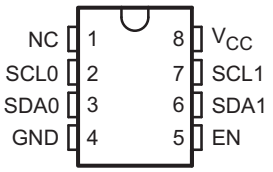
DUAL BIDIRECTIONAL I^2C BUS AND SMBus REPEATER

Check for Samples: PCA9515B

FEATURES

- **Two-Channel Bidirectional Buffers**
- **I^2C Bus and SMBus Compatible**
- **Active-High Repeater-Enable Input**
- **Open-Drain I^2C I/O**
- **5.5-V Tolerant I^2C I/O and Enable Input Support Mixed-Mode Signal Operation**
- **Lockup-Free Operation**
- **Accommodates Standard Mode, Fast Mode I^2C Devices, and Multiple Masters**
- **Supports Arbitration and Clock Stretching Across Repeater**
- **Powered-Off High-Impedance I^2C Pins**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class I**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGK PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION

The PCA9515B is a BiCMOS integrated circuit intended for I^2C bus and SMBus systems applications. The device contains two identical bidirectional open-drain buffer circuits that enables I^2C and similar bus systems to be extended without degrading system performance. The dual bidirectional I^2C buffer is operational at 2.3-V to 3.6-V V_{CC}.

The PCA9515B buffers both the serial data (SDA) and serial clock (SCL) signals on the I^2C bus, while retaining all the operating modes and features of the I^2C system. This feature allows two buses, of 400-pF bus capacitance, to be connected in an I^2C application.

The I^2C bus capacitance limit of 400 pF restricts the number of interfaced devices and bus length. Using the PCA9515B, a system designer can isolate two halves of a bus, thus accommodating more I^2C devices or longer trace lengths.

The PCA9515B has an active-high enable (EN) input with an internal pull-up. This allows users to select when the repeater is active and isolate malfunctioning slaves on power-up reset. States should never be changed during an I^2C operation. Disabling during a bus operation will hang the bus and enabling part way through a bus cycle may confuse the I^2C parts being enabled. The EN input should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

The PCA9515B can also be used to operate two buses, one at 5-V interface levels and the other at 3.3-V interface levels. The buses may also function at 400-kHz or 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated if the operation of the 400-kHz bus is required. If the master is running at 400-kHz, the maximum system operating frequency may be less than 400 kHz due to the delays added by the repeater.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	MSOP – DGK	Reel of 2500	PCA9515BDGKR	7SA

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) DGK: The actual top-side marking has one additional character that designates the assembly/test site.

The low level outputs for each internal buffer are approximately 0.5 V; however, the input voltage of each internal buffer must be 70 mV or more below the low level output when the output is driven low internally. This prevents a lockup condition from occurring when the input low condition is released.

Two or more PCA9515B devices cannot be used in series. Since there is no direction pin, different valid low-voltage levels are used to avoid lockup conditions between the input and the output of each repeater. A valid low, applied at the input of a PCA9515B, is propagated as a buffered low with a higher value on the enabled outputs. When this buffered low is applied to another PCA9515B-type device in series, the second device does not recognize it as a valid low and does not propagate it as a buffered low.

The device contains a power-up control circuit that sets an internal latch to prevent the output circuits from becoming active until V_{CC} is at a valid level (V_{CC} = 2.3 V).

As with the standard I^2C system, pullup resistors are required to provide the logic high levels on the buffered bus. The PCA9515B has standard open-collector configuration of the I^2C bus. The size of the pullup resistors depend on the system; however, each side of the repeater must have a pullup resistor. The device is designed to work with Standard Mode and Fast Mode I^2C devices in addition to SMBus devices. Standard Mode I^2C devices only specify a 3 mA termination current in a generic I^2C system where Standard Mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.

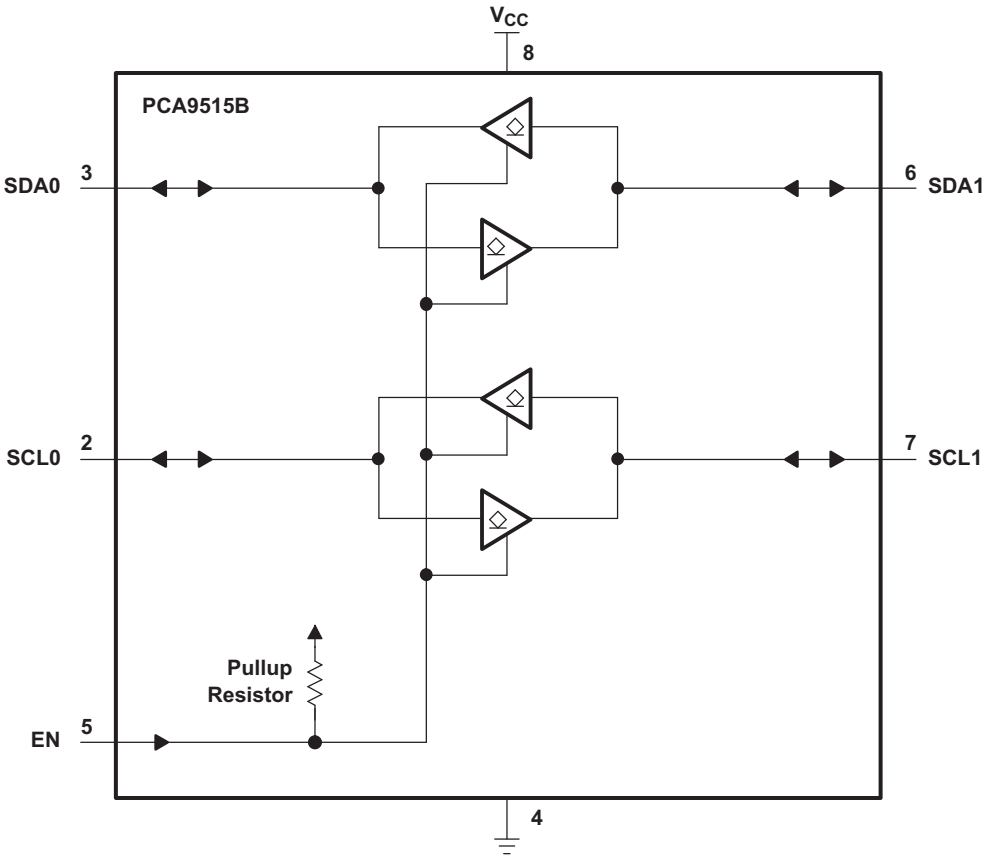
TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	NC	No internal connection
2	SCL0	Serial clock bus 0
3	SDA0	Serial data bus 0
4	GND	Supply ground
5	EN	Active-high repeater enable input
6	SDA1	Serial data bus 1
7	SCL1	Serial clock bus 1
8	V_{CC}	Supply power

Table 1. FUNCTION TABLE

INPUT EN	FUNCTION
L	Outputs disabled
H	SDA0 = SDA1, SCL0 = SCL1

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	DGK package		172	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	SDA and SCL inputs	0.7 × V_{CC}	5.5	V
		EN input	2	5.5	
V_{IL} (1)	Low-level input voltage	SDA and SCL inputs	–0.5	0.3 × V_{CC}	V
		EN input	–0.5	0.8	
V_{ILc} (1)	SDA and SCL low-level input voltage contention		–0.5	0.4	V
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 3 V		6	
T_A	Operating free-air temperature		–40	85	°C

(1) V_{IL} specification is for the EN input and the first low level seen by the SDAx and SCLx lines. V_{ILc} is for the second and subsequent low levels seen by the SDAx and SCLx lines. V_{ILc} must be at least 70 mV below V_{OL}.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = –18 mA		2.3 V to 3.6 V			–1.2	V
V_{OL}	Low-level output voltage	SDAx, SCLx	I_{OL} = 20 µA or 6 mA		2.3 V to 3.6 V	0.4	0.5	0.6	V
$V_{OL} – V_{ILc}$	Low-level input voltage below low-level output voltage	SDAx, SCLx	I_I = 10 µA		2.3 V to 3.6 V			70	mV
I_{CC}	Quiescent supply current		Both channels high, SDAx = SCLx = V_{CC}		2.7 V		0.5	3	mA
					3.6 V		0.5	3	
			Both channels low, SDA0 = SCL0 = GND and SDA1 = SCL1 = open; or SDA0 = SCL0 = open and SDA1 = SCL1 = GND		2.7 V		1	4	
					3.6 V		1	4	
			In contention, SDAx = SCLx = GND		2.7 V		1	4	
					3.6 V		1	4	
I_I	Input current	SDAx, SCLx	V_I = 3.6 V		2.3 V to 3.6 V			±1	µA
			V_I = 0.2 V					3	
		EN	V_I = V_{CC}					±1	
			V_I = 0.2 V				–10	–20	
I_{off}	Leakage current	SDAx, SCLx	V_I = 3.6 V	EN = L or H	0 V			0.5	µA
			V_I = GND					0.5	
$I_{I(ramp)}$	Leakage current during power up	SDAx, SCLx	V_I = 3.6 V	EN = L or H	0 V to 2.3 V			1	µA
C_{in}	Input capacitance	EN	V_I = 3 V or GND		3.3 V		7	9	pF
		SDAx, SCLx		EN = H	3.3 V		7	9	

(1) All typical values are at nominal supply voltage (V_{CC} = 2.5 V or 3.3 V) and T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_{su}	Setup time, EN↑ before Start condition	100		100		ns
t_h	Hold time, EN↓ after Stop condition	130		100		ns

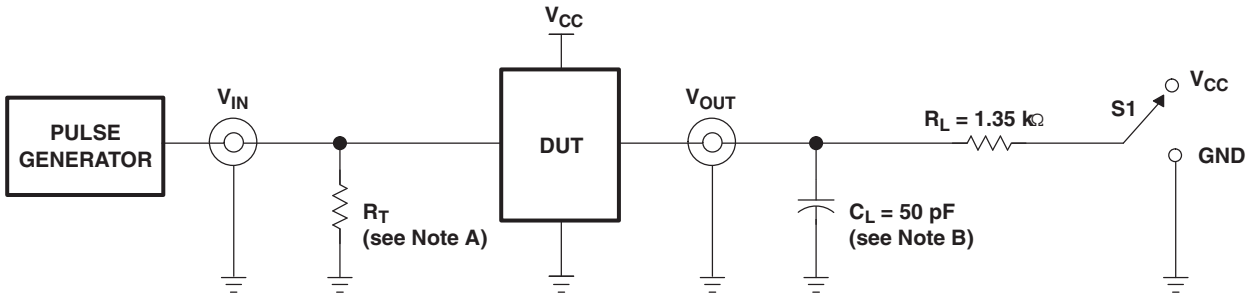
Switching Characteristics

over recommended operating free-air temperature range, C_L ≤ 100 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V			V_{CC} = 3.3 V ± 0.3 V			UNIT
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{PZL}	Propagation delay time(2)	SDA0, SCL0 or SDA1, SCL1	SDA1, SCL1 or SDA0, SCL0	45	82	130	45	68	120	ns
t_{PLZ}				33	113	190	33	102	180	
t_{tHL}	Output transition time(2) (SDAx, SCLx)	80%	20%		57			58		ns
t_{tLH}		20%	80%		148			147		

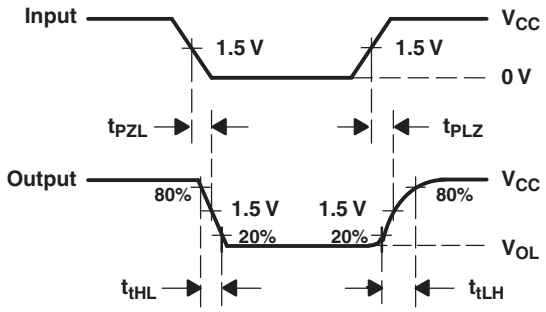
(1) All typical values are at nominal supply voltage (V_{CC} = 2.5 V or 3.3 V) and T_A = 25°C.
(2) Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

B. C_L includes probe and jig capacitance.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

G. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

A typical application is shown in Figure 2. In this example, the system master is running on a 3.3-V bus, while the slave is connected to a 5-V bus. Both buses run at 100 kHz, unless the slave bus is isolated. If the slave bus is isolated, the master bus can run at 400 kHz. Master devices can be placed on either bus.

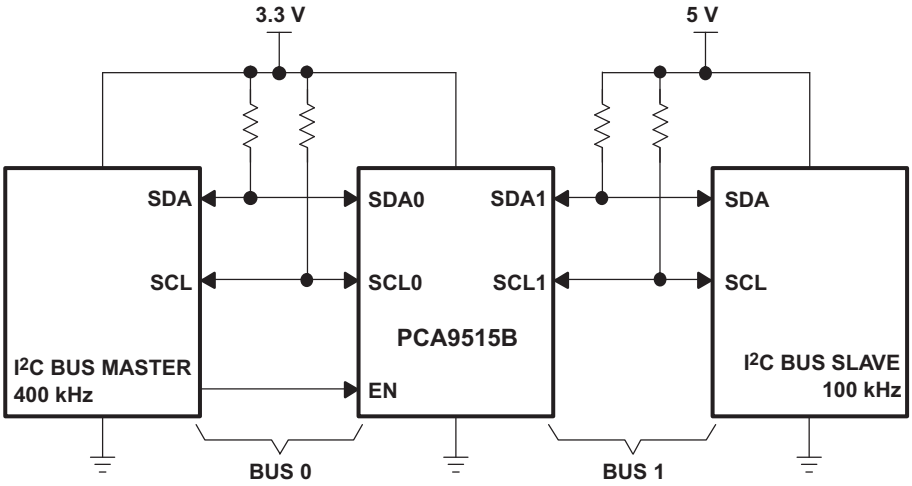


Figure 2. Typical Application

The PCA9515B is 5.5-V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9515B is pulled low by a device on the I^2C bus, a CMOS hysteresis-type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side also to go low. The side driven low by the PCA9515B has a typical value of V_{OL} = 0.5 V.

Figure 3 and Figure 4 show the waveforms that are seen in a typical application. If the bus master in Figure 2 writes to the slave through the PCA9515B, Bus 0 has the waveform shown in Figure 3. The waveform looks like a normal I^2C transmission until the falling edge of the eighth clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it low through the PCA9515B. Because the V_{OL} of the PCA9515B typically is around 0.5 V, a step in the SDA is seen. After the master has transmitted the ninth clock pulse, the slave releases the data line.

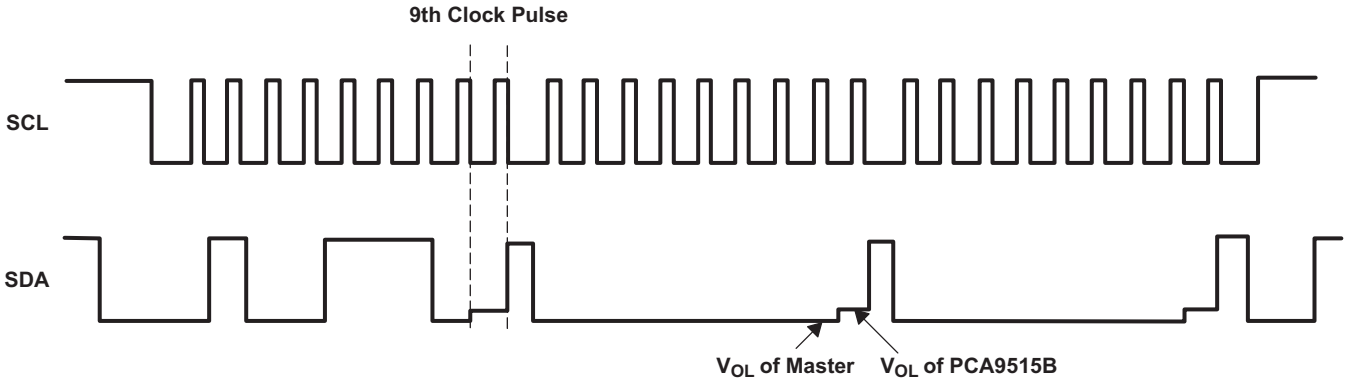


Figure 3. Bus 0 Waveforms

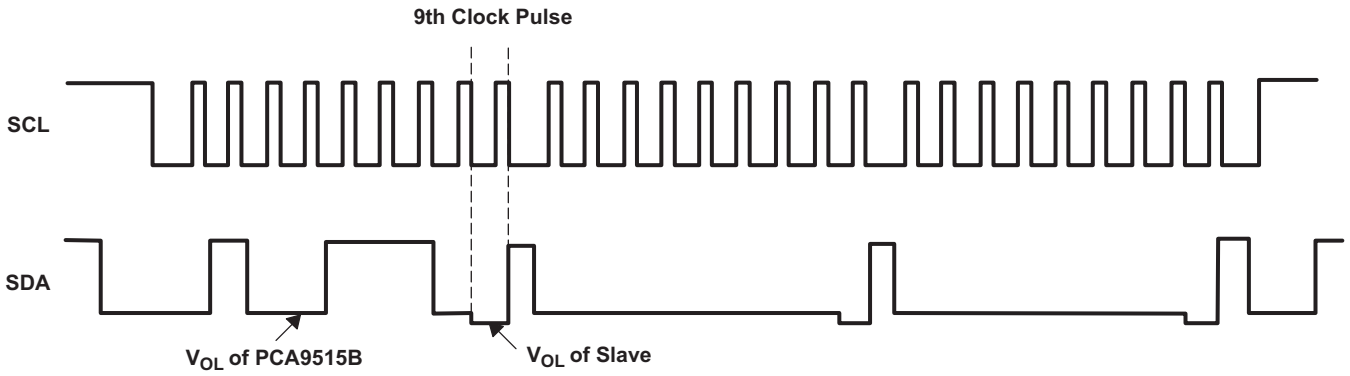


Figure 4. Bus 1 Waveforms

On the Bus 1 side of the PCA9515B, the clock and data lines have a positive offset from ground equal to the V_{OL} of the PCA9515B. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in the example.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PCA9515BDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7SE ~ 7SF)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

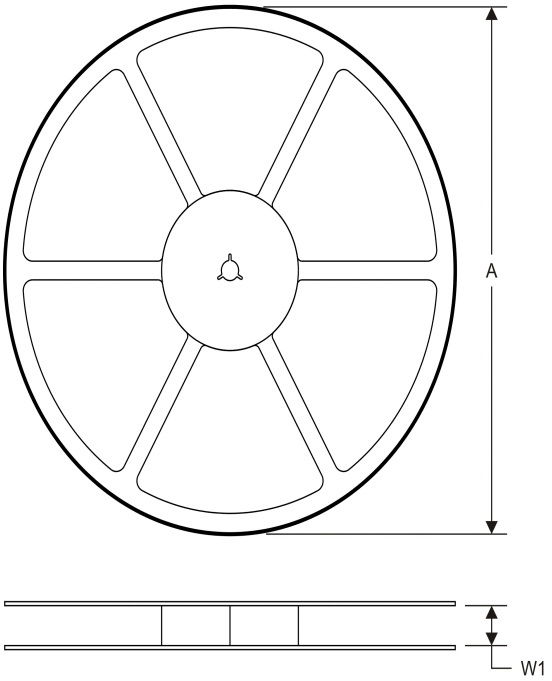
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

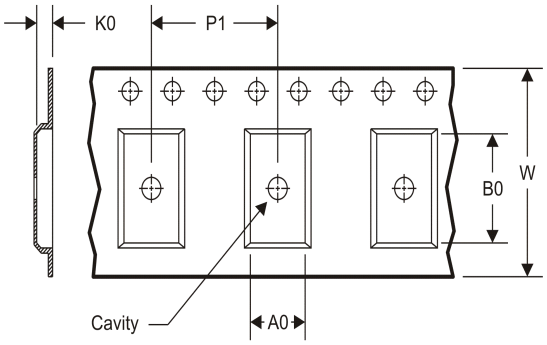
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



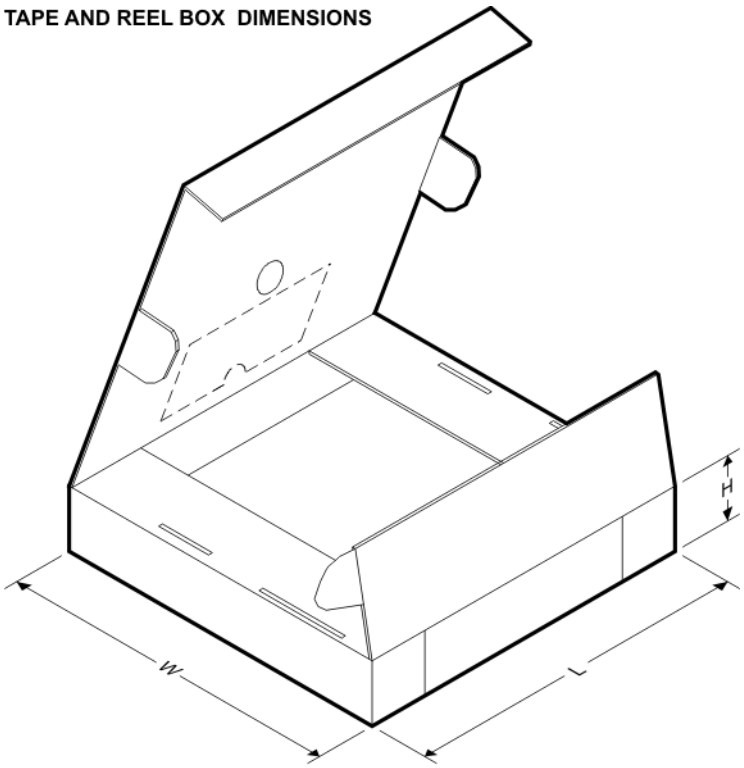
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9515BDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

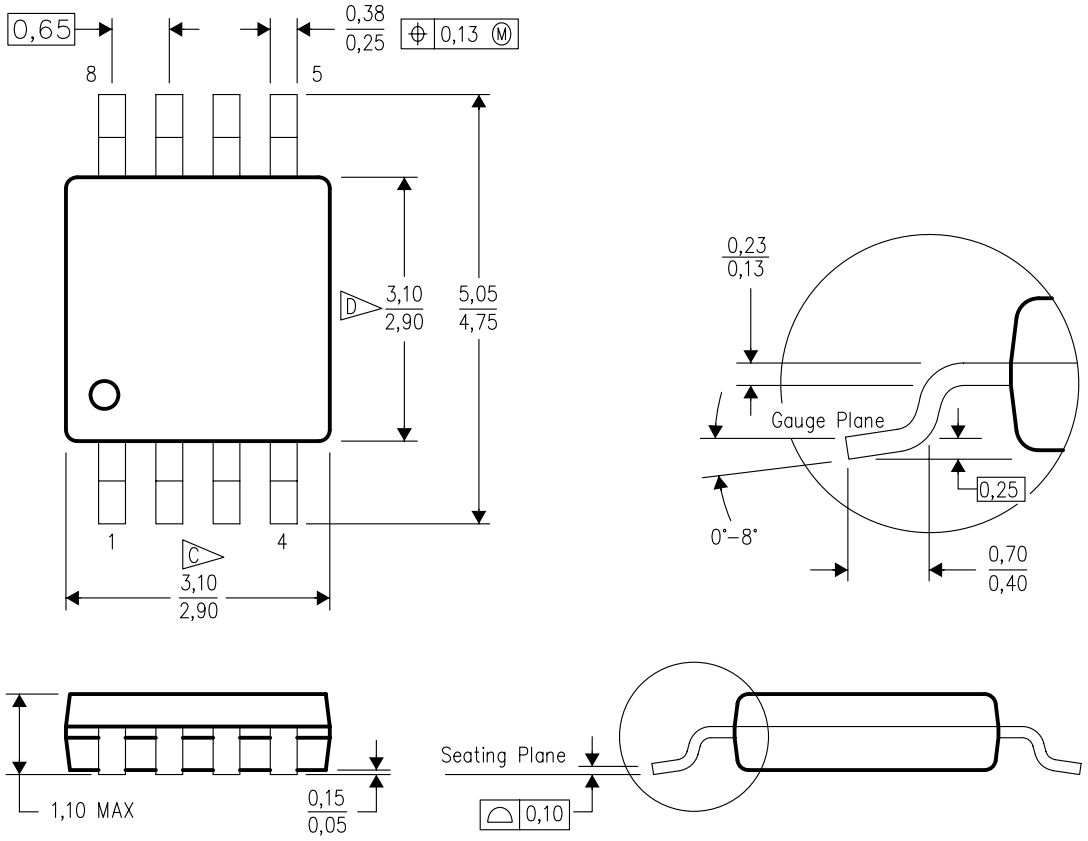
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9515BDGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265