LCD DUPLEX DRIVER PCF2100

GENERAL DESCRIPTION

The PCF2100 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 40 segments in a duplex manner; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 40 LCD-segment drive capability
- Supply voltage 2.25 to 6.5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility

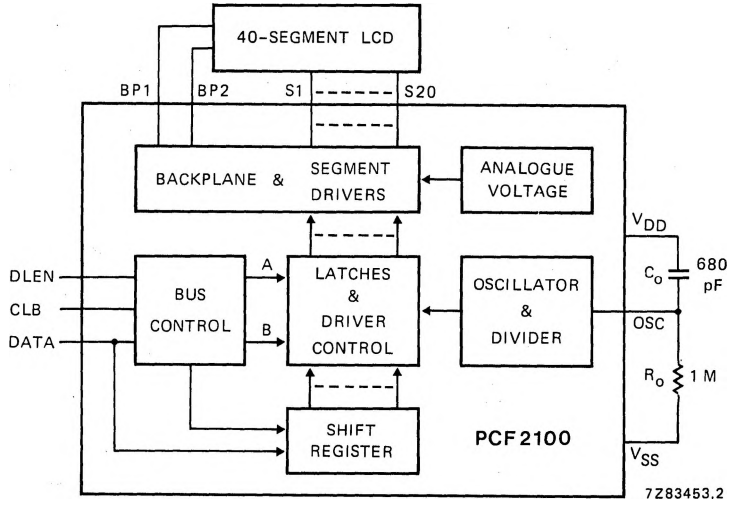


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}	−0.3 to 8 V
Voltage on any pin	V_n	V_{SS} −0.3 to V_{DD} + 0.3 V
Operating ambient temperature range	T_{amb}	−40 to + 85 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,25 to 6.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 680 pF; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to + 85 °C	I_{DD}	–	–	30	μA
Display frequency	see Fig. 8; T = 680 μs	f_{LCD}	60	80	100	Hz
D.C. component of LCD drive	with respect to V_{SX}	V_{BP}	–	± 10	–	mV
Load on each segment driver			–	–	10	MΩ
			–	–	500	pF
Load on each backplane driver			–	–	1	MΩ
			–	–	5	nF
Input voltage HIGH	see Fig. 9	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 9	V_{IL}	–	–	0,6	V
Rise time V_{BP} to V_{SX}	max. load	t_r	–	20	–	μs
Inputs CLB, DATA, DLEN	see note on next page					
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to $V_{IH\,min}$ and $V_{IL\,max}$ (see Fig. 2). If external resistors are used in the bus lines (see Fig. 9), the extra time constant has to be added.

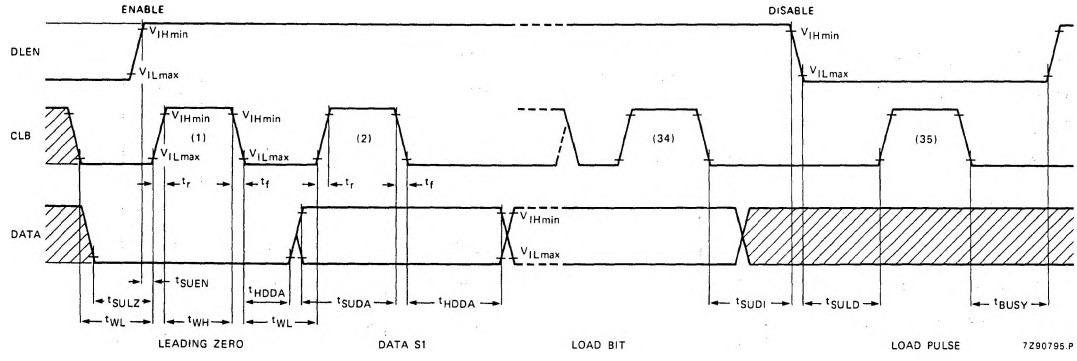


Fig. 2 CBUS timing.

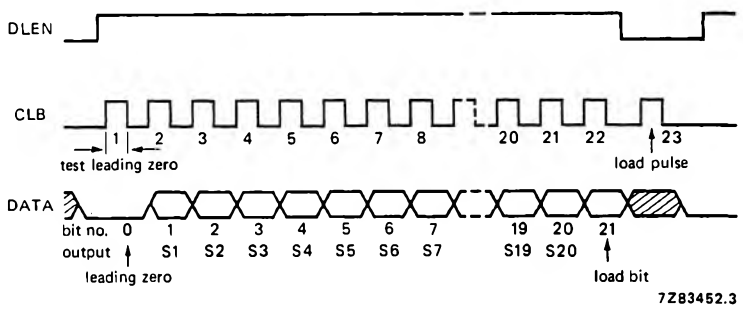


Fig. 3 CBUS data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded.
CLB-pulse 23 transfers data from shift register to selected latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load conditions (load pulse width DLEN is LOW) and the driver is ready to receive new data.

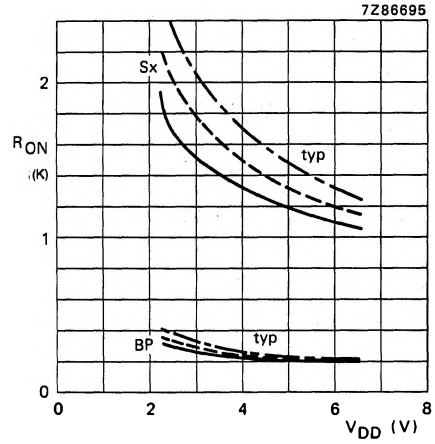


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

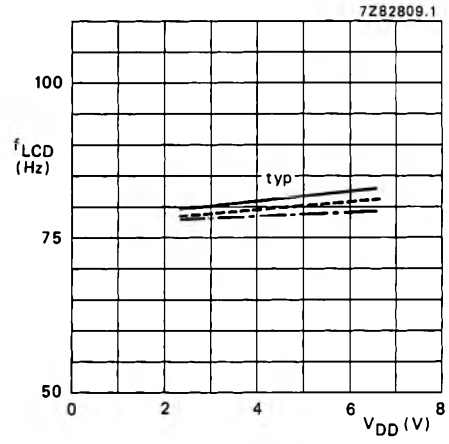


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 680 μs.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

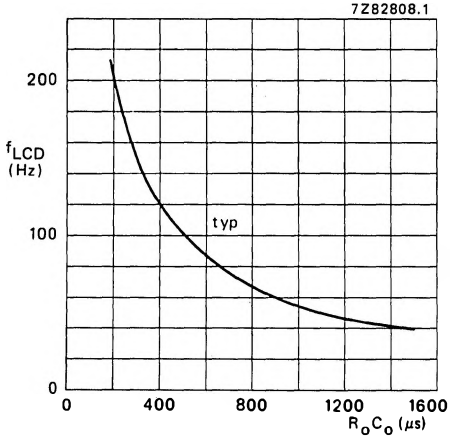


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

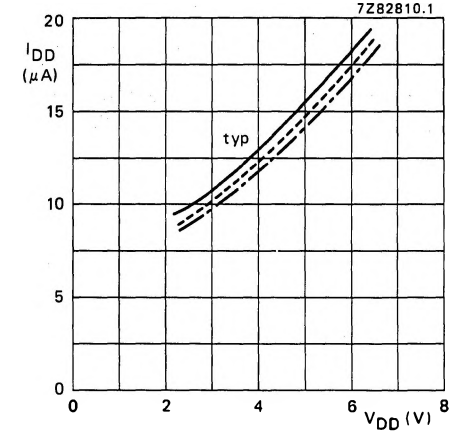


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C; – – – T_{amb} = + 25 °C; – · – · T_{amb} = +85 °C.

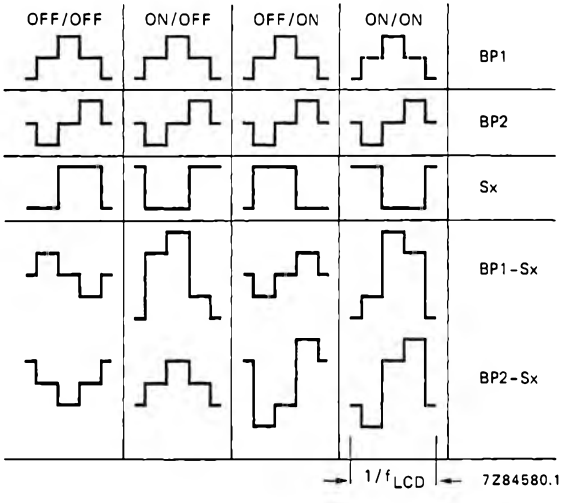


Fig. 8 Timing diagram.

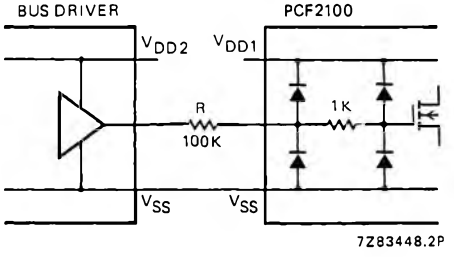
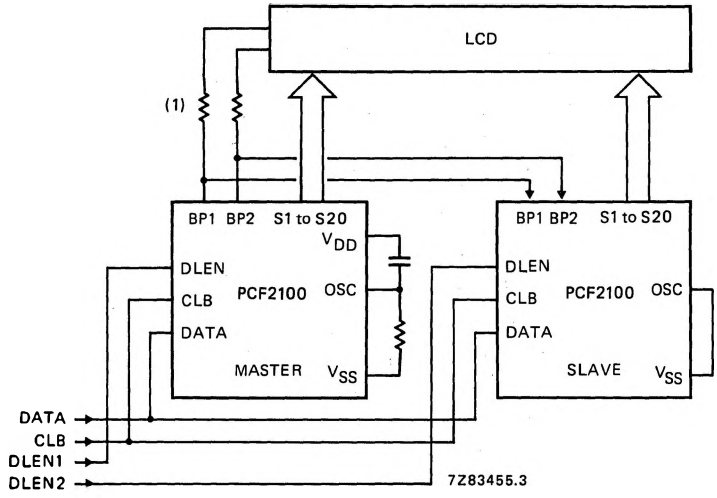


Fig. 9 Input circuitry.

Note to Fig. 9

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant 40\ \mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2100 and the backplane of the LCD must be > 2.7 kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 10 Diagram showing expansion possibility.

Note to Fig. 10

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2111, PCF2110 and PCF2100 ICs up to the BP drive capability of the master.

PCF2111 is a 64 LCD-segment driver.
PCF2110 is a 60 LCD-segment driver plus 2 LED driver outputs.

LCD DUPLEX DRIVER PCF2100

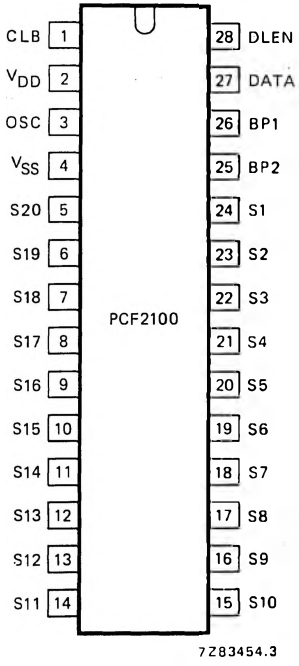


Fig. 11 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
27	DATA	Data line	CBUS
28	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

26	BP1	Backplane drivers (common of LCD)
25	BP2	Backplane drivers (common of LCD)
S1 to S20		LCD driver outputs