LCD DRIVER PCF2112

GENERAL DESCRIPTION

The PCF2112 is a single chip, silicon gate CMOS circuit designed to drive an LCD (Liquid Crystal Display) with up to 32 segments in direct drive; specially for low voltage applications. A three-line bus structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- 32 LCD-segment drive capability.
- Supply voltage 2.25 to 6.5 V.
- Low current consumption.
- Serial data input.
- CBUS control.
- One-point built-in oscillator.
- Expansion possibility.

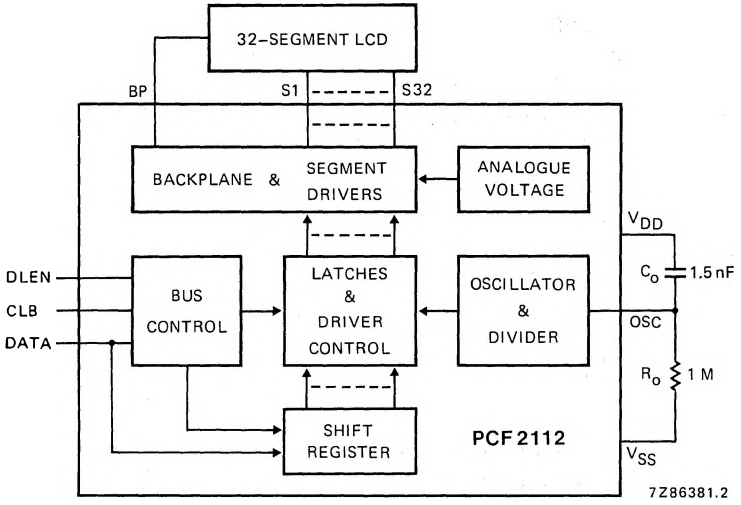


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF2112P: 40-lead DIL; plastic (SOT-129).
PCF2112T: 40-lead mini-pack; plastic (VSO-40; SOT-158A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{DD}	−0.3 to 8 V
Voltage on any pin	V_n	V_{SS}−0.3 to V_{DD} + 0.3 V
Operating ambient temperature range	T_{amb}	−40 to + 85 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2.25 to 6.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; R_o = 1 MΩ; C_o = 1.5 nF; unless otherwise specified.

parameter	condition	symbol	min.	typ.	max.	unit
Supply current	no external load	I_{DD}	–	10	50	μA
Supply current	no external load; T_{amb} = −25 to +85 °C	I_{DD}	–	–	30	μA
Display frequency	T = 1.5 ms	f_{LCD}	30	40	50	Hz
Output resistance of each segment	I_o = 10 μA	R_s	–	–	10	kΩ
Output resistance of backplane	I_o = 10 μA	R_{BP}	–	–	2	kΩ
Input voltage HIGH	see Fig. 8	V_{IH}	2	–	–	V
Input voltage LOW	see Fig. 8	V_{IL}	–	–	0.6	V
Inputs CLB,DATA,DLEN	see note on next page					
Input capacitance	for SOT-129 package	C_{IN}	–	–	10	pF
	for SOT-158A package	C_{IN}	–	–	5	pF
Rise and fall times	see Fig. 2	t_r, t_f	–	–	10	μs
CLB pulse width HIGH	see Fig. 2	t_{WH}	1	–	–	μs
CLB pulse width LOW	see Fig. 2	t_{WL}	9	–	–	μs

CHARACTERISTICS (continued)

parameter	condition	symbol	min.	typ.	max.	unit
Data set-up time DATA → CLB	see Fig. 2	t_{SUDA}	8	–	–	μs
Data hold time DATA → CLB	see Fig. 2	t_{HDDA}	8	–	–	μs
Enable set-up time DLEN → CLB	see Fig. 2	t_{SUEN}	1	–	–	μs
Disable set-up time CLB → DLEN	see Fig. 2	t_{SUDI}	8	–	–	μs
Set-up time (load pulse) DLEN → CLB	see Fig. 2	t_{SULD}	8	–	–	μs
Busy-time from load pulse to next start of transmission	see Fig. 2	t_{BUSY}	8	–	–	μs
Set-up time (leading zero) DATA → CLB	see Fig. 2	t_{SULZ}	8	–	–	μs

Note

All timing values are referred to V_{IHmin} and V_{ILmax} (see Fig. 2). If external resistors are used in the bus lines (see Fig. 8), an extra time constant has to be added.

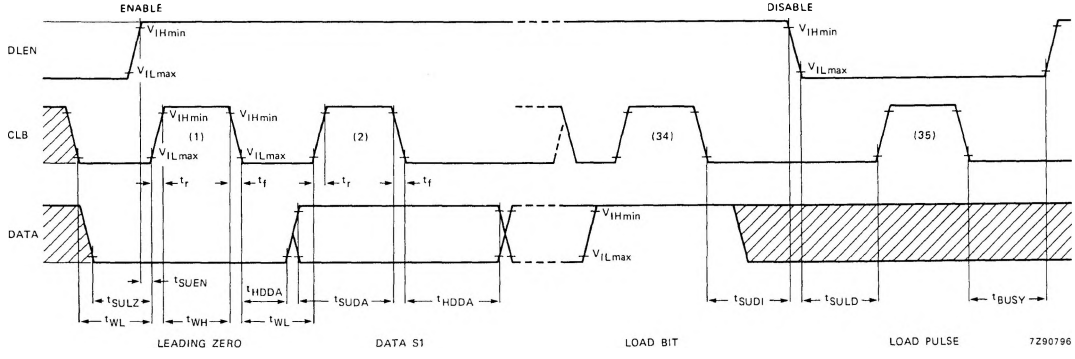


Fig. 2 CBUS timing.

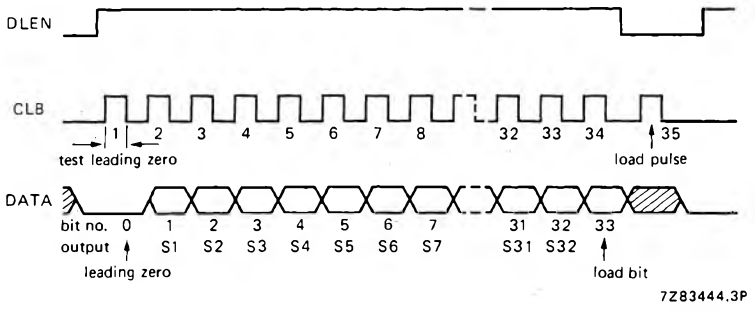


Fig. 3 Data format.

Notes to Fig. 3

An LCD segment is activated when the corresponding DATA-bit is HIGH.
When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from shift register to latches.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN is LOW) and the driver is ready to receive new data.

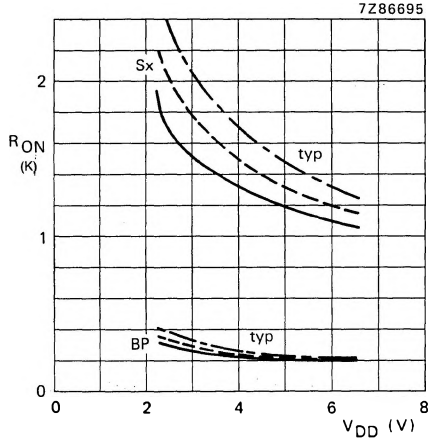


Fig. 4 Output resistance of backplane and segments.
——— T_{amb} = −40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

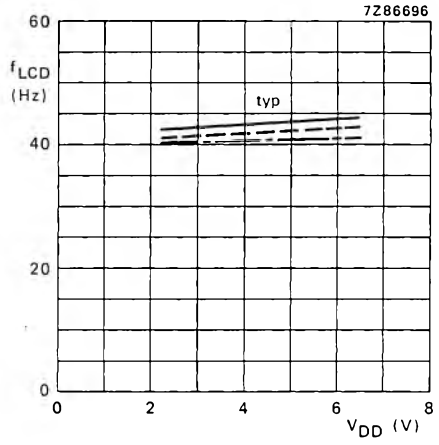


Fig. 5 Display frequency as a function of supply voltage; R_oC_o = 1.5 ms.
——— T_{amb} = −40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

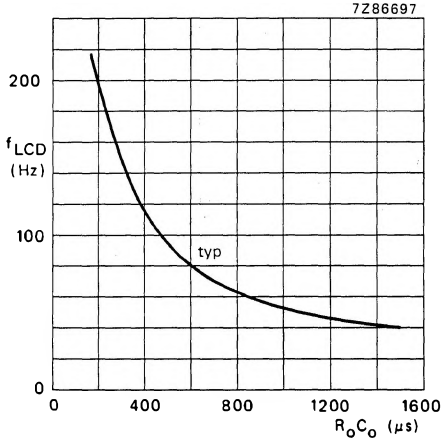


Fig. 6 Display frequency as a function of R_o x C_o time; T_{amb} = 25 °C.

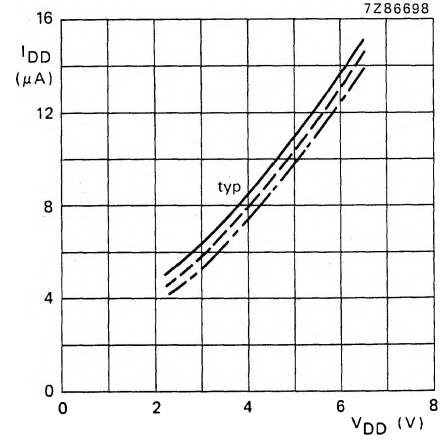


Fig. 7 Supply current as a function of supply voltage.
——— T_{amb} = −40 °C; – – – T_{amb} = + 25 °C; – · – T_{amb} = + 85 °C.

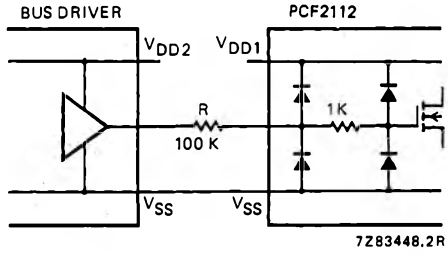
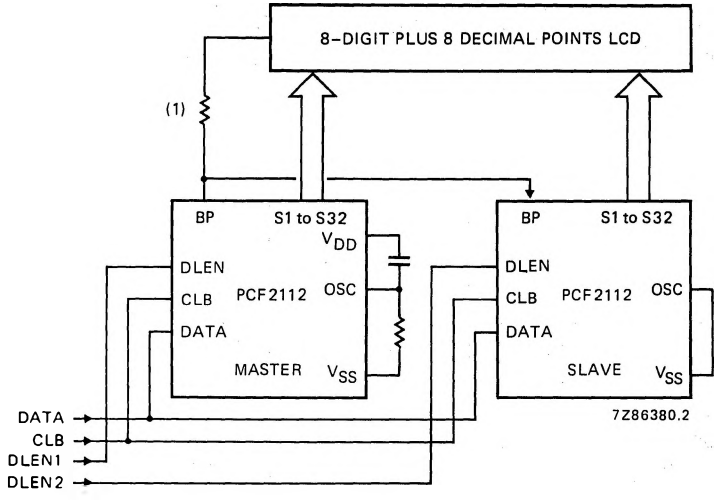


Fig. 8 Input circuitry.

Note to Fig. 8

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5$ V, a resistor should be inserted to reduce the current flowing through the input protection.
Maximum input current $\leqslant 40\ \mu A$.



(1) In the slave mode, the serial resistor between BP of the PCF2112 and the backplane of the LCD must be $> 2.7\ k\Omega$. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 9 Diagram showing expansion possibility for an 8-digit plus 8 decimal points LCD.

Note to Fig. 9

By connecting OSC to V_{SS} the BP-pin becomes input and generates signals synchronized to the single oscillator frequency, thus allowing expansion of several PCF2112 ICs up to the BP drive capability of the master.

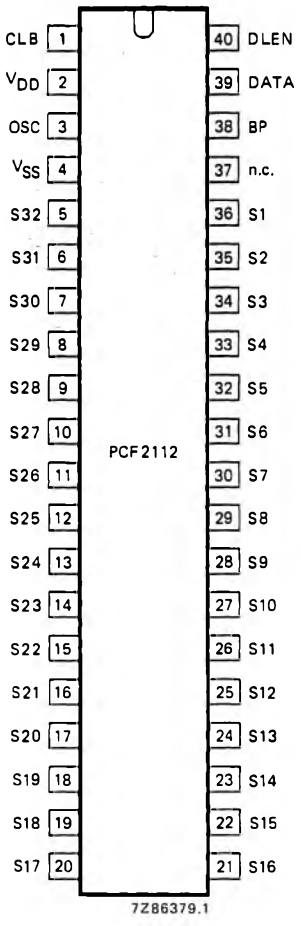


Fig. 10 Pinning diagram.

PINNING

Supply

2	V_{DD}	Positive supply
4	V_{SS}	Negative supply

Inputs

3	OSC	Oscillator input	
39	DATA	Data line	CBUS
40	DLEN	Data line enable	CBUS
1	CLB	Clock burst	CBUS

Outputs

38	BP	Back plane driver (common of LCD)
S1 to S32		LCD driver outputs
37	n.c.	not connected