DATA SHEET

PCF2116 family
LCD controller/drivers

Product specification
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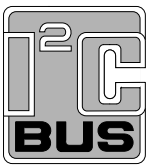
Philips
Semiconductors

PHILIPS

CONTENTS



1 FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5×7 character format plus cursor; 5×8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I^2C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption
- I^2C-bus address: 011101 SA0.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of the PCF2116x, the PCF2114x and the PCF2116K. The term ‘PCF2116’ is used to refer to all devices for common information. Specific information is given in separate paragraphs.

The ‘x’ in ‘PCF2116x’ and ‘PCF2114x’ represents a specific letter code for a character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, and G (see Figs 8 to 10). Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5×8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I^2C-bus. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}.

The PCF2116K differs from the other members of the family in that:

- V_{LCD}/V_{OP} generation is different (see Section 8.1)
- It is available with character set C only (see Fig.9).

4 ORDERING INFORMATION

TYPE NUMBER(1)	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2116xU/10	–	chip on flexible film carrier	–
PCF2114xU/10	–	chip on flexible film carrier	–
PCF2116xU/12	–	chip with bumps on flexible film carrier	–
PCF2114xU/12	–	chip with bumps on flexible film carrier	–
PCF2116xHZ	LQFP128	plastic low profile quad flat package; 128 leads; body $14 \times 20 \times 1.4$ mm	SOT425-1

Note

1. The letter ‘x’ in the type number represents the letter of the required built-in character set: A, C or G.

5 BLOCK DIAGRAM

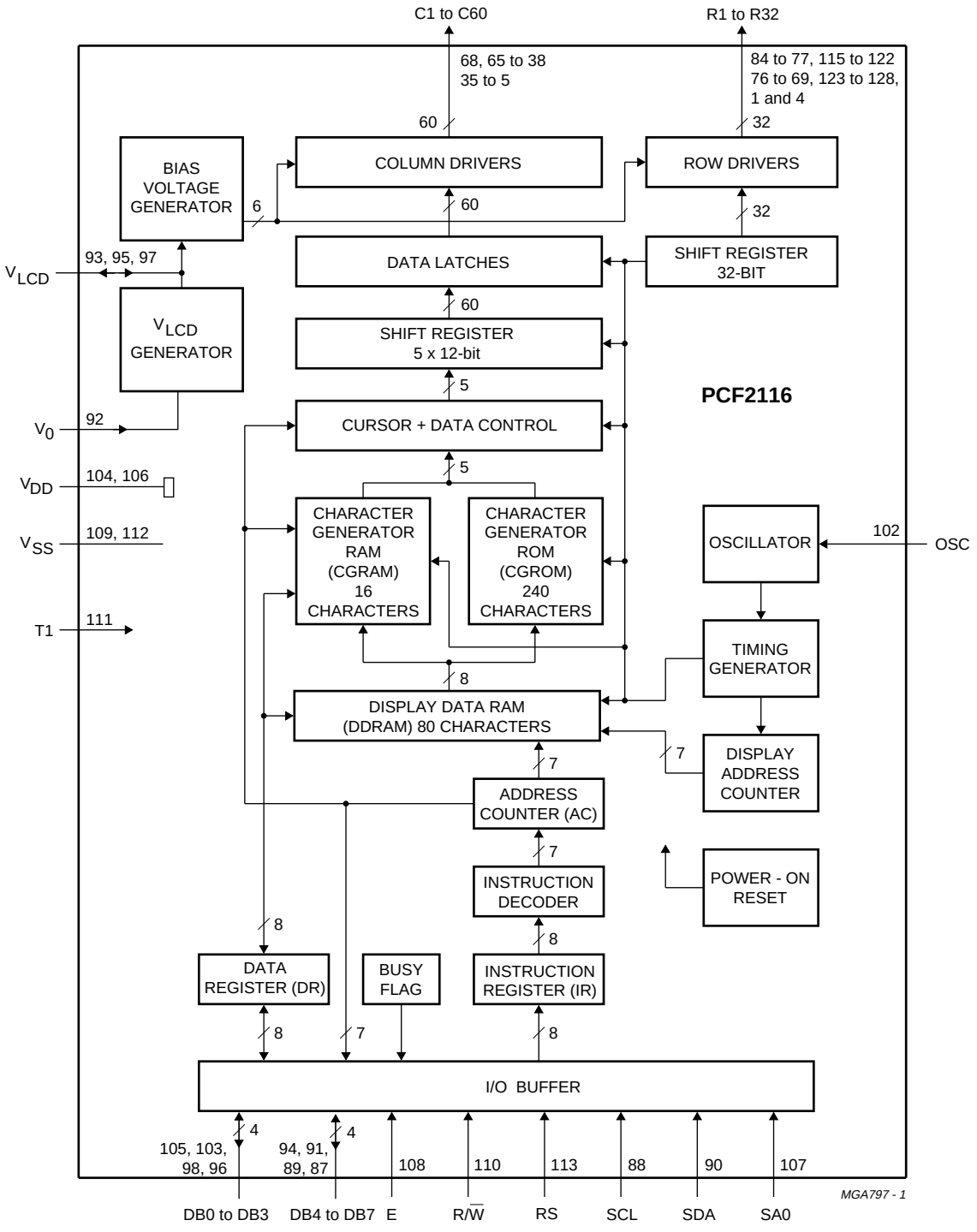


Fig.1 Block diagram (pin numbers for LQFP128 package).

6 PINNING

SYMBOL	LQFP128	FFC PAD	TYPE	DESCRIPTION
R31	1	27	O	LCD row driver output
n.c.	2 and 3	–	–	not connected
R32	4	28	O	LCD row driver output
C60 to C30	5 to 35	29 to 59	O	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	–	not connected
C29 to C2	38 to 65	60 to 87	O	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	–	not connected
C1	68	88	O	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	O	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	O	LCD row driver outputs
n.c.	85 and 86	–	–	not connected
DB7	87	105	I/O	1 bit of 8-bit bidirectional data bus
SCL	88	106	I	I^2C-bus serial clock input
DB6	89	107	I/O	1 bit of 8-bit bidirectional data bus
SDA	90	108	I/O	I^2C-bus serial data input/output
DB5	91	109	I/O	1 bit of 8-bit bidirectional data bus
V_0	92	110	I	control input for V_{LCD}
V_{LCD1}	93	111	I/O	LCD supply voltage input/output 1
DB4	94	112	I/O	1 bit of 8-bit bidirectional data bus
V_{LCD2}	95	113	I/O	LCD supply voltage input/output 2
DB3	96	114	I/O	1 bit of 8-bit bidirectional data bus
V_{LCD3}	97	115	I/O	LCD supply voltage input/output 3
DB2	98	116	I/O	1 bit of 8-bit bidirectional data bus
n.c.	99 to 101	–	–	not connected
OSC	102	1	I	oscillator/external clock input
DB1	103	2	I/O	1 bit of 8-bit bidirectional data bus
V_{DD2}	104	3	P	supply voltage 2
DB0	105	4	I/O	1 bit of 8-bit bidirectional data bus
V_{DD1}	106	5	P	supply voltage 1
SA0	107	6	I	I^2C-bus address pin
E	108	7	I	data bus clock input (parallel control)
V_{SS1}	109	8	P	ground (logic) 1
R/$\overline{W}$	110	9	I	read/write input (parallel control)
T1	111	10	I	test pad (connect to V_{SS})
V_{SS2}	112	11	P	ground (logic) 2
RS	113	12	I	register select input (parallel control)
n.c.	114	–	–	not connected
R9 to R16	115 to 122	13 to 20	O	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	O	LCD row driver outputs

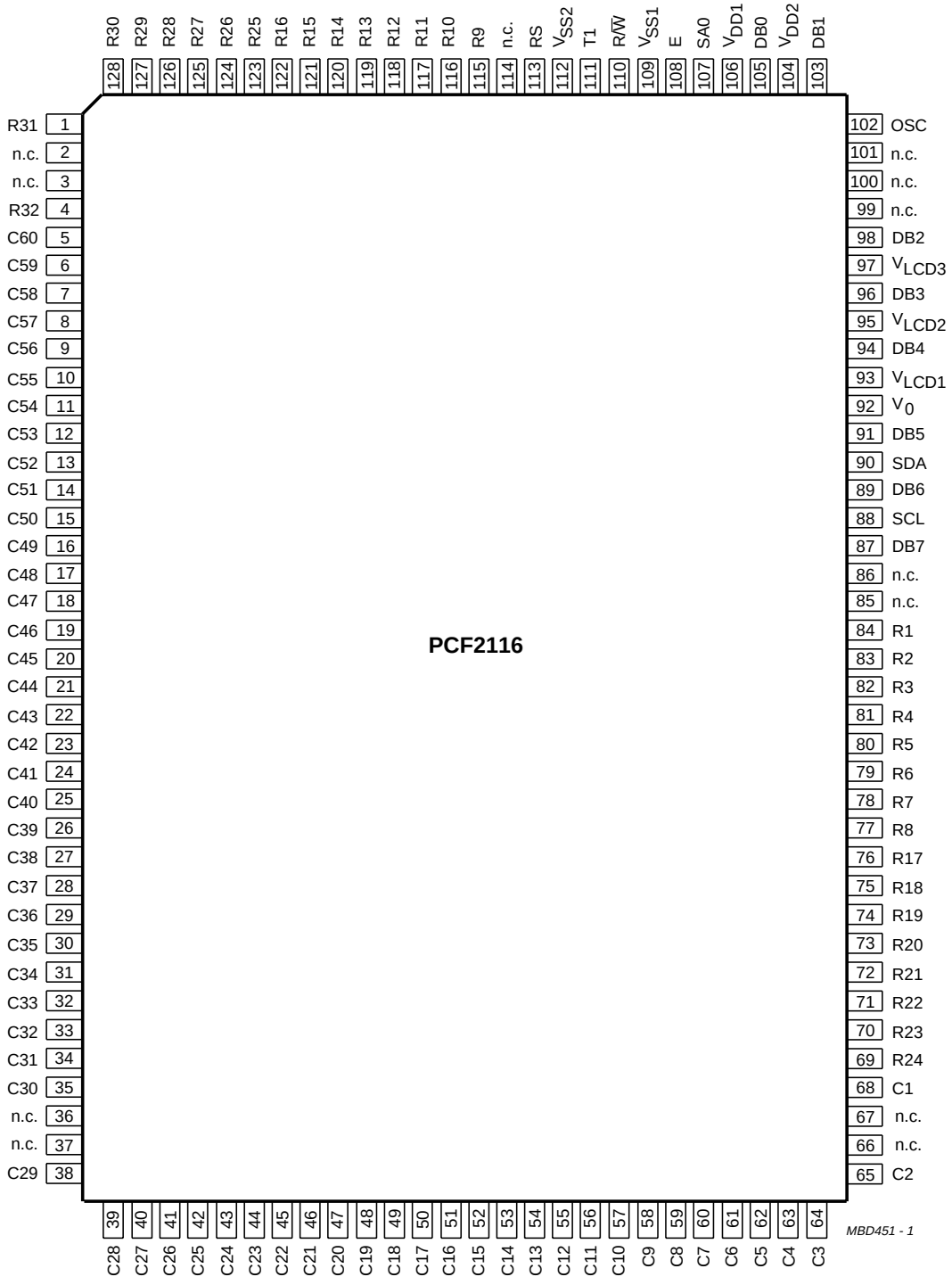


Fig.2 Pin configuration (LQFP128).

7 PIN FUNCTIONS

7.1 RS: register select (parallel control)

RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = logic 0 selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic 1 selects the data register for both read and write. There is an internal pull-up on pin RS.

7.2 R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic 1) or write (R/$\overline{W}$ = logic 0) operation when control is by the parallel interface. There is an internal pull-up on this pin.

7.3 E: data bus clock

The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be tied to logic 0 (V_{SS}) when I^2C-bus control is used.

7.4 DB0 to DB7: data bus

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2116. DB7 may be used as the Busy Flag, signalling that internal operations are not yet completed. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines. Note that these pins must be left open circuit when I^2C-bus control is used.

7.5 C1 to C60: column driver outputs

These pins output the data for pairs of columns. This arrangement permits optimized chip-on-glass (COG) layout for 4-line by 12 characters.

7.6 R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

7.7 V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display. This may be generated on-chip or supplied externally.

7.8 V_0: V_{LCD} control input

The input level at this pin determines the generated V_{LCD} output voltage.

7.9 OSC: oscillator

When the on-chip oscillator is used this pin must be connected to V_{DD}. An external clock signal, if used, is input at this pin.

7.10 SCL: serial clock line

Input for the I^2C-bus clock signal.

7.11 SDA: serial data line

Input/output for the I^2C-bus data line.

7.12 SA0: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2116s on the same I^2C-bus.

7.13 T1: test pad

Must be connected to V_{SS}. Not user accessible.

8 FUNCTIONAL DESCRIPTION (see Fig.1)

8.1 LCD supply voltage generator, PCF2114x and PCF2116x

The on-chip voltage generator is controlled by bit G of the 'Function set' instruction and V_0.

V_0 is a high-impedance input and draws no current from the system power supply. Its range is between V_{SS} and $V_{DD} - 1$ V. When V_0 is connected to V_{DD} the generator is switched off and an external voltage must be supplied to pin V_{LCD}. This may be more negative than V_{SS}.

When G = logic 1 the generator produces a negative voltage at pin V_{LCD}, controlled by the input voltage at pin V_0. The LCD operating voltage is given by the relationship:

$$V_{OP} = 1.8V_{DD} - V_0$$

Where:

$$V_{OP} = V_{DD} - V_{LCD}$$

$$V_{LCD} = V_0 - (0.8V_{DD})$$

When G = logic 0, the generated output voltage V_{LCD} is equal to V_0 (between V_{SS} and V_{DD}). In this instance:

$$V_{OP} = V_{DD} - V_0$$

When V_{LCD} is generated on-chip the V_{LCD} pin should be decoupled to V_{DD} with a suitable capacitor. V_{DD} and V_0 must be selected to limit the maximum value of V_{OP} to 9 V.

Figure 3 shows the two generator control characteristics.

8.2 LCD supply voltage generator, PCF2116K

In the PCF2116K version, V_0 is connected through an on-chip resistor (R_0) to V_{LCD}. Resistor R_0 has a nominal value of 1 MΩ and draws a typical current of 4 μA from the pin V_0. A constant voltage (equal to $1.34V_{DD}$) is always present across R_0.

The voltage range of the PCF2116K is between V_{SS} and V_{DD} – 0.5 V (see Fig.4). When V_0 is connected to V_{DD} the generator is switched off and an external voltage must be supplied to pin V_{LCD}. This may be more negative than V_{SS}.

When G = logic 1 the generator produces a negative voltage at pin V_{LCD}, controlled by the input voltage at pin V_0. The LCD operating voltage is given by the relationship:

$$V_{OP} = 2.34V_{DD} - V_0$$

Where:

$$V_{OP} = V_{DD} - V_{LCD}$$

$$V_{LCD} = V_0 - (1.34V_{DD})$$

When G = logic 0, the generated output voltage V_{LCD} is equal to V_0 (between V_{SS} and V_{DD}). In this instance:

$$V_{OP} = V_{DD} - V_0$$

8.3 Character generator ROM (CGROM)

The standard character sets A, C and G are available for the PCF2114x and PCF2116x. Standard character set C is available for the PCF2116K.

8.4 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system power consumption. The optimum levels depend on the multiplex rate and are selected automatically when the number of lines in the display is defined.

The optimum value of V_{OP} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships in Table 1.Using a 5-level bias scheme for 1 : 16 MUX rate allows $V_{OP} < 5$ V for most LCD liquids. The effect on the display contrast is negligible.

8.5 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required. Pin OSC must be connected to V_{DD}.

8.6 External clock

If an external clock is to be used, it must be input at pin OSC. The resulting display frame frequency is given by $f_{frame} = {}^{1}\!/_{2304} f_{osc}$. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

8.7 Power-on reset

The power-on reset block initializes the chip after power-on or power failure.

8.8 Registers

The PCF2116 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed.

The instruction register stores instruction codes such as ‘Display clear’ and ‘Cursor shift’, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to, but not read, by the system controller.

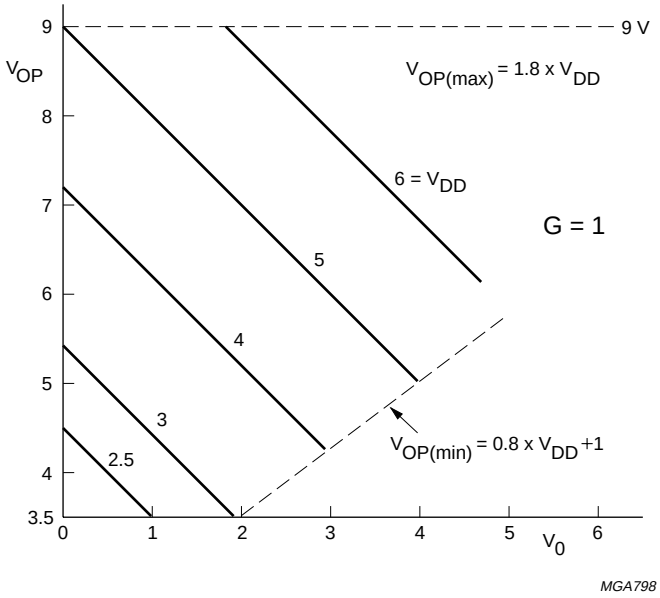
The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the Address Counter is written to the data register prior to being read by the ‘Read data’ instruction.

8.9 Busy Flag

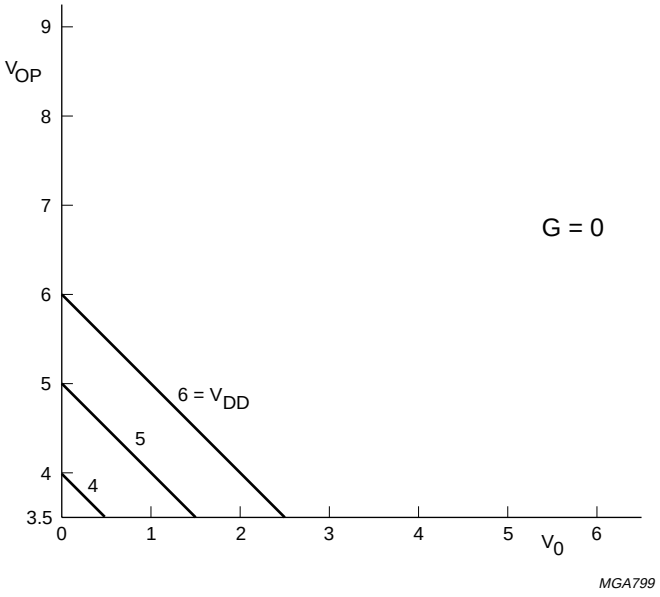
The Busy Flag indicates the free/busy status of the PCF2116. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The Busy Flag is output to pin DB7 when RS = logic 0 and R/$\overline{W}$ = logic 1. Instructions should only be written after checking that the Busy Flag is logic 0 or waiting for the required number of clock cycles.

Table 1 Optimum values for V_{OP}

MUX RATE	NUMBER OF BIAS LEVELS	V_{OP}/V_{th}	DISCRIMINATION V_{on}/V_{off}
1 : 16	5	3.67	1.277
1 : 32	6	5.19	1.196

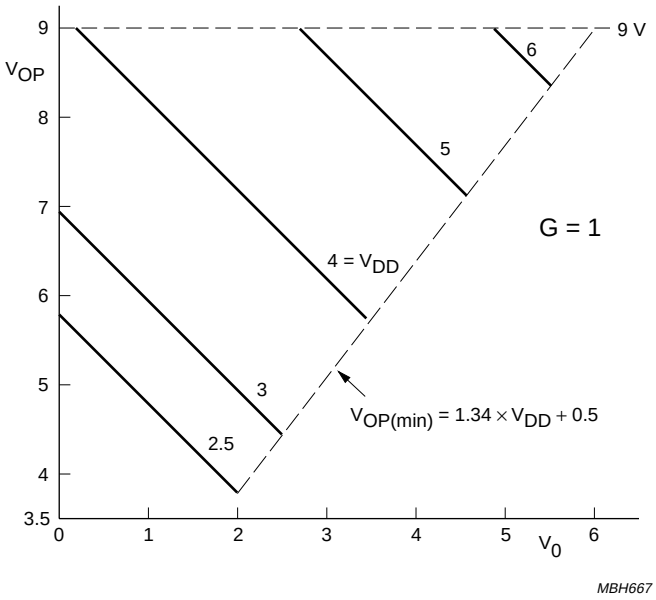


a. High-voltage mode $V_{OP} = 1.8V_{DD} - V_0$.

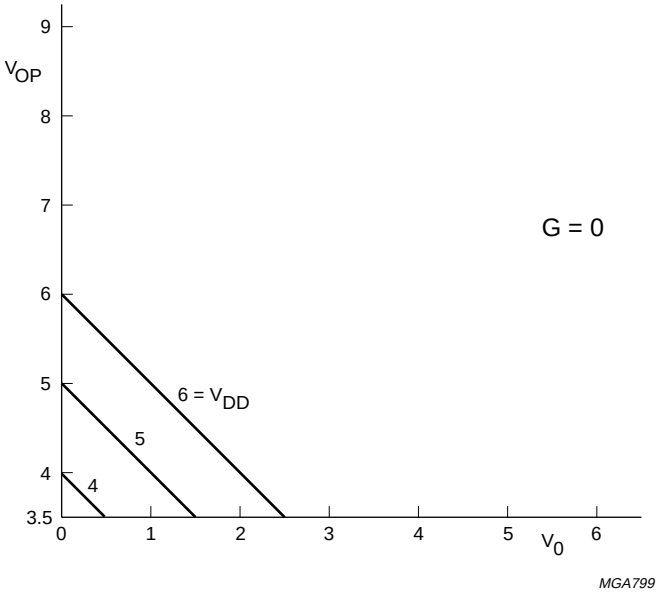


b. Buffer mode $V_{OP} = V_{DD} - V_0$.

Fig.3 V_{OP} as a function of V_0 control characteristics.



a. High-voltage mode $V_{OP} = 2.34V_{DD} - V_0$.



b. Buffer mode $V_{OP} = V_{DD} - V_0$.

Fig.4 V_{OP} as a function of V_0 control characteristics (PCF2116K).

8.10 Address Counter (AC)

The Address Counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the instructions 'Set CGRAM address' and 'Set DDRAM address'. After a read/write operation the Address Counter is automatically incremented or decremented by 1.The Address Counter contents are output to the bus (DB0 to DB6) when RS = logic 0 and R/$\overline{W}$ = logic 1.

8.11 Display data RAM (DDRAM)

The display data RAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations not used for storing display data can be used as general purpose RAM. The basic DDRAM-to-display mapping scheme is shown in Fig.5. With no display shift the characters represented by the codes in the first 12 or 24 RAM locations starting at address 00 in line 1 are displayed. Subsequent lines display data starting at addresses 20, 40, or 60 Hex. Figs 6 and 7 show the DDRAM-to-display mapping principle when the display is shifted.

The address range for a 1-line display is 00 to 4F; for a 2-line display from 00 to 27 (line 1) and 40 to 67 (line 2); for a 4-line display from 00 to 13, 20 to 33, 40 to 53 and 60 to 73 for lines 1, 2, 3 and 4 respectively.
For 2 and 4-line displays the end address of one line and the start address of the next line are not consecutive. When the display is shifted each line wraps around independently of the others (Figs 6 and 7).

When data is written into the DDRAM wrap-around occurs from 4F to 00 in 1-line mode and from 27 to 40 and 67 to 00 in 2-line mode; from 13 to 20, 33 to 40, 53 to 60 and 73 to 00 in 4-line mode.

8.12 Character generator ROM (CGROM)

The character generator ROM generates 240 character patterns in 5×8 dot format from 8-bit character codes. Figures 8 to 10 show the character sets currently available.

8.13 Character generator RAM (CGRAM)

Up to 16 user-defined characters may be stored in the character generator RAM. The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.8). Figure 11 shows the addressing principle for the CGRAM.

8.14 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or character blink as shown in Fig.12) at the DDRAM address contained in the Address Counter. When the Address Counter contains the CGRAM address the cursor will be inhibited.

8.15 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.16 LCD row and column drivers

The PCF2116 contains 32 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display, in accordance with the data to be displayed. The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 13 and 14 show typical waveforms.

In 1-line mode (1 : 16) the row outputs are driven in pairs: R1/R17, R2/R18 for example. This allows the output pairs to be connected in parallel, providing greater drive capability.

Unused outputs should be left unconnected.

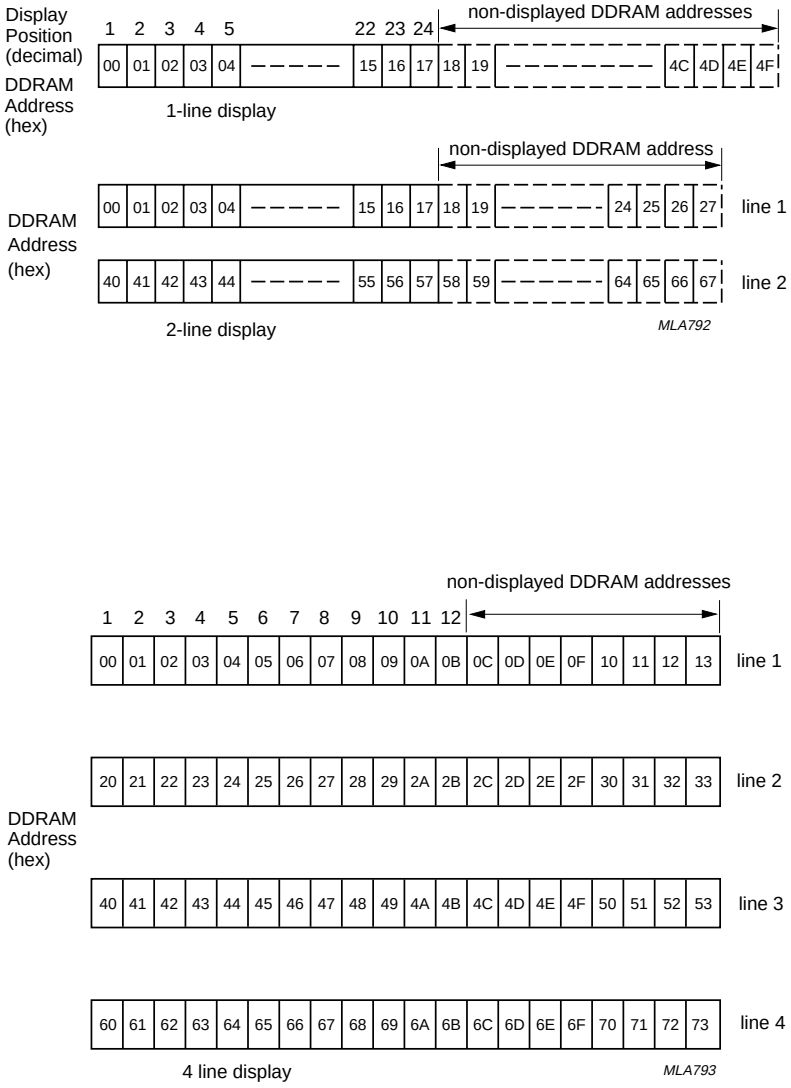
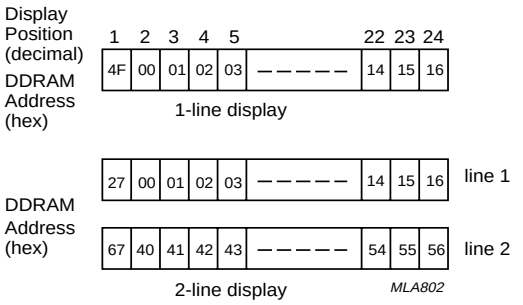


Fig.5 DDRAM-to-display mapping; no shift.



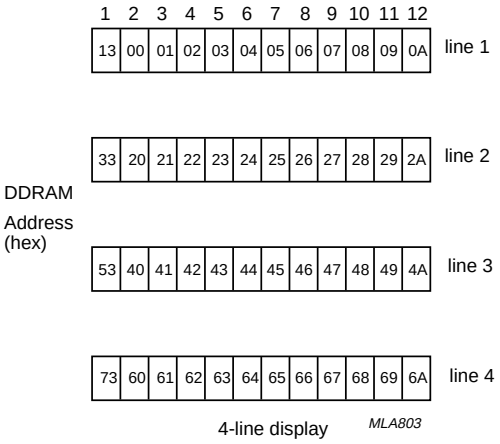
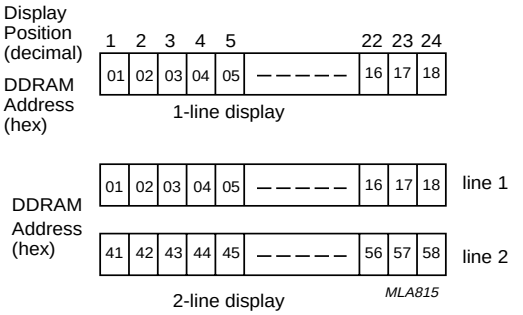


Fig.6 DDRAM-to-display mappi7ng; right shift.



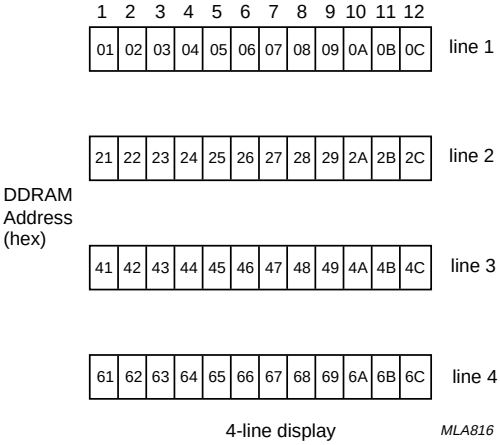


Fig.7 DDRAM-to-display mapping; left shift.

lower 6 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

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Fig.8 Character set ‘A’ in CGROM: **PCF2116A; PCF2114A.**

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

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Fig.9 Character set ‘C’ in CGROM: **PCF2116C; PCF2114C**.

lower 6 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	CG RAM 1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

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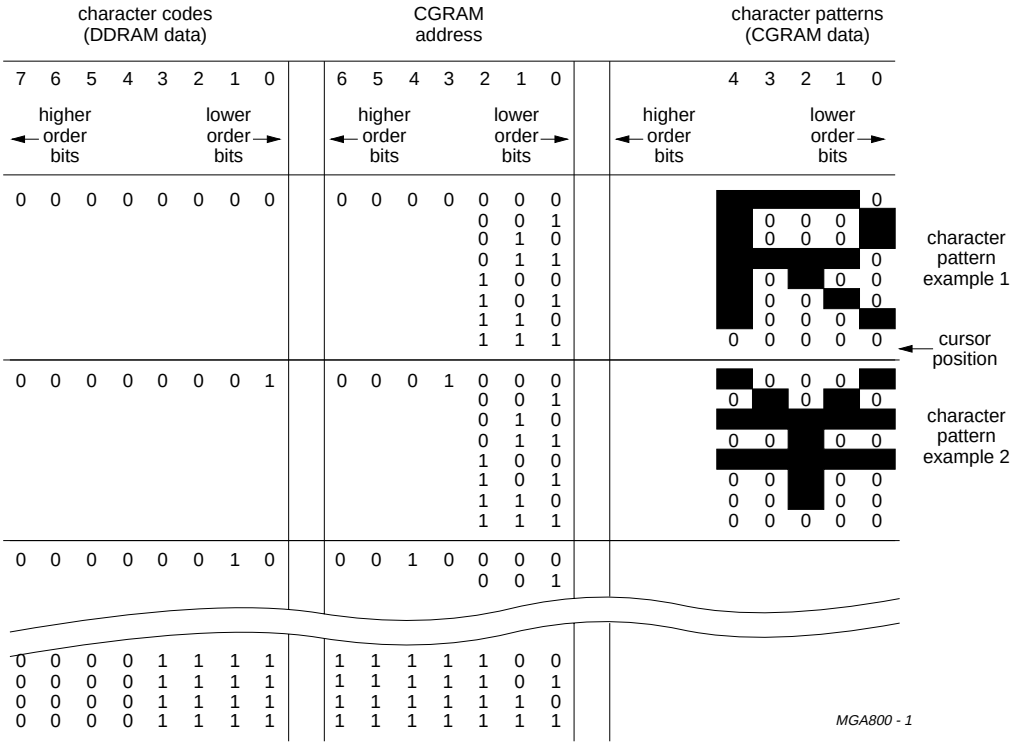
Fig.10 Character set ‘G’ in CGROM: **PCF2116G; PCF2114G**.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

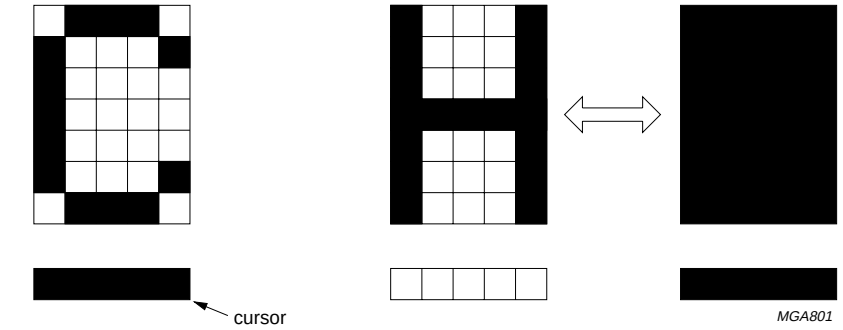
CGRAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th line will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.11 (bit 4 being at the left end).

As shown in Figs 8 and 11, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the ‘Set CGRAM address’ instruction. Bit 6 can be set using the ‘Set DDRAM address’ instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the ‘Read busy flag and address’ instruction.

Fig.11 Relationship between CGRAM addresses and data and display patterns.



5 x 7 dot character font

alternating display

cursor display example

blink display example

Fig.12 Cursor and blink display examples.

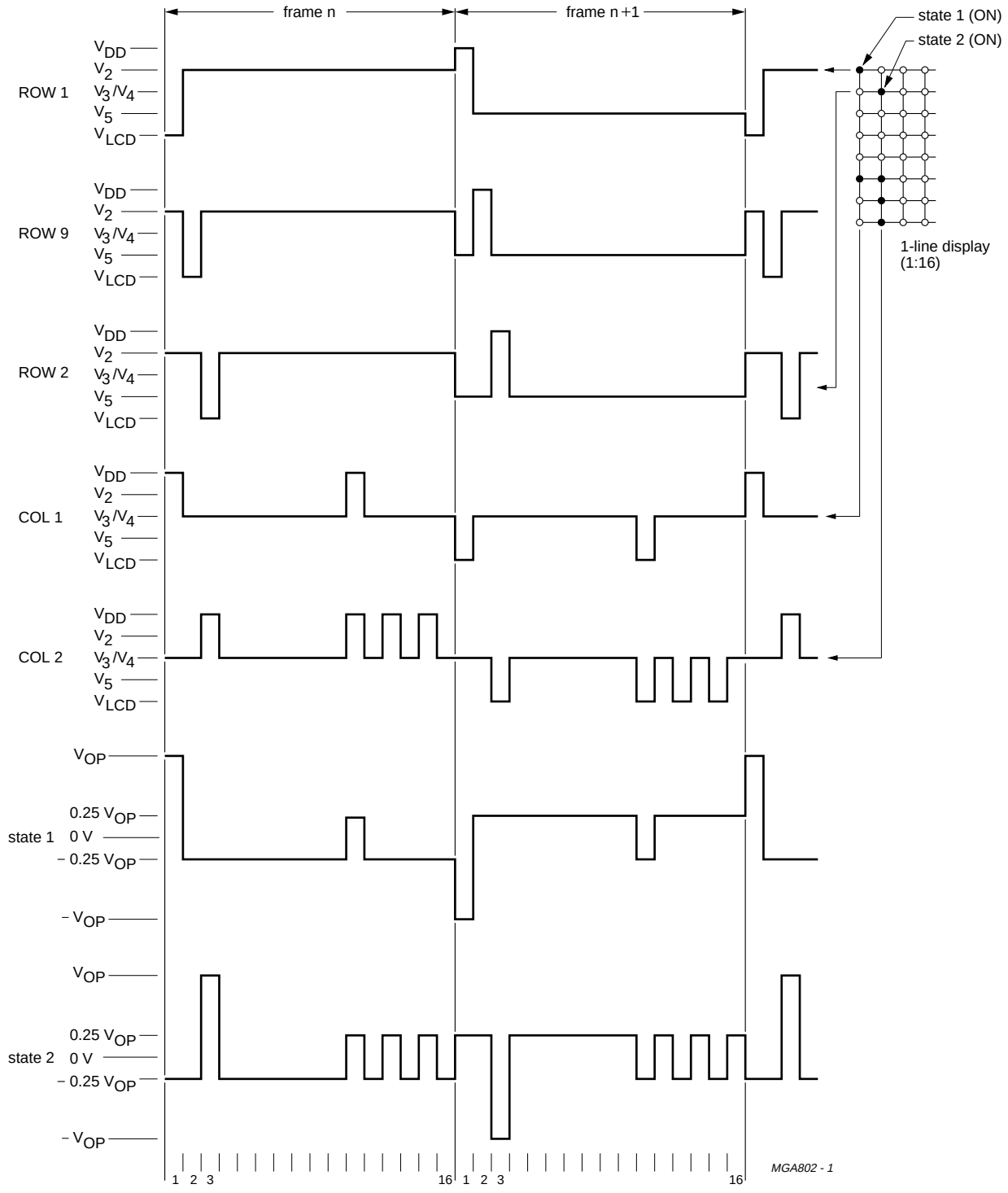


Fig.13 Typical LCD waveforms; 1-line mode.

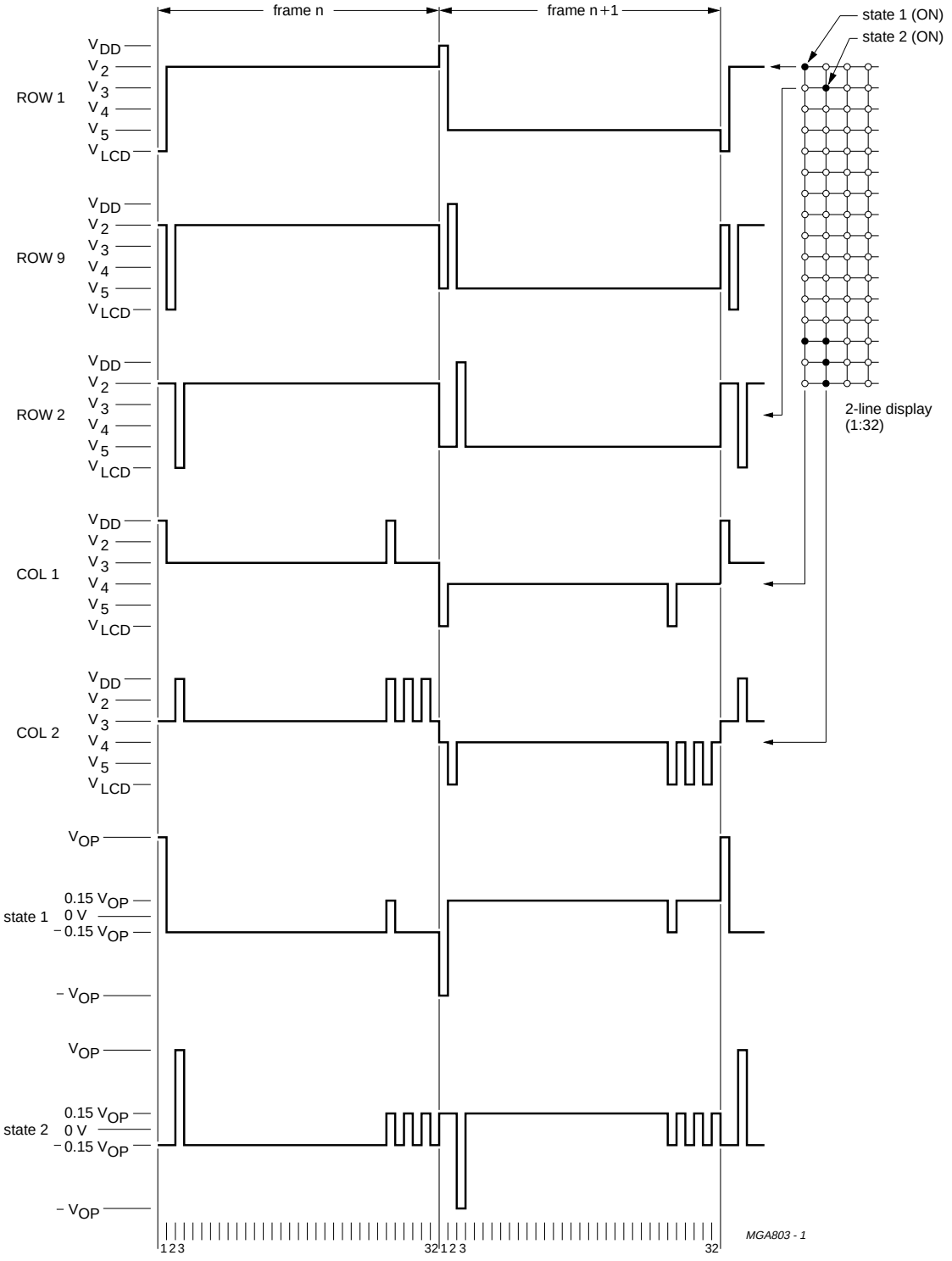


Fig.14 Typical LCD waveforms; 2-line mode.

8.17 Programming MUX 1 : 16 displays with the PCF2114x

The PCF2114x can be used in:

- 1-line mode to drive a 2-line display
- 2 × 12 characters with MUX rate 1 : 16, resulting in better contrast. The internal data flow of the chip is optimized for this purpose.

With the ‘Function set’ instruction M and N are set to 0, 0. Figures 15 to 17 show DDRAM addresses of the display characters. The second row of each table corresponds to either the right half of a 1-line display or to the second line of a 2-line display. Wrap around of data during display shift or when writing data is non-standard.

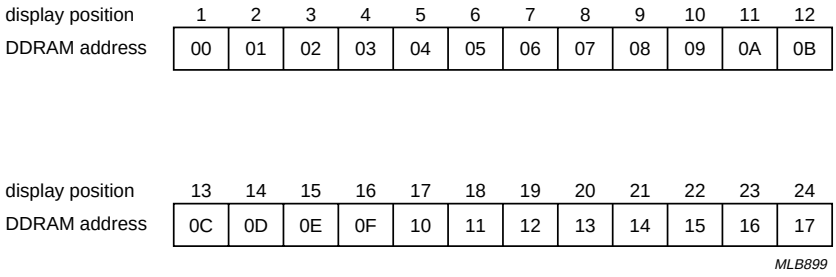


Fig.15 DDRAM-to-display mapping; no shift (PCF2114x).

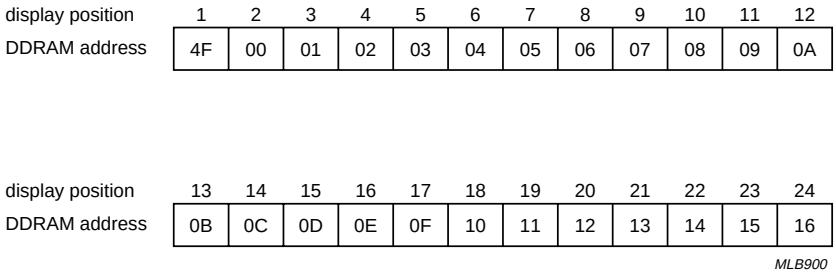


Fig.16 DDRAM-to-display mapping; right shift (PCF2114x).

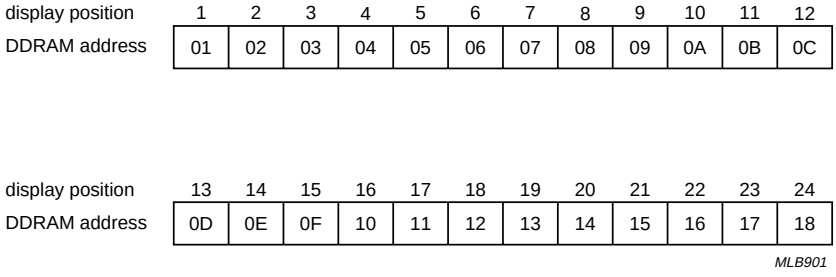


Fig.17 DDRAM-to-display mapping; left shift (PCF2114x).

8.18 Programming MUX 1 : 32 displays with the PCF2114x

To drive a 2-line by 24 characters MUX 1 : 32 display, use instruction 'Function set' M, N to 0, 1. Note that the right half of the display needs mirrored column connection compared to a display driven by a PCF2116x.

To drive a 4-line by 12 characters MUX 1 : 32 display the PCF2116x operating instructions apply. There is no functional difference between the PCF2114x and the PCF2116x in this mode. For such an application set M, N to 1, 1 with the 'Function set' instruction.

8.19 Reset function

The PCF2116 automatically initializes (resets) when power is turned on. After reset the chip has the following state.

Table 2 State after reset

STEP	DESCRIPTION		
1	display clear		
2	function set	DL = 1	8-bit interface
		M, N = 0	1-line display
		G = 0	voltage generator; $V_{LCD} = V_0$
3	display on/off control	D = 0	display off
		C = 0	cursor off
		B = 0	blink off
4	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
5	Default address pointer to DDRAM. The Busy Flag (BF) indicates the busy state (BF = logic 1) until initialization ends. The busy state lasts 2 ms. The chip may also be initialized by software. See Figs 28 and 29.		
6	I^2C-bus interface reset		

9 INSTRUCTIONS

Only two PCF2116 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs.
The PCF2116 operation is controlled by the instructions shown in Table 3 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 categories, those that:

1. Designate PCF2116 functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than 'Read busy flag and address' will be executed.

Because the Busy Flag is set to logic 1 while an instruction is being executed, check to make sure it is on logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 3. An instruction sent while the Busy Flag is HIGH will not be executed.

Table 3 Instructions (note 1)

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES(2)
NOP	0	0	0	0	0	0	0	0	0	0	No operation.	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in Address Counter.	165
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 in Address Counter. Also returns shifted display to original position. DDRAM contents remain unchanged.	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	3
Display control	0	0	0	0	0	0	1	D	C	B	Sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B).	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and shifts display without changing DDRAM contents.	3
Function set	0	0	0	0	1	DL	N	M	G	0	Sets interface data length (DL), number of display lines (N, M) and voltage generator control (G).	3
Set CGRAM address	0	0	0	1	A_{CG}						Sets CGRAM address.	3
Set DDRAM address	0	0	1	A_{DD}							Sets DDRAM address.	3
Read busy flag and address	0	1	BF	A_C							Reads Busy Flag (BF) indicating internal operation is being performed and reads Address Counter contents.	0
Read data	1	1	read data								Reads data from CGRAM or DDRAM.	3
Write data	1	0	write data								Writes data to CGRAM or DDRAM.	3

Notes

1. In the I^2C-bus mode the DL bit is don't care. 8-bit mode is assumed.
   In the I^2C-bus mode a control byte is required when RS or R/$\overline{W}$ is changed; control byte: Co, RS, R/$\overline{W}$, 0, 0, 0, 0, 0; command byte: DB7 to DB0.
2. Example: f_{osc} = 150 kHz, $T_{cy} = \frac{1}{f_{osc}}$ = 6.67 µs; 3 cycles = 20 µs, 165 cycles = 1.1 ms.

Table 4 Command bit identities

BIT	0	1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	character at cursor position does not blink	character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
G	voltage generator: $V_{LCD} = V_0$	voltage generator; $V_{LCD} = V_0 - 0.8V_{DD}$
N, (M = 0)		
PCF2116x	1 line × 24 characters; MUX 1 : 16	2 lines × 24 characters; MUX 1 : 32
PCF2114x	2 line × 12 characters; MUX 1 : 16	2 lines × 24 characters; MUX 1 : 32
N, (M = 1)	reserved	4 lines × 12 characters; MUX 1 : 32
BF	end of internal operation	internal operation in progress
Co	last control byte, only data bytes to follow	next two bytes are a data byte and another control byte

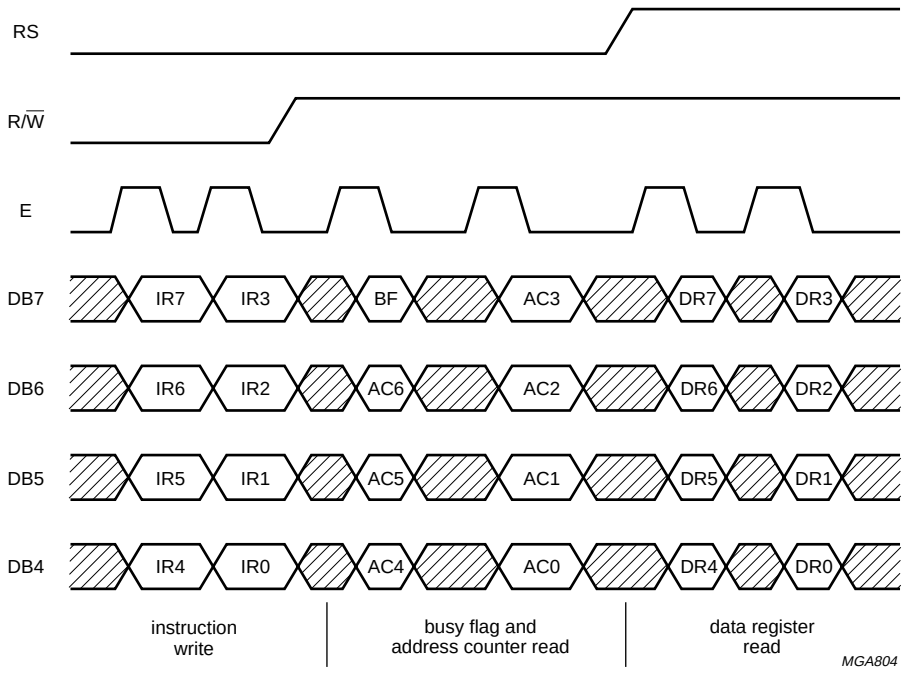
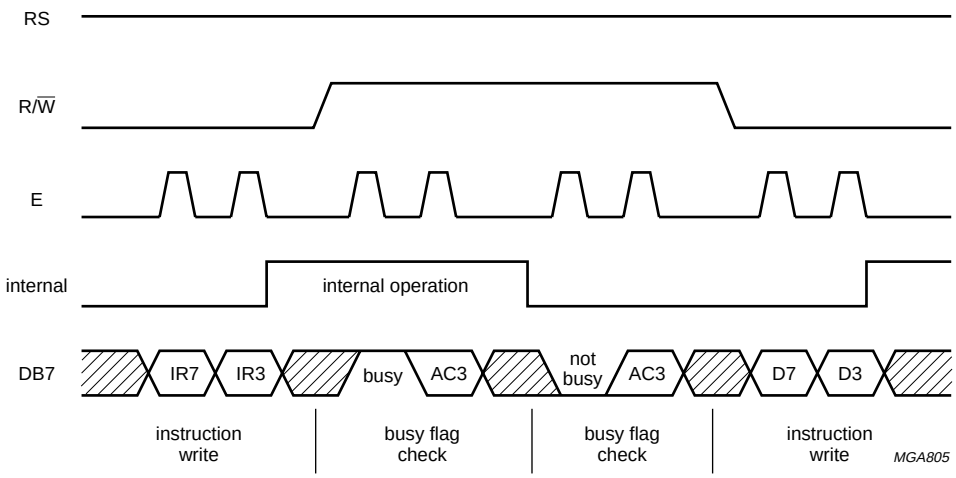


Fig.18 4-bit transfer example.



IR7, IR3: instruction 7th bit, 3rd bit.
AC3: Address Counter 3rd bit.

Fig.19 An example of 4-bit data transfer timing sequence.

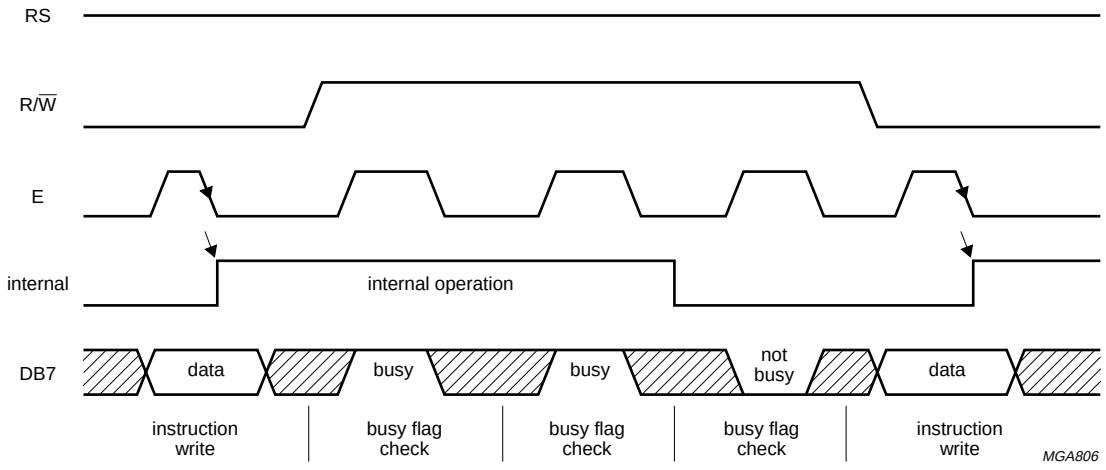


Fig.20 Example of Busy Flag check timing sequence.

9.1 Clear display

'Clear display' writes space code 20 (hexadecimal) into all DDRAM addresses (The character pattern for character code 20 must be blank pattern). Sets the DDRAM Address Counter to logic 0. Returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display (the first line if 2 or 4 lines are displayed). Sets entry mode I/D = logic 1 (increment mode). S of entry mode does not change.

The instruction 'Clear display' requires extra execution time. This may be allowed for by checking the busy-flag (BF) or by waiting until 2 ms has elapsed. The latter must be applied where no read-back options are foreseen, as in some chip-on-glass (COG) applications.

9.2 Return home

'Return home' sets the DDRAM Address Counter to logic 0. Returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the display (the first line if 2 or 4 lines are displayed). I/D and S of entry mode do not change.

9.3 Entry mode set

9.3.1 I/D

When I/D = logic 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor and blink are inhibited when the CGRAM is accessed.

9.3.2 S

When S = logic 1, the entire display shifts either to the right (I/D = logic 0) or to the left (I/D = logic 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = logic 0 the display does not shift.

9.4 Display on/off control

9.4.1 D

The display is on when D = logic 1 and off when D = logic 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

9.4.2 C

The cursor is displayed when C = logic 1 and inhibited when C = logic 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.12).

9.4.3 B

The character indicated by the cursor blinks when B = logic 1. The blink is displayed by switching between display characters and all dots on with a period of 1 second when f_{osc} = 150 kHz (see Fig.12). At other clock frequencies the blink period is equal to 150 kHz/f_{osc}. The cursor and the blink can be set to display simultaneously.

9.5 Cursor/display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2 or 4-line displays, the cursor moves to the next line when it passes the last position (40 or 20 decimal) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line. The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the cursor shift.

9.6 Function set

9.6.1 DL (PARALLEL MODE ONLY)

Defines interface data width when the parallel data interface is used.

Data is sent or received in bytes (bits DB7 to DB0) when DL = logic 1, or in two 4-bit nibbles (DB7 to DB4) when DL = logic 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus(1).

When using the I^{2}C-bus interface the DL should not previously have been set to 0 using the parallel interface.

9.6.2 N, M

Sets number of display lines.

(1) In a 4-bit application DB3 to DB0 are left open (internal pull-ups). Hence in the first 'Function set' instruction after power-on, G and H are set to 1. A second 'Function set' must then be sent (2 nibbles) to set G and H to their required values.

9.6.3 G

Controls the V_{LCD} voltage generator characteristic.

9.7 Set CGRAM address

'Set CGRAM address' sets bit 0 to 5 of the CGRAM address (A_{CG} in Table 3) into the Address Counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Only bits 0 to 5 of the CGRAM address are set by the 'Set CGRAM address' instruction. Bit 6 can be set using the 'Set DDRAM address' instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'Read busy flag and address' instruction.

9.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address (A_{DD} in Table 3) into the Address Counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

Hexadecimal address ranges.

ADDRESS	FUNCTION
00 to 4F	1-line by 24; 2114x/2116x
00 to 0B and 0C to 4F	2-line by 12; 2114x
00 to 27 and 40 to 67	2-line by 24; 2114x/2116x
00 to 13, 20 to 33, 40 to 53 and 60 to 73	4-line by 12; 2114x/2116x

9.9 Read busy flag and address

'Read busy flag and address' reads the Busy Flag (BF). BF = logic 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = logic 0, so BF should be checked before sending another instruction.

At the same time, the value of the Address Counter (A_C in Table 3) expressed in binary A[6] to A[0] is read out. The Address Counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

9.10 Write data to CGRAM or DDRAM

Writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous specification of CGRAM or DDRAM address setting.

After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

9.11 Read data from CGRAM or DDRAM

Reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'Set address' instruction determines whether the CGRAM or DDRAM is to be read.

The 'Read data' instruction gates the content of the data register (DR) to the bus while E = HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Remark: the only three instructions that update the data register (DR) are:

- 'Set CGRAM address'
- 'Set DDRAM address'
- 'Read data' from CGRAM or DDRAM.

Other instructions (e.g. 'Write data', 'Cursor/Display shift', 'Clear display', 'Return home') will not modify the data register content.

10 INTERFACE TO MICROCONTROLLER (PARALLEL INTERFACE)

The PCF2116 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB0 to DB7. Three further control lines E, RS, and R/$\overline{W}$ are required.

In 4-bit mode data is transferred in two cycles of 4-bits each. The higher order bits (corresponding to DB4 to DB7 in 8-bit mode) are sent in the first cycle and the lower order bits (DB0 to DB3 in 8-bit mode) in the second.
Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the Busy Flag check. 4-bit operation is selected by instruction. See Figs 18, 19 and 20 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

11 INTERFACE TO MICROCONTROLLER (I²C-BUS INTERFACE)

11.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

11.2 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

11.3 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

11.4 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

11.5 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

11.6 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2116 READ and WRITE cycles is shown in Figs 25 to 27.

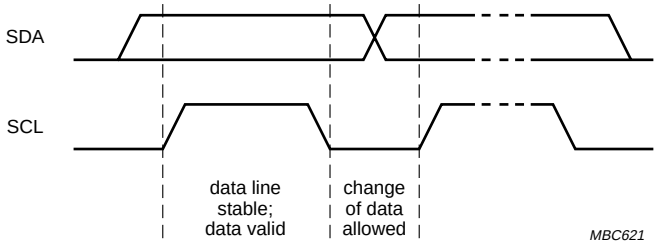


Fig.21 Bit transfer.

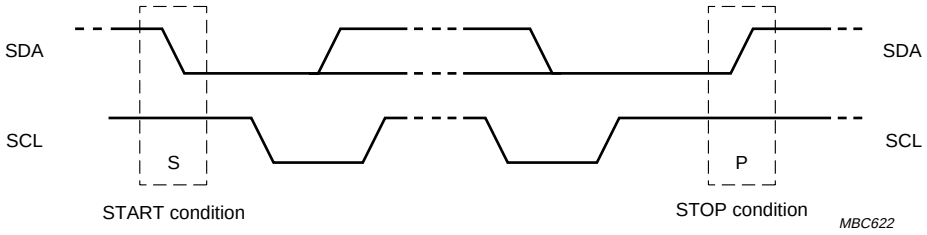


Fig.22 Definition of START and STOP conditions.

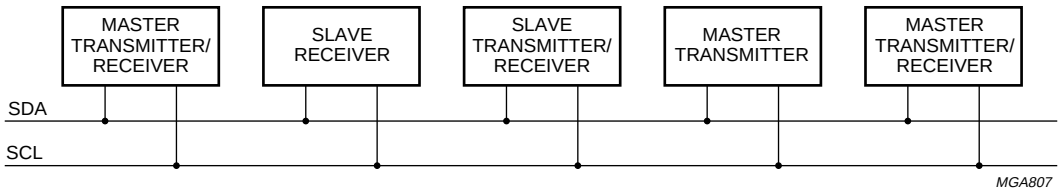


Fig.23 System configuration.

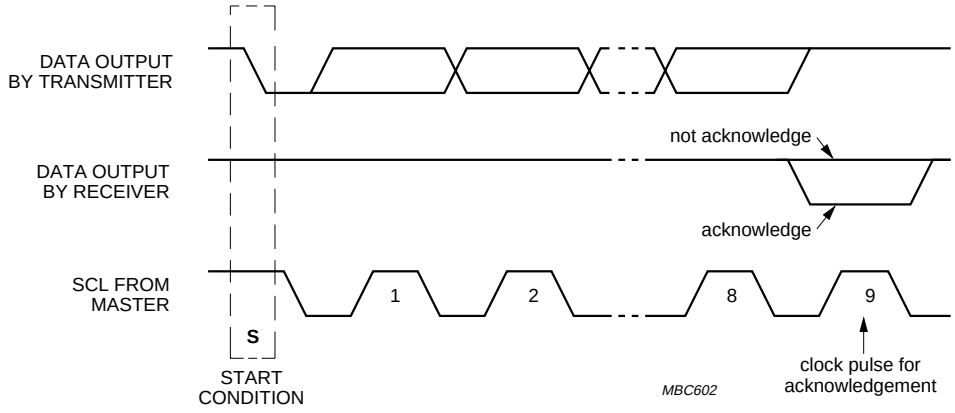


Fig.24 Acknowledgement on the I^2C-bus.

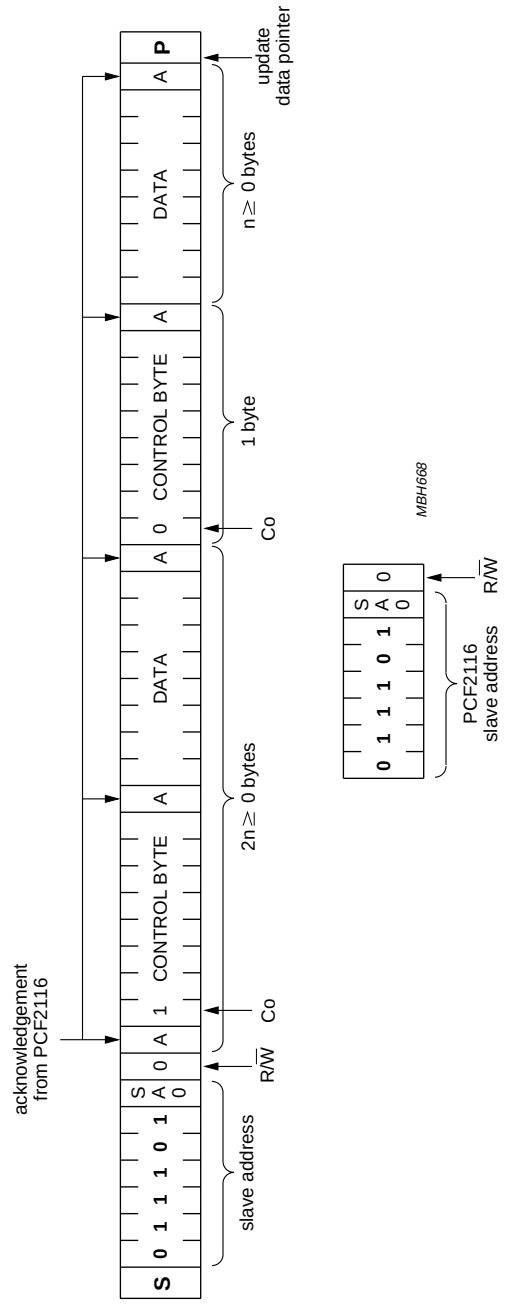
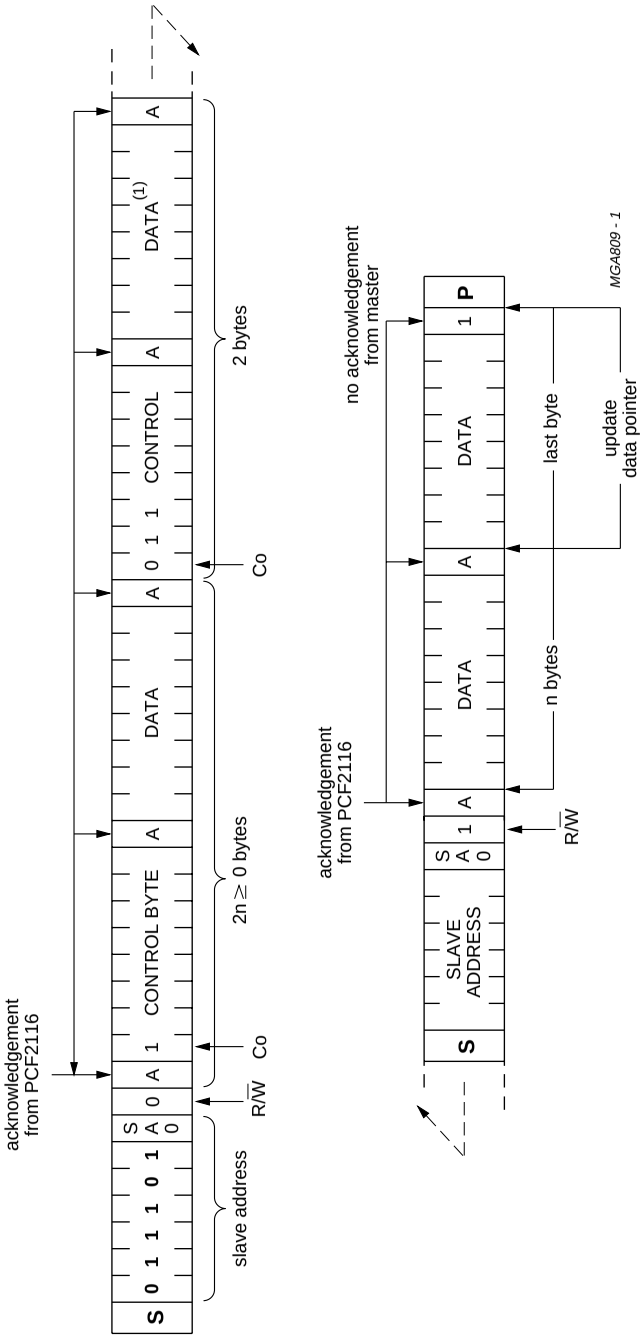


Fig.25 Master transmits to slave receiver; WRITE mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.26 Master reads after setting word address; write word address, set RS/$\overline{RW}$; READ data.

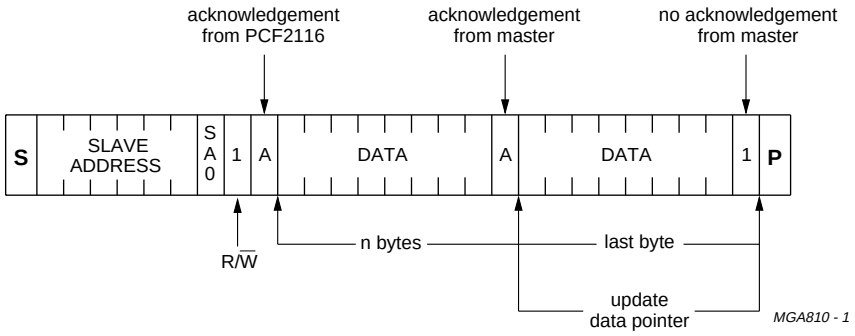


Fig.27 Master reads slave immediately after first byte; READ mode (RS previously defined).

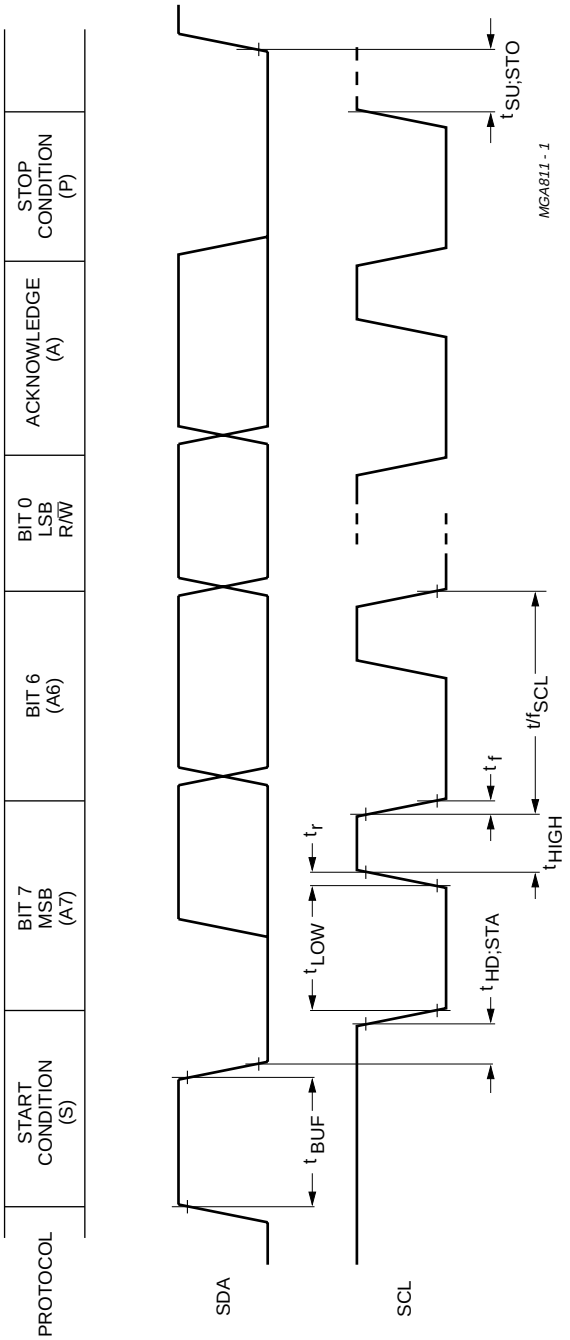


Fig.28 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} – 11	V_{DD}	V
V_I	input voltage OSC, V_0, RS, R/$\overline{W}$, E and DB0 to DB7	V_{SS} – 0.5	V_{DD} + 0.5	V
V_O	output voltage R1 to R32, C1 to C60 and V_{LCD}	V_{LCD} – 0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	–50	+50	mA
P_{tot}	total power dissipation	–	400	mW
P_O	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

13 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS Devices”*).

14 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 to V_{DD} − 9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
I_{DD}	supply current external V_{LCD}	note 1				
I_{DD1}	supply current 1		–	200	500	μA
I_{DD2}	supply current 2	V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	200	300	μA
I_{DD3}	supply current 3	V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	150	200	μA
I_{DD}	supply current internal V_{LCD}	notes 1, 2 and 8				
I_{DD4}	supply current 4		–	700	1100	μA
I_{DD5}	supply current 5	V_{DD} = 5 V; V_{OP} = 9 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	600	900	μA
I_{DD6}	supply current 6	V_{DD} = 3 V; V_{OP} = 5 V; f_{osc} = 150 kHz; T_{amb} = 25 °C	–	500	800	μA
I_{LCD}	V_{LCD} input current	notes 1 and 7	–	50	100	μA
V_{POR}	power-on reset voltage level	note 3	–	1.3	1.8	V
Logic						
V_{IL1}	LOW level input voltage E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		V_{SS}	–	0.3V_{DD}	V
V_{IH1}	HIGH level input voltage E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		0.7V_{DD}	–	V_{DD}	V
$V_{IL(osc)}$	LOW level input voltage OSC		V_{SS}	–	V_{DD} − 1.5	V
$V_{IH(osc)}$	HIGH level input voltage OSC		V_{DD} − 0.1	–	V_{DD}	V
$V_{IL(V0)}$	LOW level input voltage V_0		V_{SS}	–	V_{DD} − 0.5	V
$V_{IH(V0)}$	HIGH level input voltage V_0		V_{DD} − 0.05	–	V_{DD}	V
I_{pu}	pull-up current at DB0 to DB7	V_I = V_{SS}	0.04	0.15	1.00	μA
$I_{OL(DB)}$	LOW level output current DB0 to DB7	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	–	–	mA
$I_{OH(DB)}$	HIGH level output current DB0 to DB7	V_{OH} = 4 V; V_{DD} = 5 V	−1.0	–	–	mA
I_{L1}	leakage current OSC, V_0, E, RS, R/$\overline{W}$, DB0 to DB7 and SA0	V_I = V_{DD} or V_{SS}	−1	–	+1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus						
SDA, SCL						
V_{IL2}	LOW level input voltage	note 4	V_{SS}	–	$0.3V_{DD}$	V
V_{IH2}	HIGH level input voltage	note 4	$0.7V_{DD}$	–	V_{DD}	V
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	μA
C_i	input capacitance	note 5	–	–	7	pF
$I_{OL(SDA)}$	LOW level output current (SDA)	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
R_{ROW}	row output resistance R1 to R32	note 6	–	1.5	3	kΩ
R_{COL}	column output resistance C1 to C60	note 6	–	3	6	kΩ
V_{tol1}	bias voltage tolerance R1 to R32 and C1 to C60	note 7	–	±20	±130	mV
V_{tol2}	LCD supply voltage (V_{LCD}) tolerance	note 2	–	±40	±300	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; $V_0 = V_{DD}$; bus inactive; internal or external clock with duty cycle 50% (I_{DD1} only).
2. LCD outputs are open-circuit; LCD supply voltage generator is on; load current at V_{LCD} = 20 μA.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
5. Tested on sample basis.
6. Resistance of output terminals (R1 to R32 and C1 to C60) with load current = 150 μA; $V_{OP} = V_{DD} - V_{LCD}$ = 9 V; outputs measured one at a time; (external V_{LCD}).
7. LCD outputs open-circuit; external V_{LCD}.
8. Maximum value occurs at 85 °C.

15 DC CHARACTERISTICS (PCF2116K)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; $V_{LCD} = V_{DD} - 3.5$ to $V_{DD} - 9$ V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		$V_{DD} - 9$	–	$V_{DD} - 3.5$	V
V_0	voltage generator control input voltage		V_{SS}	–	$V_{DD} - 0.5$	V
R_0	voltage generator control input resistance	T_{amb} = 25 °C; note 1	700	1000	1300	kΩ

Note

1. R_0 has a temperature coefficient of resistance of +0.6%/K.

16 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal clock); note 1	40	65	100	Hz
f_{osc}	external clock frequency	90	150	225	kHz
Bus timing characteristics: Parallel Interface; notes 1 and 2					
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2116)					
T_{cy}	enable cycle time	500	–	–	ns
PW_{EH}	enable pulse width	220	–	–	ns
t_{ASU}	address set-up time	50	–	–	ns
t_{AH}	address hold time	25	–	–	ns
t_{DSW}	data set-up time	60	–	–	ns
t_{HD}	data hold time	25	–	–	ns
READ OPERATION (READING DATA FROM PCF2116 TO MICROCONTROLLER)					
T_{cy}	enable cycle time	500	–	–	ns
PW_{EH}	enable pulse width	220	–	–	ns
t_{ASU}	address set-up time	50	–	–	ns
t_{AH}	address hold time	25	–	–	ns
t_{DHD}	data delay time	–	–	150	ns
t_{HD}	data hold time	20	–	100	ns
Timing characteristics: I^2C-bus interface; note 2					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SW}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4	–	–	µs
t_r	SCL and SDA rise time	–	–	1	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition	4	–	–	µs

Notes

1. V_{DD} = 5 V.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

17 TIMING CHARACTERISTICS

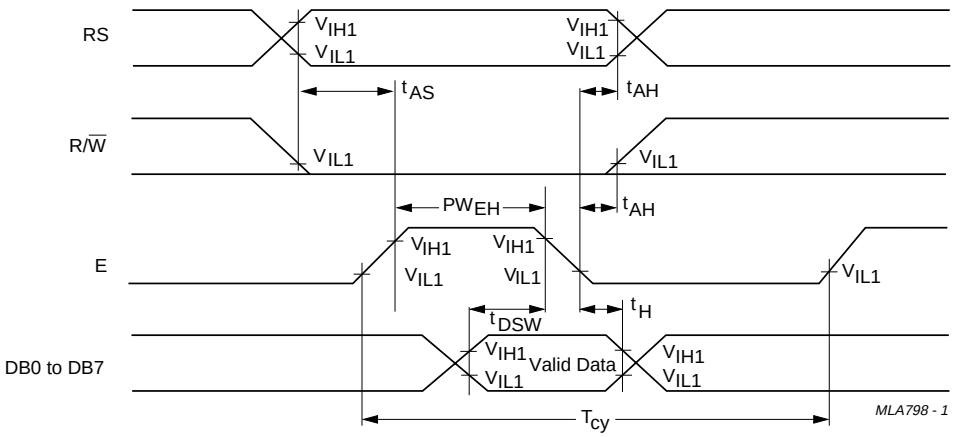


Fig.29 Parallel bus write operation sequence; writing data from microcontroller to PCF2116.

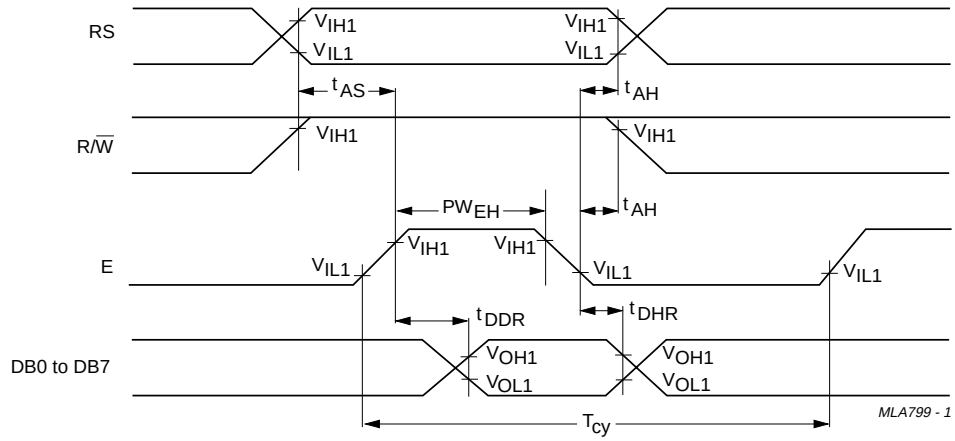


Fig.30 Parallel bus read operation sequence; reading data from PCF2116 to microcontroller.

18 APPLICATION INFORMATION

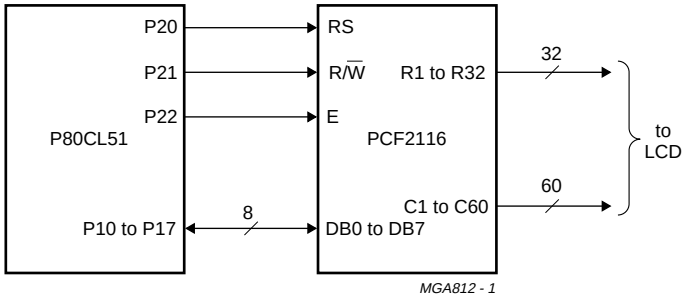


Fig.31 Direct connection to 8-bit microcontroller; 8-bit bus.

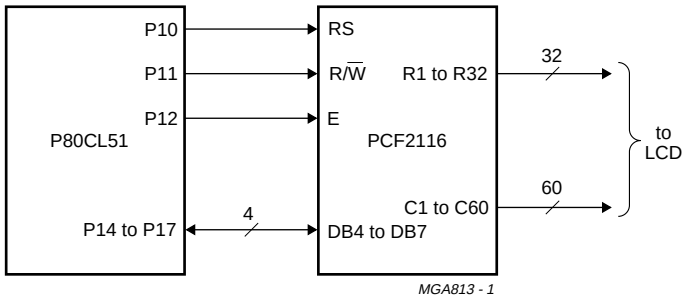


Fig.32 Direct connection to 8-bit microcontroller; 4-bit bus.

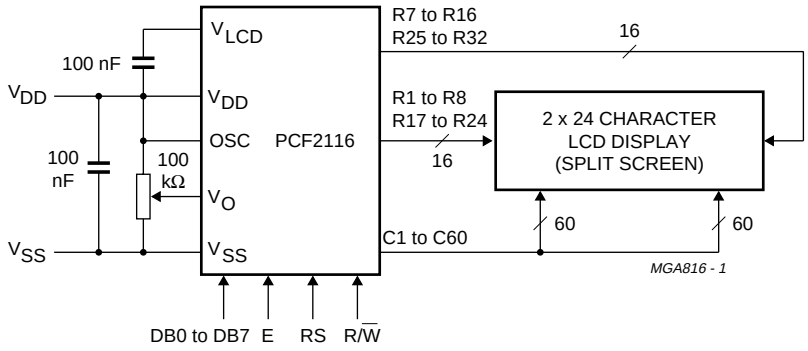


Fig.33 Typical application using parallel interface.

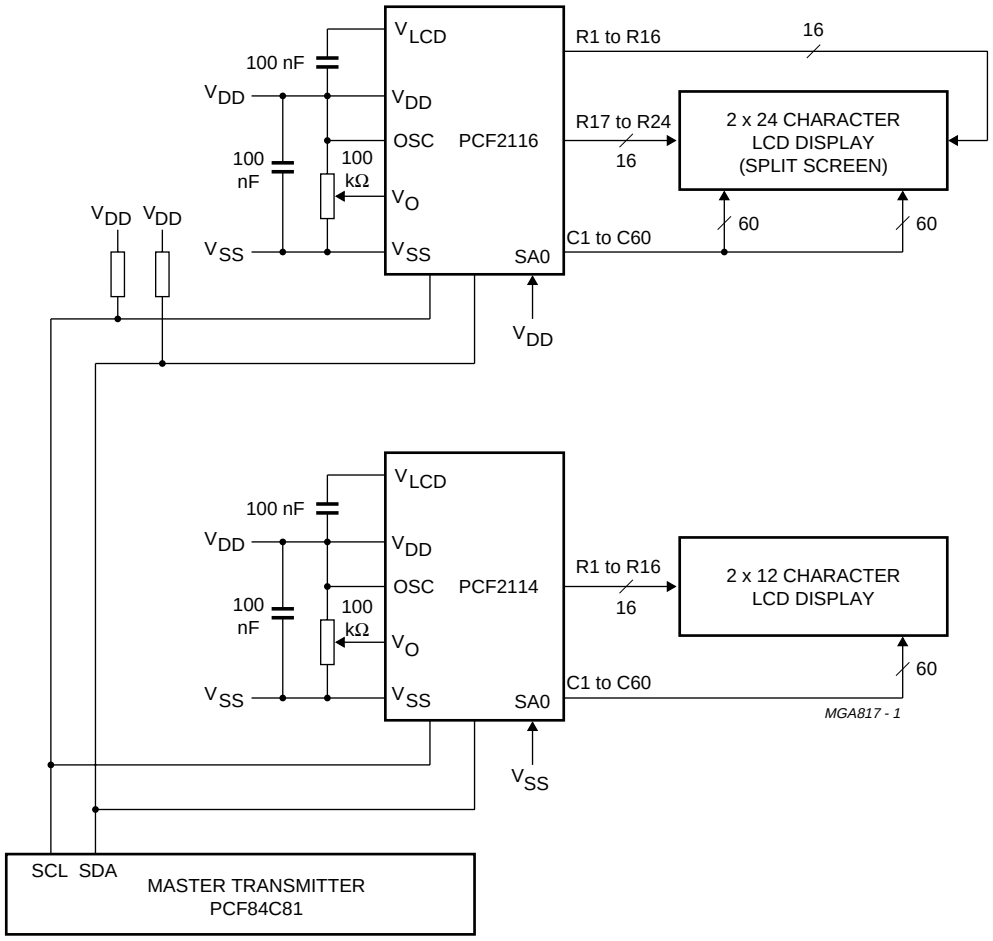


Fig.34 Application using I²C-bus interface.

18.1 8-bit operation, 1-line display using internal reset

Table 6 shows an example of a 1-line display in 8-bit operation. The PCF2116 functions must be set by the 'Function set' instruction prior to display. Since the display data RAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the Return Home operation is performed.

18.2 4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation. Table 5 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2116 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 5 step 3).

Thus, DB4 to DB7 of the function set are written twice.

18.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 7). Note that both lines of the display are always shifted together; data does not shift from one line to the other.

18.4 I^2C operation, 1-line display

A control byte is required with most instructions (see Table 8).

18.5 Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the PCF2116 must be initialized by instruction. Tables 9 and 10 show how this may be performed for 8-bit and 4-bit operation.

Table 5 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2116 is initialized by the internal reset circuit)							Initialized. No display appears.
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		Sets to 4-bit operation. In this instance operation is handled as 8-bits by initialization and only this instruction completes with one write.
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		Sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$. 4-bit operation starts from this point and resetting is needed.
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	Turns on display and cursor. Entire display is blank after initialization.
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
	0	0	0	1	1	0		
6	write data to CGRAM/DDRAM							
	1	0	0	1	0	1	**P**_	Writes 'P'. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
	1	0	0	0	0	0		

Table 6 8-bit operation, 1-line display example; using internal reset (character set ‘A’)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2116 is initialized by the internal reset function)		Initialized. No display appears.
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		Sets to 8-bit operation, selects 1-line display and $V_{LCD} = V_0$.
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM. Display is not shifted.
5	write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	Writes ‘P’. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6	write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	Writes ‘H’.
7			
8	write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	Writes ‘S’.
9	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	Sets mode for display shift at the time of write.
10	write data to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**PHILIPS**_	Writes space.
11	write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS M**_	Writes ‘M’.

STEP	INSTRUCTION	DISPLAY	OPERATION
12		|	
		|	
		|	
13	write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**MICROKO_**	Writes ‘O’.
14	cursor or display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	Shifts only the cursor position to the left.
15	cursor or display shift 0 0 0 0 0 1 0 0 0 0	**MICROKO**	Shifts only the cursor position to the left.
16	write data to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1	**ICROCO**	Writes ‘C’ correction. The display moves to the left.
17	cursor or display shift 0 0 0 0 0 1 1 1 0 0	**MICROCO**	Shifts the display and cursor to the right.
Z18	cursor or display shift 0 0 0 0 0 1 0 1 0 0	**MICROCO_**	Shifts only the cursor to the right.
19	write data to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ICROCOM_**	Writes ‘M’.
20		|	
		|	
		|	
21	Return Home 0 0 0 0 0 0 0 0 1 0	**PHILIPS M**	Returns both display and cursor to the original position (address 0).

Table 7 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2116 is initialized by the internal reset function)		Initialized. No display appears.
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		Sets to 8-bit operation, selects 2-line display and voltage generator off.
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is blank after initialization.
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM w 1 0 0 1 0 1 0 0 0 0	**P**_	Writes ‘P’. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
6		|	
7	write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	Writes ‘S’.
8	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	Sets DDRAM address to position the cursor at the head of the 2nd line.
9	write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	Writes ‘M’.
10		|	

STEP	INSTRUCTION	DISPLAY	OPERATION
11	write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 1 1	**PHILIPS** **MICROCO_**	Writes ‘O’.
12	write data to CGRAM/ DDRAM 0 0 0 0 0 0 0 1 1 1	**PHILIPS** **MICROCO_**	Sets mode for display shift at the time of write.
13	write data to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **ICROCOM_**	Writes ‘M’. Display is shifted to the left. The first and second lines shift together.
14			
15	return Home 0 0 0 0 0 0 0 0 1 0	**PHILIPS** **MICROCOM**	Returns both display and cursor to the original position (address 0).

Table 8 Example of I^2C operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	I^2C BYTE	DISPLAY	OPERATION
1	I^2C START		Initialized. No display appears.
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		During the acknowledge cycle SDA will be pulled-down by the PCF2116.
3	send a control byte for function set Co RS R/$\overline{W}$ Ack 0 0 0 X X X X X 1		Control byte sets RS and R/$\overline{W}$ for following data bytes.
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		Selects 1-line display and $V_{LCD} = V_0$; SCL pulse during acknowledge cycle starts execution of instruction.
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	Turns on display and cursor. Entire display shows character Hex 20 (blank in ASCII-like character sets).
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM. Display is not shifted.
7	I^2C START	_	For writing data to DDRAM, RS must be set to 1. Therefore a control byte is needed.
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for write data Co RS R/$\overline{W}$ Ack 0 1 0 X X X X X 1	_	
10	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	 **P**_	Writes ‘P’. The DDRAM has been selected at power-up. The cursor is incremented by 1 and shifted to the right.

STEP	I^2C BYTE	DISPLAY	OPERATION
11	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH_**	Writes ‘H’.
12 to 15	|		
16	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	Writes ‘S’.
17	(optional I^2C stop) I^2C start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS R/$\overline{W}$ Ack 1 0 0 X X X X X 1	**PHILIPS_**	
19	Return Home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	Sets DDRAM address 0 in Address Counter. (also returns shifted display to original position. DDRAM contents unchanged). This instruction does not update the Data Register (DR).
20	control byte for read Co RS R/$\overline{W}$ Ack 0 1 1 X X X X X 1	**PHILIPS**	DDRAM content will be read from following instructions. The R/$\overline{W}$ has to be set to 1 while still in I^2C-write mode.
21	I^2C START	**PHILIPS**	
22	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	During the acknowledge cycle the content of the DR is loaded into the internal I^2C interface to be shifted out. In the previous instruction neither a ‘Set address’ nor a ‘Read data’ has been performed. Therefore the content of the DR was unknown.

STEP	I^2C BYTE	DISPLAY	OPERATION
23	read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA. MSB is DB7. During master acknowledge content of DDRAM address 01 is loaded into the I^2C interface.
24	read data: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	**PHILIPS**	8 × SCL; code of letter 'H' is read first. During master acknowledge code of 'I' is loaded into the I^2C interface.
25	read data: 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	**PHILIPS**	No master acknowledge; After the content of the I^2C interface register is shifted out no internal action is performed. No new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted.
26	I^2C STOP	**PHILIPS**	

Notes

1. X = don't care.
2. SDA is left at high-impedance by the microcontroller during the READ acknowledge.

Table 9 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					↓					
wait 2 ms after V_{DD} rises above V_{POR}										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
					↓					
wait 2 ms										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
					↓					
wait more than 40 μs										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction.
0	0	0	0	1	1	X	X	X	X	Function set (interface is 8-bits long).
					↓ ↓					BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time (see Table 3).
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function set (interface is 8-bits long). Specify the number of display lines and voltage generator characteristic.
0	0	0	0	1	1	N	M	G	0	
0	0	0	0	0	0	1	0	0	0	Display off.
0	0	0	0	0	0	0	0	0	1	Clear display.
0	0	0	0	0	0	0	1	I/D	S	Entry mode set.
					↓					
Initialization ends										

Note

1. X = don’t care.

Table 10 Initialization by instruction, 4-bit interface. Not applicable for I^2C-bus operation

STEP						DESCRIPTION
power-on or unknown state						
wait 2 ms after V_{DD} rises above V_{POR}						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
wait 40 μs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction.
0	0	0	0	1	1	Function set (interface is 8-bits long).
						BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is the specified instruction time. (See Table 3).
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	Function set (set interface to 4-bits long).
0	0	0	0	1	0	Interface is 8-bits long.
0	0	0	0	1	0	Function set (interface is 4-bits long).
0	0	N	M	G	0	Specify number of display lines and voltage generator characteristic.
0	0	0	0	0	0	
0	0	1	0	0	0	Display off.
0	0	0	0	0	0	Clear display.
0	0	0	0	0	1	
0	0	0	0	0	0	Entry mode set.
0	0	0	1	I/D	S	
Initialization ends						

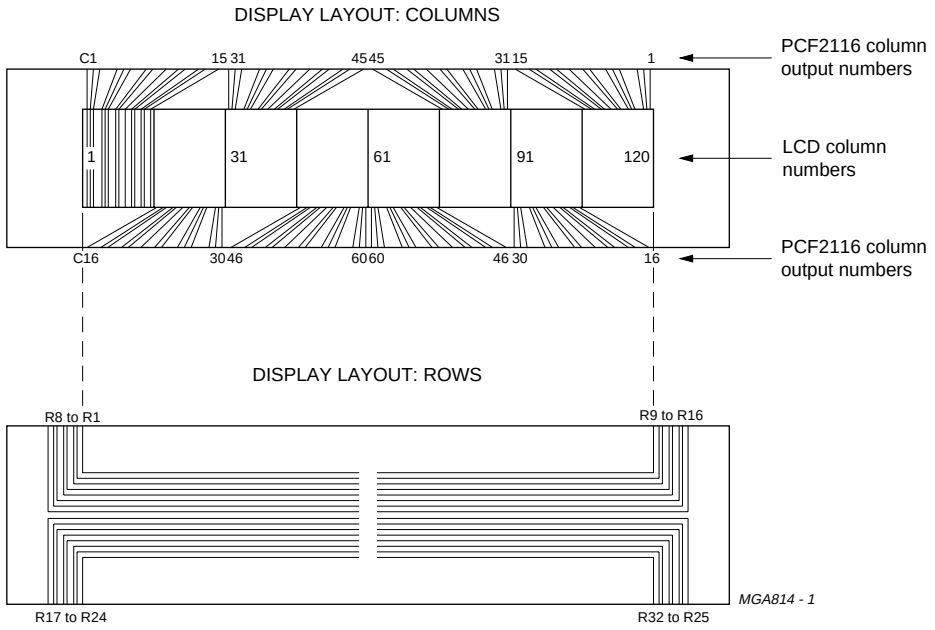


Fig.35 Example of 2 × 24 display layout (PCF2116x).

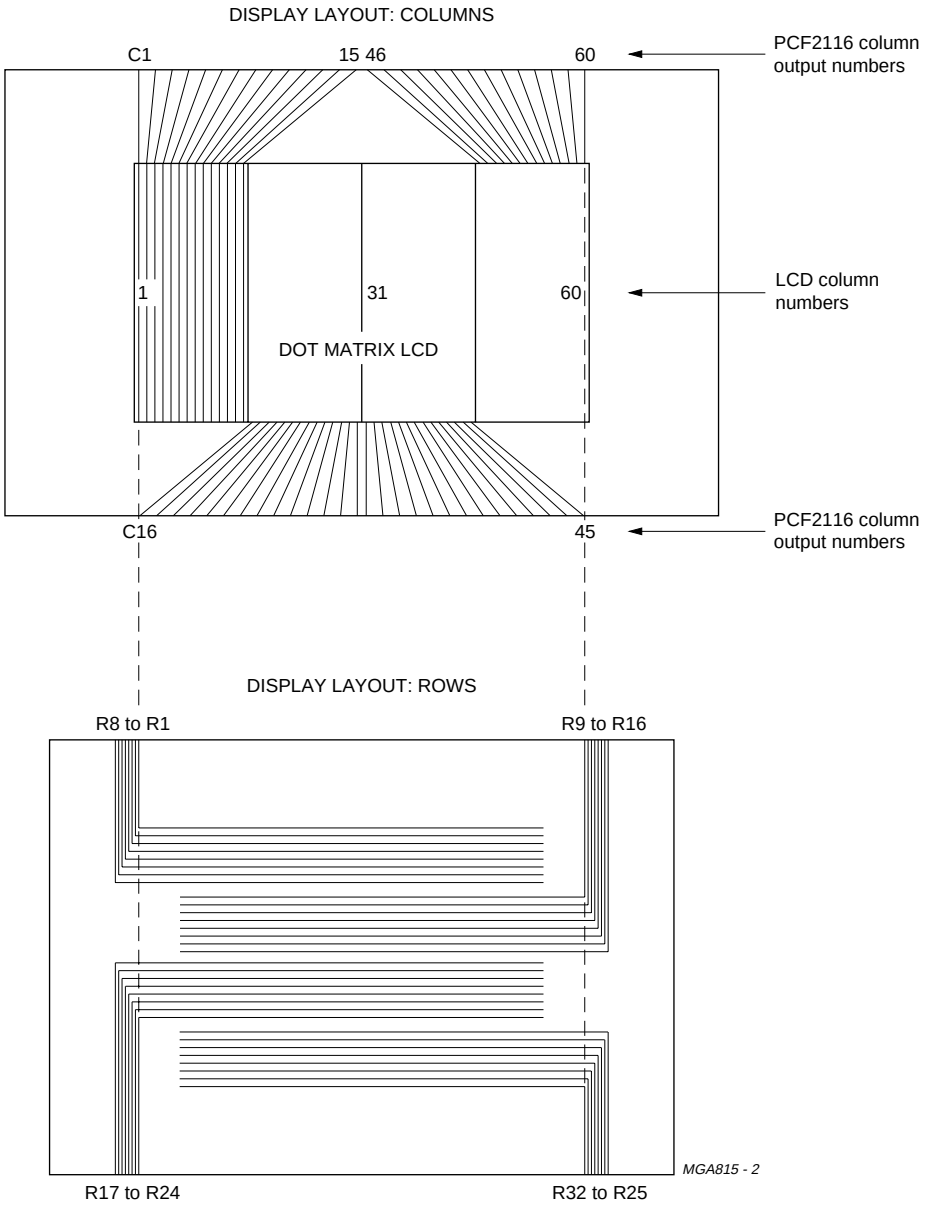


Fig.36 Example of 4 × 12 display layout (PCF2114x/PCF2116x).

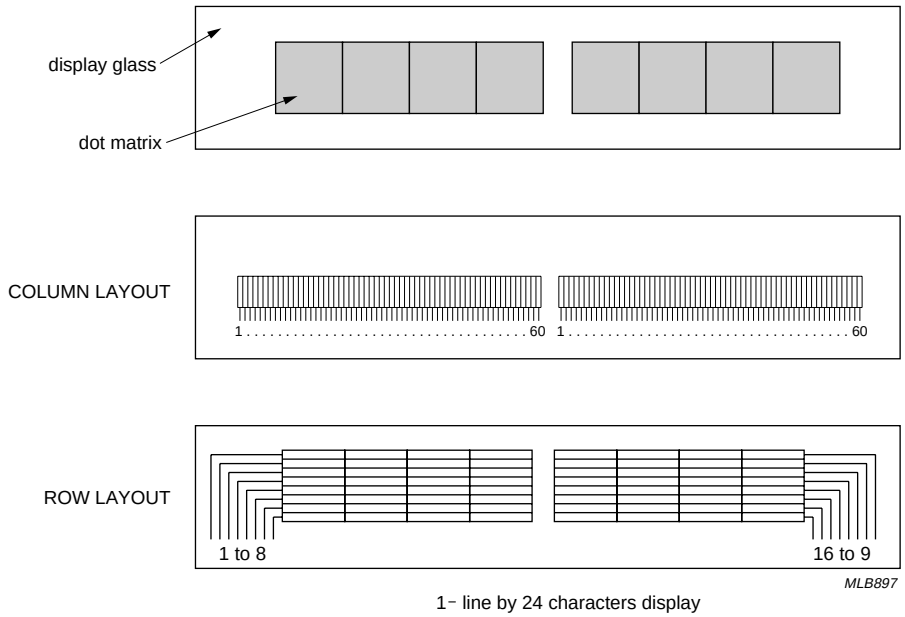


Fig.37 Display example (PCF2114x); 1-line by 24 characters.

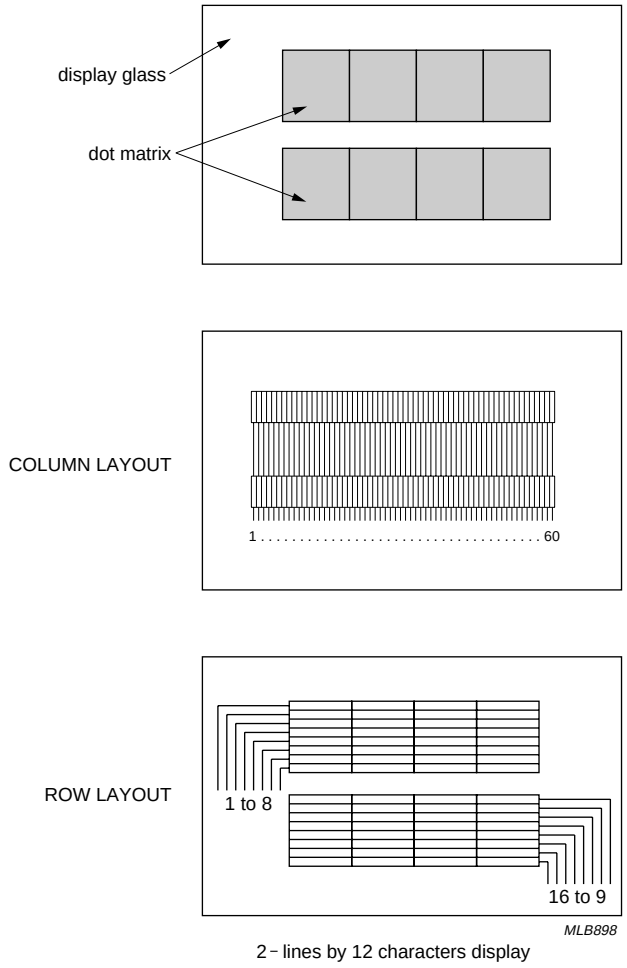


Fig.38 Display example (PCF2114x); 2-lines by 12 characters.

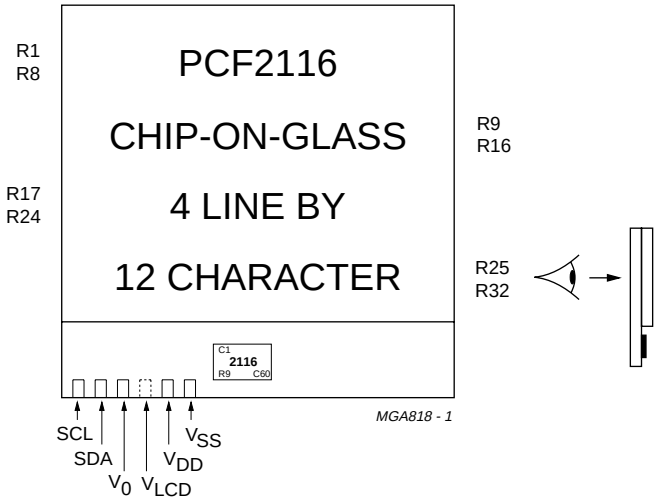
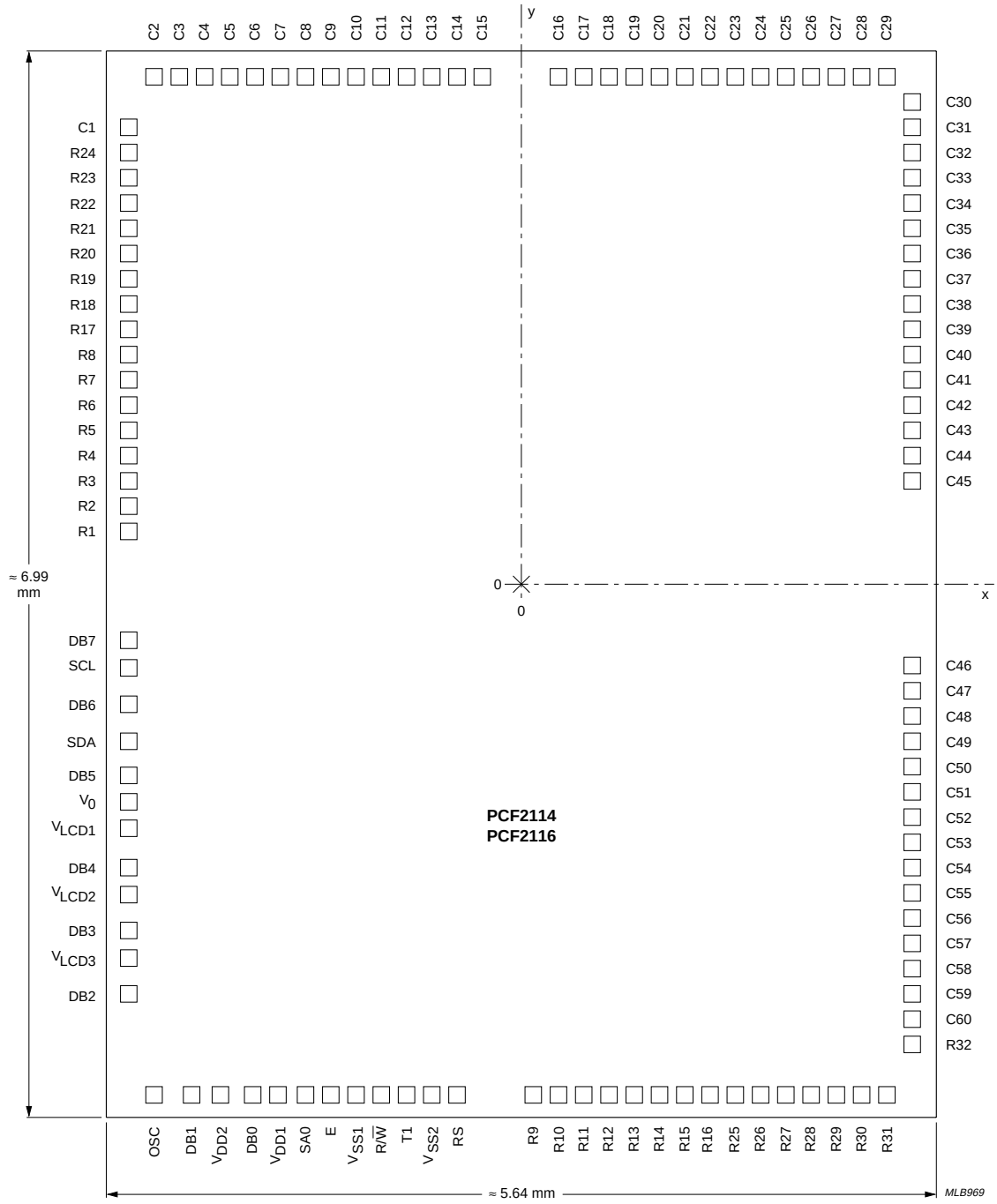


Fig.39 Chip on glass application.

19 BONDING PAD LOCATIONS



Chip dimensions: approximately 5.64 × 6.99 mm.
Pad area: 0.0121 mm^2.
Bonding pad dimensions: 110 × 110 μm.

Fig.40 Bonding pad locations.

Table 11 Bonding pad locations (dimensions in μm)
All x/y coordinates are referenced to centre of chip, see Fig.40.

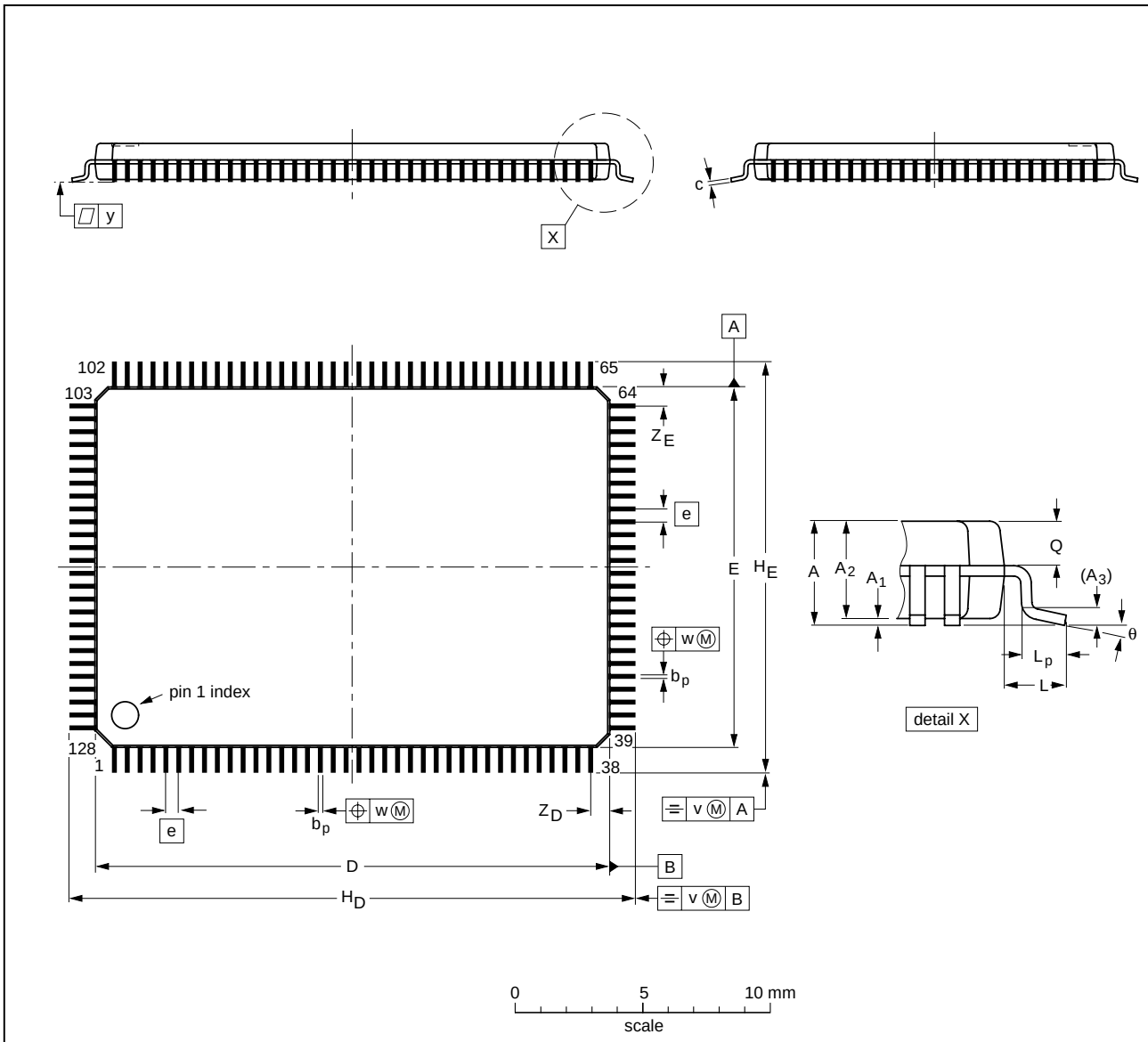
SYMBOL	PAD	x	y
OSC	1	–2445	–3300
DB1	2	–2211	–3300
V_{DD2}	3	–2034	–3300
DB0	4	–1806	–3300
V_{DD1}	5	–1627	–3300
SA0	6	–1437	–3300
E	7	–1245	–3300
V_{SS1}	8	–1056	–3300
R/$\overline{W}$	9	–867	–3300
T1	10	–672	–3300
V_{SS2}	11	–486	–3300
RS	12	–297	–3300
R9	13	77	–3300
R10	14	247	–3300
R11	15	417	–3300
R12	16	587	–3300
R13	17	757	–3300
R14	18	927	–3300
R15	19	1097	–3300
R16	20	1267	–3300
R25	21	1436	–3300
R26	22	1606	–3300
R27	23	1776	–3300
R28	24	1946	–3300
R29	25	2116	–3300
R30	26	2286	–3300
R31	27	2456	–3300
R32	28	2626	–3013
C60	29	2626	–2760
C59	30	2626	–2590
C58	31	2626	–2420
C57	32	2626	–2250
C56	33	2626	–2080
C55	34	2626	–1910
C54	35	2626	–1740
C53	36	2626	–1570
C52	37	2626	–1400
C51	38	2626	–1230

SYMBOL	PAD	x	y
C50	39	2626	–1060
C49	40	2626	–890
C48	41	2626	–720
C47	42	2626	–550
C46	43	2626	–380
C45	44	2626	582
C44	45	2626	752
C43	46	2626	922
C42	47	2626	1092
C41	48	2626	1262
C40	49	2626	1432
C39	50	2626	1602
C38	51	2626	1772
C37	52	2626	1942
C36	53	2626	2112
C35	54	2626	2282
C34	55	2626	2452
C33	56	2626	2622
C32	57	2626	2792
C31	58	2626	2962
C30	59	2626	3132
C29	60	2339	3302
C28	61	2169	3302
C27	62	1999	3302
C26	63	1829	3302
C25	64	1659	3302
C24	65	1489	3302
C23	66	1319	3302
C22	67	1149	3302
C21	68	979	3302
C20	69	809	3302
C19	70	639	3302
C18	71	469	3302
C17	72	299	3302
C16	73	129	3302
C15	74	–245	3302
C14	75	–415	3302
C13	76	–585	3302

SYMBOL	PAD	x	y
C12	77	–755	3302
C11	78	–925	3302
C10	79	–1095	3302
C9	80	–1265	3302
C8	81	–1435	3302
C7	82	–1605	3302
C6	83	–1775	3302
C5	84	–1945	3302
C4	85	–2115	3302
C3	86	–2285	3302
C2	87	–2455	3302
C1	88	–2625	3015
R24	89	–2625	2846
R23	90	–2625	2676
R22	91	–2625	2506
R21	92	–2625	2336
R20	93	–2625	2166
R19	94	–2625	1996
R18	95	–2625	1826
R17	96	–2625	1656
R8	97	–2625	1487
R7	98	–2625	1317
R6	99	–2625	1147
R5	100	–2625	977
R4	101	–2625	807
R3	102	–2625	637
R2	103	–2625	467
R1	104	–2625	297
DB7	105	–2625	–290
SCL	106	–2625	–479
DB6	107	–2625	–716
SDA	108	–2625	–976
DB5	109	–2625	–1202
V_0	110	–2625	–1388
V_{LCD1}	111	–2625	–1580
DB4	112	–2625	–1808
V_{LCD2}	113	–2625	–1985
DB3	114	–2625	–2213
V_{LCD3}	115	–2625	–2390
DB2	116	–2625	–2621

20 PACKAGE OUTLINE

LQFP128: plastic low profile quad flat package; 128 leads; body 14 x 20 x 1.4 mm **SOT425-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	14.1 13.9	0.5	22.15 21.85	16.15 15.85	1.0	0.75 0.45	0.70 0.58	0.2	0.12	0.1	0.81 0.59	0.81 0.59	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT425-1						96-04-02

21 SOLDERING

21.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

21.2 Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

21.3 Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

21.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

22 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

23 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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