DATA SHEET

PCF8533
Universal LCD driver for low multiplex rates

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Philips
Semiconductors

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CONTENTS

Universal LCD driver for low multiplex rates PCF8533

1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 80 segment drives: up to forty 8-segment numeric characters; up to twentyone 15-segment alphanumeric characters; or any graphics of up to 320 elements
- 80 $\times$ 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 1.8 to 5.5 V
- Wide LCD supply range: from 2.5 V for low threshold LCDs and up to 6.5 V for guest-host LCDs and high threshold (automobile) twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- TTL/CMOS compatible
- Compatible with 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 5120 segments possible)
- No external components
- Compatible with Chip-On-Glass (COG) technology
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8533 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 80 segments and can easily be cascaded for larger LCD applications. The PCF8533 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8533U	–	chip with bumps in tray	–

4 BLOCK DIAGRAM

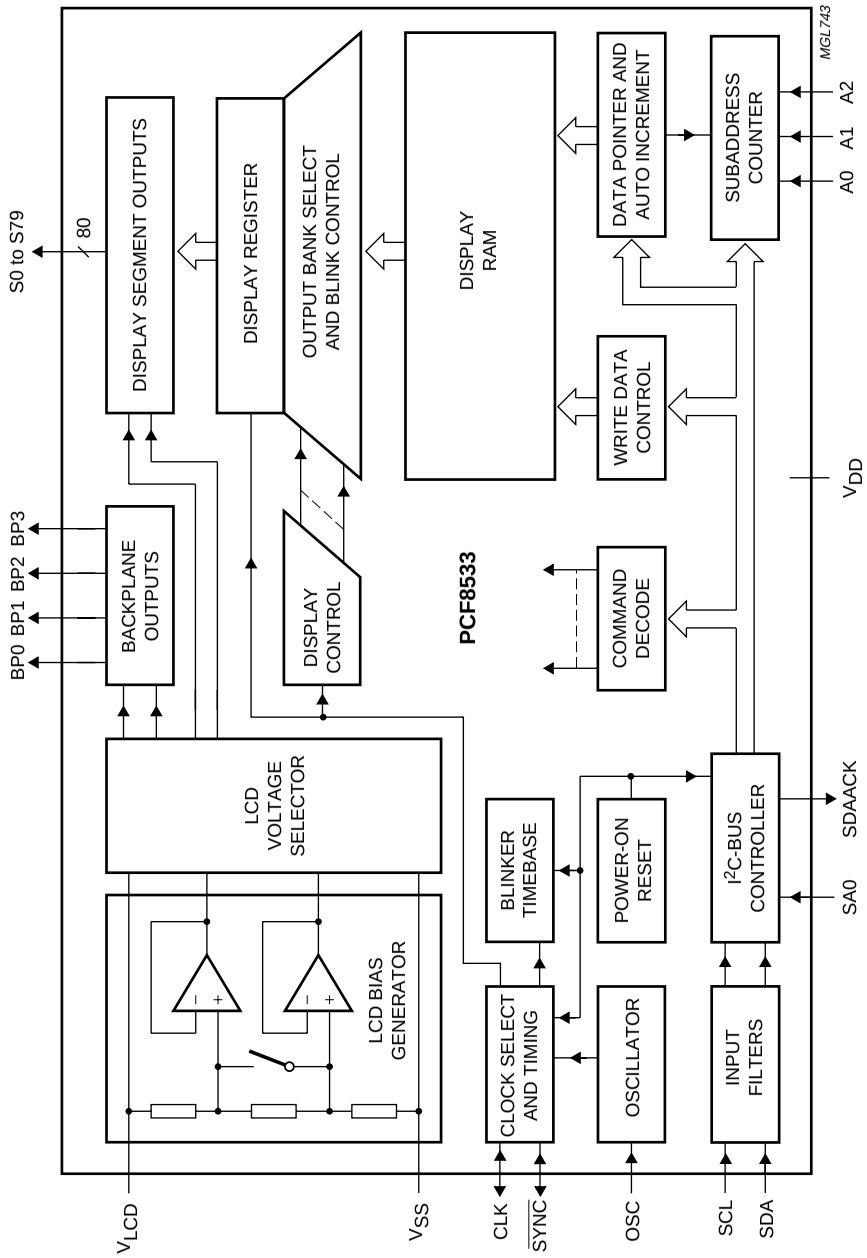


Fig.1 Block diagram.

5 PINNING

SYMBOL	PAD	DESCRIPTION
SDAACK	1	I^2C-bus acknowledge output; note 1
SDA	2 and 3	I^2C-bus serial data input; note 1
SCL	4 and 5	I^2C-bus serial clock input
CLK	6	external clock input/output
V_{DD}	7	supply voltage
$\overline{SYNC}$	8	cascade synchronization input/output
OSC	9	internal oscillator enable input
A0, A1 and A2	10, 11 and 12	subaddress inputs
SA0	13	I^2C-bus slave address input; bit 0
V_{SS}	14	logic ground
V_{LCD}	15	LCD supply voltage
BP0, BP1, BP2 and BP3	17, 99, 16 and 98	LCD backplane outputs
S0 to S79	18 to 97	LCD segment outputs

Note

1. For most applications SDA and SDAACK will be shorted together; see Chapter 7.

6 FUNCTIONAL DESCRIPTION

The PCF8533 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 80 segments. The display configurations possible with the PCF8533 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.2.

The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8533. The internal oscillator is selected by connecting pad OSC to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel selected for the application.

Table 1 Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	320	40	40	20	40	320 dots (4×80)
3	240	30	30	16	16	240 dots (3×80)
2	160	20	20	10	20	160 dots (2×80)
1	80	10	10	5	10	80 dots (1×80)

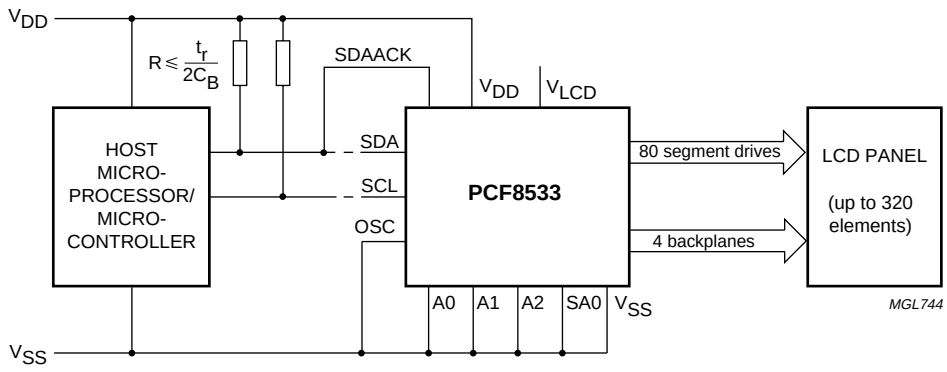


Fig.2 Typical system configuration.

6.1 Power-on reset

At Power-on the PCF8533 resets to a starting condition as follows:

1. All backplane outputs are set to V_{LCD}.
2. All segment outputs are set to V_{LCD}.
3. The drive mode '1 : 4 multiplex with $\frac{1}{3}$bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.
8. Display disabled.

Data transfers on the I^2C-bus should be avoided for 1 ms following Power-on to allow completion of the reset action.

6.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of the circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder.

The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{OP} and the resulting discrimination ratios (D), are given in Table 2.

A practical value for V_{OP} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{OP} > 3V_{th}$.

Multiplex drive ratios of 1 : 3 and 1 : 4 with $\frac{1}{2}$bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3}$ = 1.732 for 1 : 3 multiplex or $\frac{\sqrt{21}}{3}$ = 1.528 for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage V_{OP} as follows:

- 1 : 3 multiplex ($\frac{1}{2}$bias):

  $$V_{OP} = \sqrt{6} \times V_{off(rms)} = 2.449 V_{off(rms)}$$

- 1 : 4 multiplex ($\frac{1}{2}$bias):

  $$V_{OP} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(rms)}$$

These compare with $V_{OP} = 3V_{off(rms)}$ when $\frac{1}{3}$bias is used. Note: $V_{OP} = V_{LCD}$.

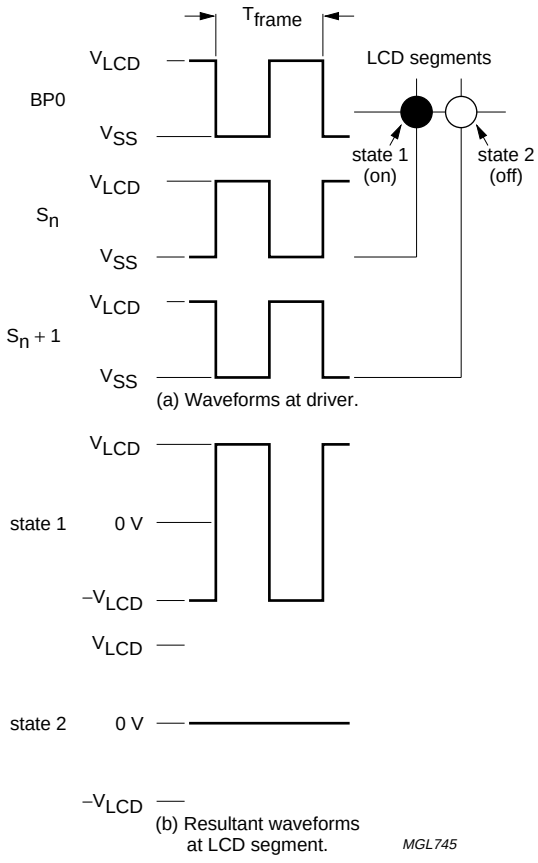
Table 2 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{OP}}$	$\frac{V_{on(rms)}}{V_{OP}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1 : 2	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1 : 3	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1 : 4	4	4	$\frac{1}{3}$	0.333	0.577	1.732

6.4 LCD drive mode waveforms

6.4.1 STATIC DRIVE MODE

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.3.

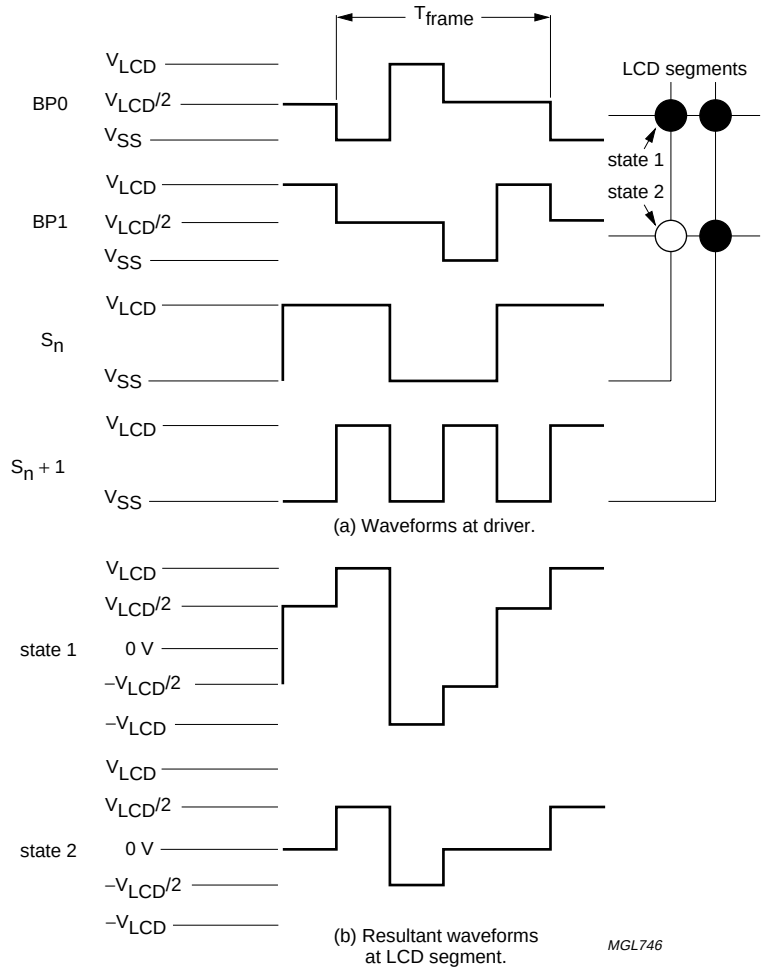


$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.
$V_{on(rms)} = V_{LCD}$.
$V_{state2}(t) = V_{sn+1}(t) - V_{BP0}(t)$.
$V_{off(rms)} = 0$ V.

Fig.3 Static drive mode waveforms.

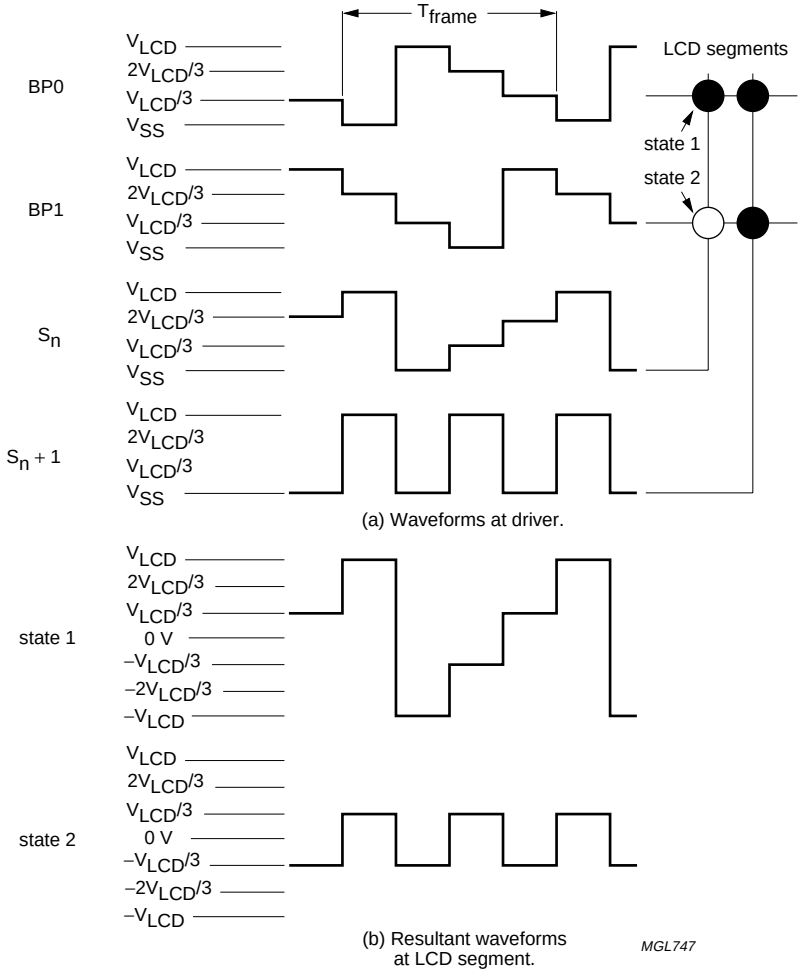
6.4.2 1 : 2 MULTIPLEX DRIVE MODE

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies. The PCF8533 allows the use of $\frac{1}{2}$bias or $\frac{1}{3}$bias in this mode as shown in Figs 4 and 5.



$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.
$V_{on(rms)} = 0.791V_{LCD}$.
$V_{state2}(t) = V_{sn}(t) - V_{BP1}(t)$.
$V_{off(rms)} = 0.354V_{LCD}$.

Fig.4 Waveforms for the 1 : 2 multiplex drive mode with $\frac{1}{2}$bias.

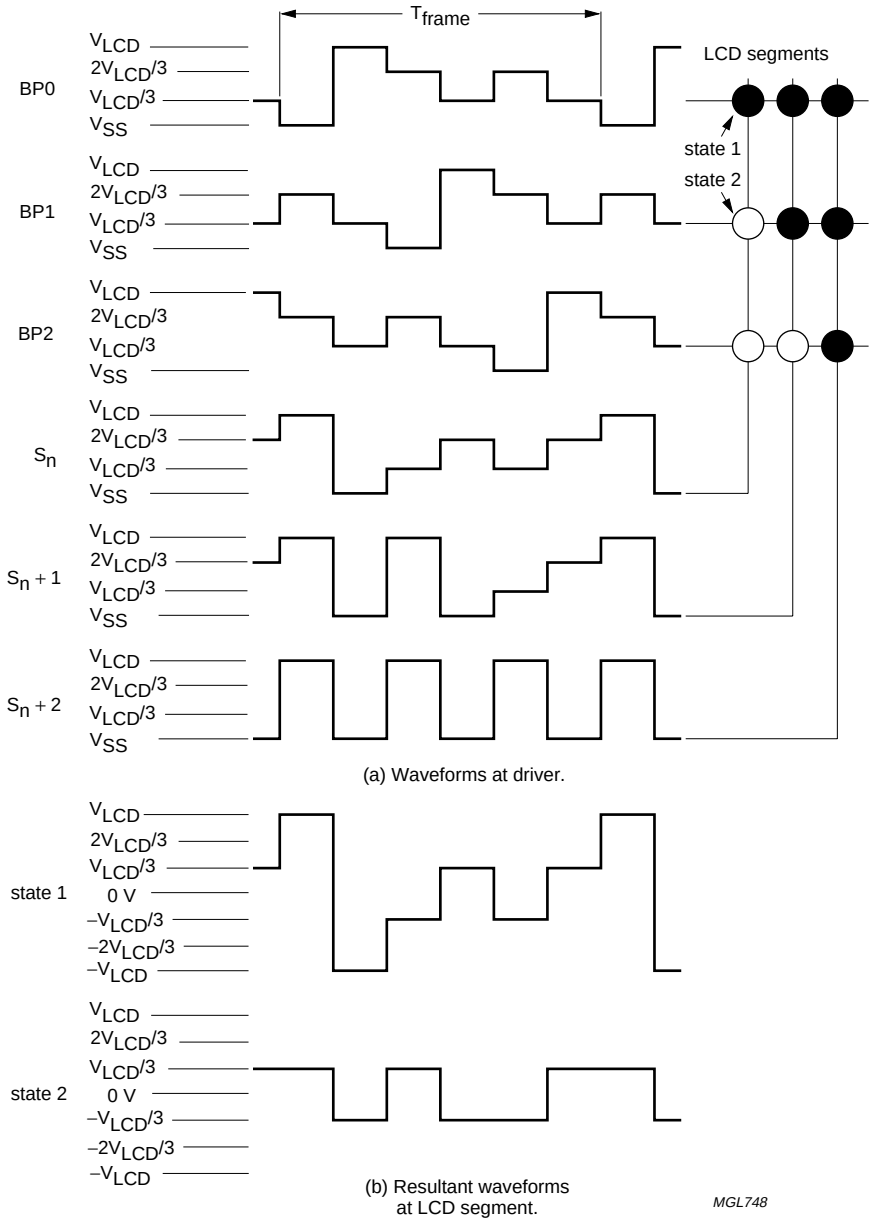


$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.
$V_{on(rms)} = 0.745V_{LCD}$.
$V_{state2}(t) = V_{sn}(t) - V_{BP1}(t)$.
$V_{off(rms)} = 0.333V_{LCD}$.

Fig.5 Waveforms for the 1 : 2 multiplex drive mode with $\frac{1}{3}$bias.

6.4.3 1 : 3 MULTIPLEX DRIVE MODE

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies, as shown in Fig.6.

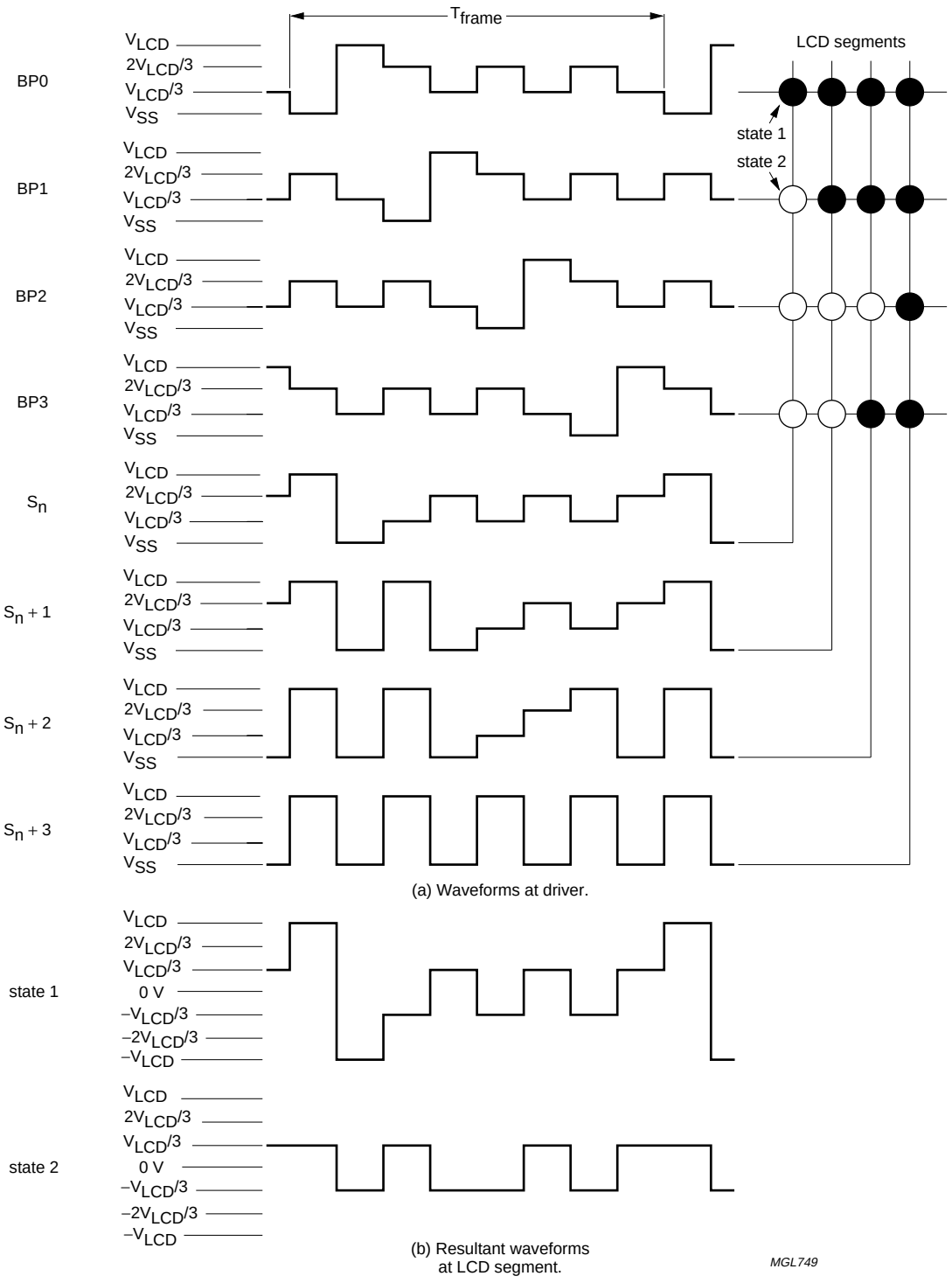


$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$.
$V_{on(rms)} = 0.638V_{LCD}$.
$V_{state2}(t) = V_{sn}(t) - V_{BP1}(t)$.
$V_{off(rms)} = 0.333V_{LCD}$.

Fig.6 Waveforms for the 1 : 3 multiplex drive mode.

6.4.4 1 : 4 MULTIPLEX DRIVE MODE

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies, as shown in Fig.7.



$V_{state1}(t) = V_{sn}(t) - V_{BP0}(t)$: $V_{on(rms)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{sn}(t) - V_{BP1}(t)$: $V_{off(rms)} = 0.333V_{LCD}$.

Fig.7 Waveforms for the 1 : 4 multiplex drive mode.

6.5 Oscillator

6.5.1 INTERNAL CLOCK

The internal logic and the LCD drive signals of the PCF8533 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, pad OSC should be connected to V_{SS}. In this event, the output from pad CLK provides the clock signal for cascaded PCF8533s in the system. After power-up, SDA must be HIGH to guarantee that the clock starts.

6.5.2 EXTERNAL CLOCK

The condition for external clock is made by tying pad OSC to V_{DD}; pad CLK then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The timing of the PCF8533 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between the PCF8533s in the system. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency (see Table 3). The frame frequency is a fixed division of the internal clock or of the frequency applied to pad CLK when an external clock is used.

6.7 Display register

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.8 Segment outputs

The LCD drive section includes 80 segment outputs (S0 to S79) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 80 segment outputs are required the unused segment outputs should be left open-circuit.

6.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.10 Display RAM

The display RAM is a static 80×4-bit RAM which stores LCD data. A logic 1 in the RAM bit map indicates the on-state of the corresponding LCD segment; similarly, a logic 0 indicates the off-state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 80 segments operated with respect to backplane BP0 (see Fig.8). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8533 the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current mux mode data is stored singularly, in pairs, triplets or quadruplets. e.g. in 1 : 2 mux mode the RAM data is stored every second bit. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.9; the RAM filling organization depicted applies equally to other LCD types. With reference to Fig.9, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses.

In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Table 3 LCD frame frequencies

FRAME FREQUENCY	NOMINAL FRAME FREQUENCY (Hz)
$\frac{f_{CLK}}{24}$	64

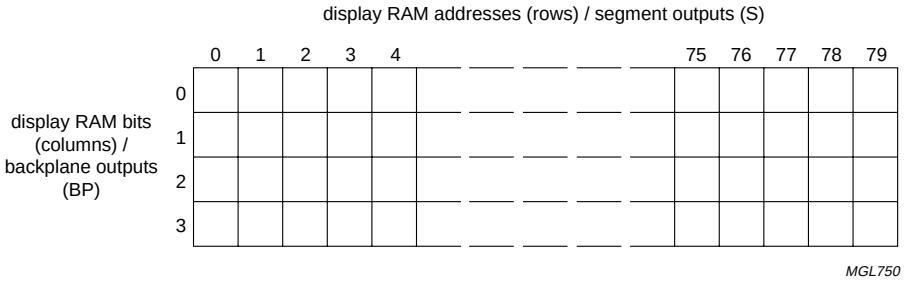


Fig.8 Display RAM bit map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

6.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.9. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode). If an I^2C-bus data access is terminated early then the state of the data pointer will be unknown. The data pointer should be re-written prior to further RAM accesses.

6.12 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place.
The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8533 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 27th display data byte transmitted in 1 : 3 multiplex mode).

The hardware subaddress should not be changed whilst the device is being accessed on the I^2C-bus interface.

6.13 Output bank selector

The output bank selector selects one of the four bits per display RAM address for transfer to the display latch. The actual bit selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

In 1 : 4 multiplex, all RAM addresses of bit 0 are selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected.
The $\overline{SYNC}$ signal will reset these sequences to the following starting points; bit 3 for 1 : 4 multiplex, bit 2 for 1 : 3 multiplex, bit 1 for 1 : 2 multiplex and bit 0 for static mode.

The PCF8533 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using

the BANK SELECT command. The input bank selector functions independently to the output bank selector.

6.15 Blinker

The display blinking capabilities of the PCF8533 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency. The ratios between the clock and blinking frequencies depend on the mode in which the device is operating, see Table 4.

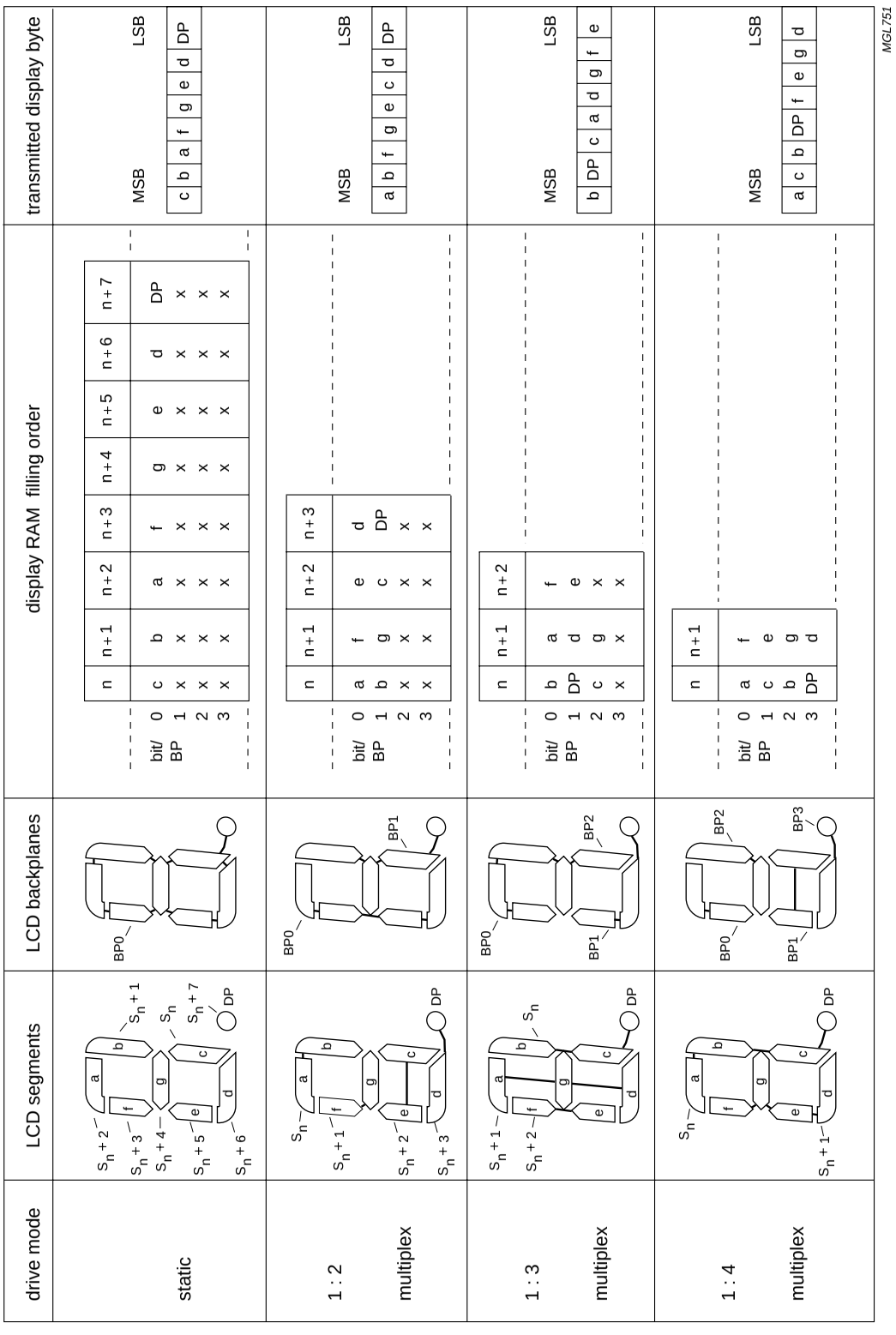
An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	NOMINAL BLINKING FREQUENCY
Off	–	blinking off
2 Hz	$\frac{f_{CLK}}{768}$	2 Hz
1 Hz	$\frac{f_{CLK}}{1536}$	1 Hz
0.5 Hz	$\frac{f_{CLK}}{3072}$	0.5 Hz



X = data bit unchanged.

Fig.9 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus.

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

By connecting SDAACK to SDA on the PCF8533, the SDA line becomes fully I²C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAACK pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the PCF8533 will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAACK pad to the system SDA line to guarantee a valid low level.

The following definition assumes SDA and SDAACK are connected and refers to the pair as SDA.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.10.

7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.11.

7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’. The system configuration is illustrated in Fig.12.

7.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C-bus is illustrated in Fig.13.

7.5 PCF8533 I²C-bus controller

The PCF8533 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8533 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (01110000 and 01110010) are reserved for the PCF8533. The least significant bit of the slave address that a PCF8533 will respond to is defined by the level tied at its input SA0. The PCF8533 is a write only device and will not respond to a read access. Therefore, two types of PCF8533 can be distinguished on the same I²C-bus which allows:

1. Up to 16 PCF8533s on the same I²C-bus for very large LCD applications
2. The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.14. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8533 slave addresses available. All PCF8533s with the corresponding SA0 level acknowledge in parallel to the slave address, but all PCF8533s with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, a control byte follows which defines if the next byte is RAM or command information. The control byte also defines if the next following byte is a control byte or further RAM/command data.

In this way it is possible to configure the device then fill the display RAM with little overhead.

The command bytes and control bytes are also acknowledged by all addressed PCF8533s connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8533 device.

The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8533. After the last display byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART an I²C-bus access.

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The five commands available to the PCF8533 are defined in Table 5.

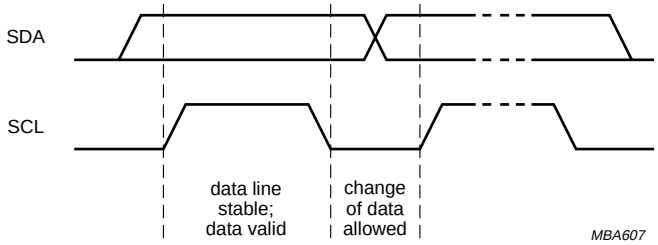


Fig.10 Bit transfer.

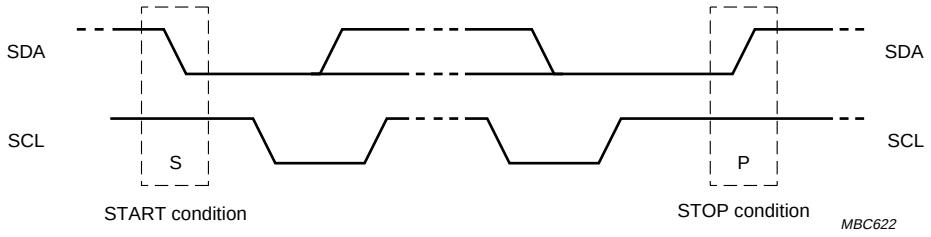


Fig.11 Definition of START and STOP conditions.

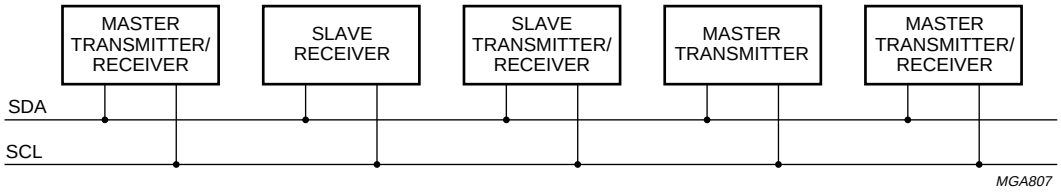


Fig.12 System configuration.

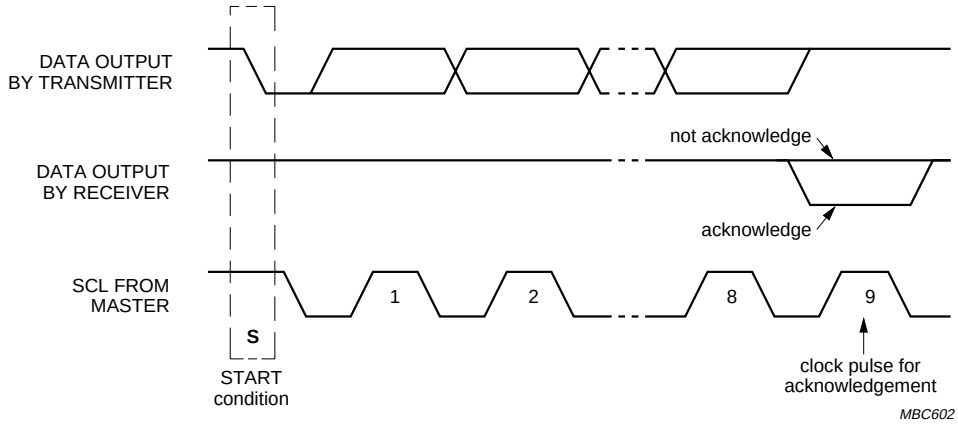


Fig.13 Acknowledgement on the I^2C-bus.

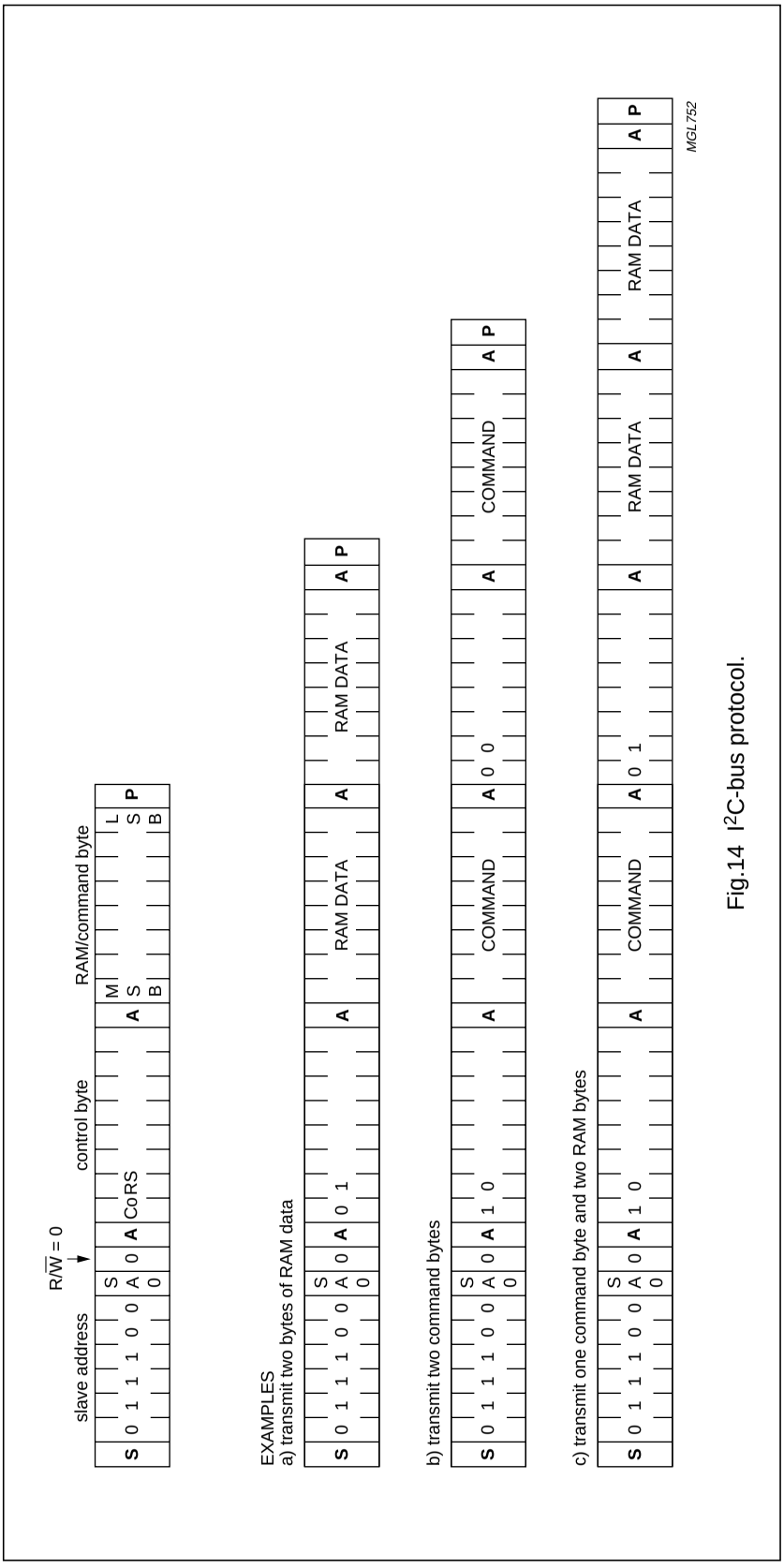


Fig.14 I²C-bus protocol.

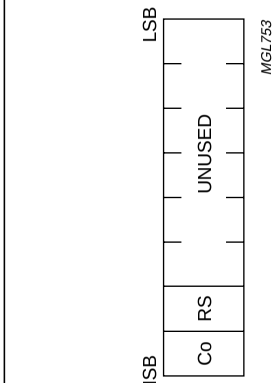


Fig.15 Format of control byte.

Co = 0; last control byte.
Co = 1; control bytes continue.
RS = 0; data is a command byte
RS = 1; data is a display byte

Table 5 Definition of PCF8533 commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
MODE SET	1	1	0	0	E	B	M1	M0	Table 6	defines LCD drive mode
									Table 7	defines LCD bias configuration
									Table 8	defines display status; the possibility to disable the display allows implementation of blinking under external control
LOAD DATA POINTER	0	P6	P5	P4	P3	P2	P1	P0	Table 9	seven bits of immediate data, bits P6 to P0, are transferred to the data pointer to define one of eighty display RAM addresses
DEVICE SELECT	1	1	1	0	0	A2	A1	A0	Table 10	three bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of eight hardware subaddresses
BANK SELECT	1	1	1	1	1	0	I	O	Table 11	defines input bank selection (storage of arriving display data)
									Table 12	defines output bank selection (retrieval of LCD display data); the BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK	1	1	1	1	0	A	BF 1	BF 0	Table 13	defines the blinking frequency
									Table 14	selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Table 6 Mode set option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	**BACKPLANE**	**M1**	**M0**
Static	1 BP	0	1
1 : 2	MUX (2 BP)	1	0
1 : 3	MUX (3 BP)	1	1
1 : 4	MUX (4 BP)	0	0

Table 7 Mode set option 2

LCD BIAS	BIT B
$\frac{1}{3}$bias	0
$\frac{1}{2}$bias	1

Table 8 Mode set option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 Load data pointer option 1

DESCRIPTION	BITS						
7 bit binary value of 0 to 79	P6	P5	P4	P3	P2	P1	P0

Table 10 Device select option 1

DESCRIPTION	BITS		
3 bit binary value of 0 to 7	A2	A1	A0

Table 11 Bank select option 1 (Input)

STATIC	1 : 2 MUX	BIT I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 12 Bank select option 2 (Output)

STATIC	1 : 2 MUX	BIT O
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13 Blink option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 14 Blink option 2

BLINK MODE	BIT A
Normal blinking(1)	0
Alternation blinking	1

Note

1. Normal blinking is assumed when multiplex rates 1 : 3 or 1 : 4 are selected.

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8533 and co-ordinates their effects.
The controller is also responsible for loading display data into the display RAM as required by the filling order.

7.10 Cascaded operation

In large display configurations, up to 16 PCF8533s can be distinguished on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0). When cascaded PCF8533s are synchronized they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8533s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Fig.16).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8533s. This synchronization is guaranteed after the Power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments, or by the definition of a multiplex mode when PCF8533s with different SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pad; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8533 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8533 to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8533 are shown in Fig.17.

The contact resistance between the $\overline{\text{SYNC}}$ pads of cascaded devices must be controlled. If the resistance is too high then the device will not be able to synchronize properly. This is particularly applicable to COG applications. Table 15 shows the limiting values for contact resistance.

Table 15 $\overline{\text{SYNC}}$ contact resistance

NUMBER OF DEVICES	MAXIMUM CONTACT RESISTANCE
2	6000 Ω
3 to 5	2200 Ω
6 to 10	1200 Ω
11 to 16	700 Ω

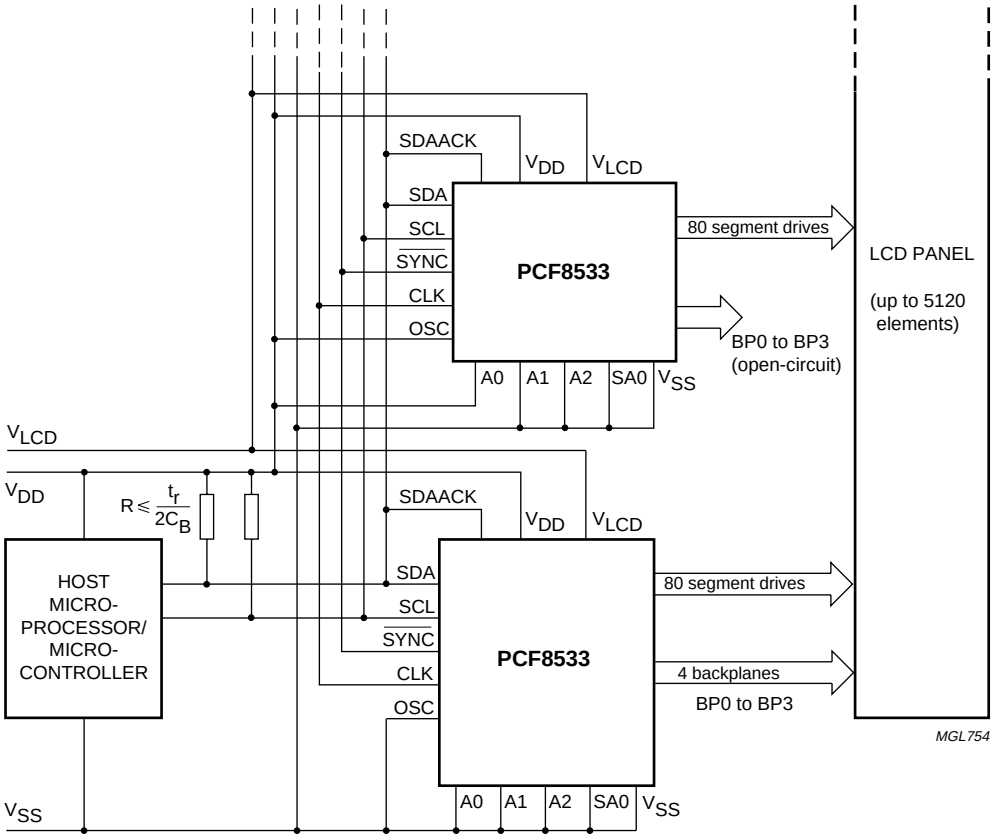


Fig.16 Cascaded PCF8533 configuration.

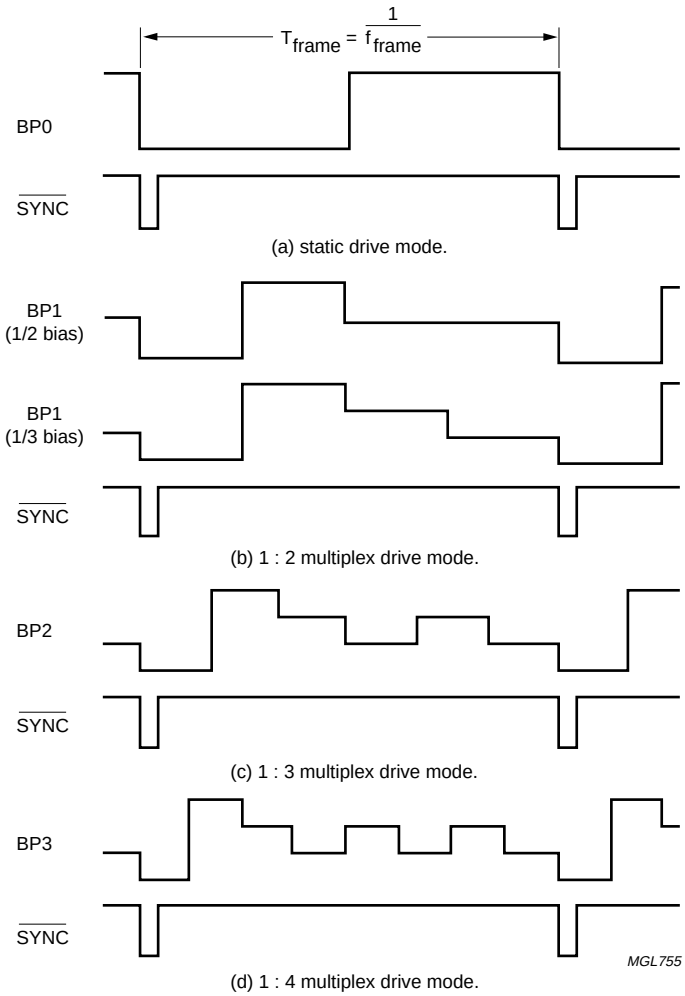


Fig.17 Synchronization of the cascade for the various PCF8533 drive modes.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
I_{DD}	supply current	–50	+50	mA
V_{LCD}	LCD supply voltage	V_{SS} – 0.5	+7.5	V
I_{LCD}	LCD supply current	–50	+50	mA
I_{SS}	negative supply current	–50	+50	mA
$V_{I(n)}$	input voltage on pads SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC and A0 to A2	V_{SS} – 0.5	V_{DD} + 0.5	V
$V_{O(n)}$	output voltage on pads S0 to S79 and BP0 to BP3	V_{SS} – 0.5	V_{LCD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation	–	400	mW
P/out	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS Devices”*).

10 DC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 to 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	5.5	V
V_{LCD}	LCD supply voltage		2.5	–	6.5	V
I_{DD}	supply current	f_{CLK} = 1536 Hz; note 1	–	8	20	µA
I_{LCD}	LCD supply current	f_{CLK} = 1536 Hz; note 1	–	24	60	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{OL1}	LOW-level output current on pads CLK and $\overline{SYNC}$	V_{OL} = 0.4 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH-level output current pad CLK	V_{OH} = 4.6 V; V_{DD} = 5 V	–1	–	–	mA
I_{OL2}	LOW-level output current pad SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current on pads SA0, A0 to A2, CLK, SDA and SCL	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	µA
I_{L2}	leakage current pad OSC	$V_I = V_{DD}$	–1	–	+1	µA
V_{POR}	Power-on reset voltage level		1.0	1.3	1.6	V
C_I	input capacitance	note 2	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component on pads BP0 to BP3	C_{BP} = 35 nF	–100	–	+100	mV
V_S	DC voltage component on pads S0 to S79	C_S = 5 nF	–100	–	+100	mV
R_{BP}	output resistance at pads BP0 to BP3	V_{LCD} = 5 V; note 3	–	1.5	10	kΩ
R_S	output resistance at pads S0 to S79	V_{LCD} = 5 V; note 3	–	6.0	13.5	kΩ

Notes

1. LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
2. Not tested; given by design.
3. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 to 6.5 V; T_{amb} = –40 to + 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{CLK}	oscillator frequency at pad CLK	V_{DD} = 5 V; note 1	797	1536	3046	Hz
t_{CLKH}	input CLK HIGH time		130	–	–	µs
t_{CLKL}	input CLK LOW time		130	–	–	µs
$t_{d(p)SYNC}$	$\overline{SYNC}$ propagation delay time		–	30	–	ns
t_{SYNCL}	$\overline{SYNC}$ LOW time		1	–	–	µs
$t_{d(PLCD)}$	driver delays with test loads	V_{LCD} = 5 V	–	–	30	µs
Timing characteristics: I²C-bus; note 2						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{BUF}	bus free time between a STOP and START		1.3	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time		–	–	0.3	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_b	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Notes

1. Typical output duty cycle of 50%.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

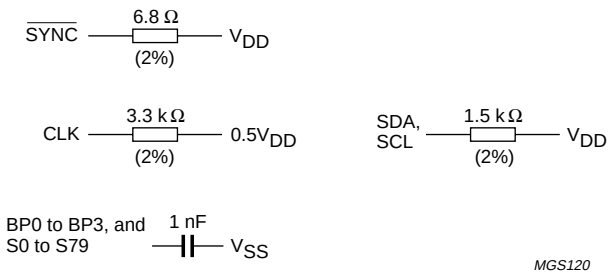


Fig.18 Test loads.

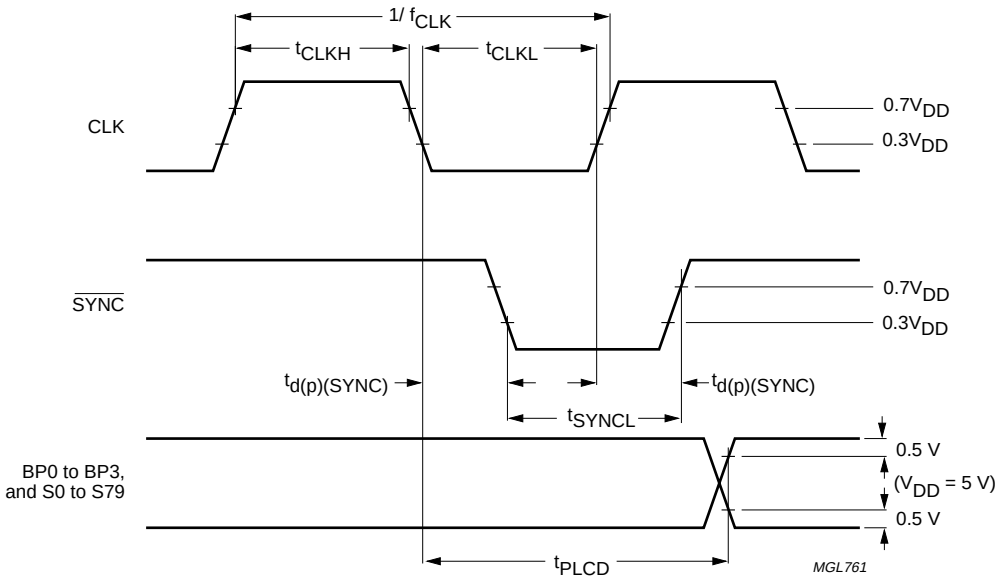


Fig.19 Driver timing waveforms.

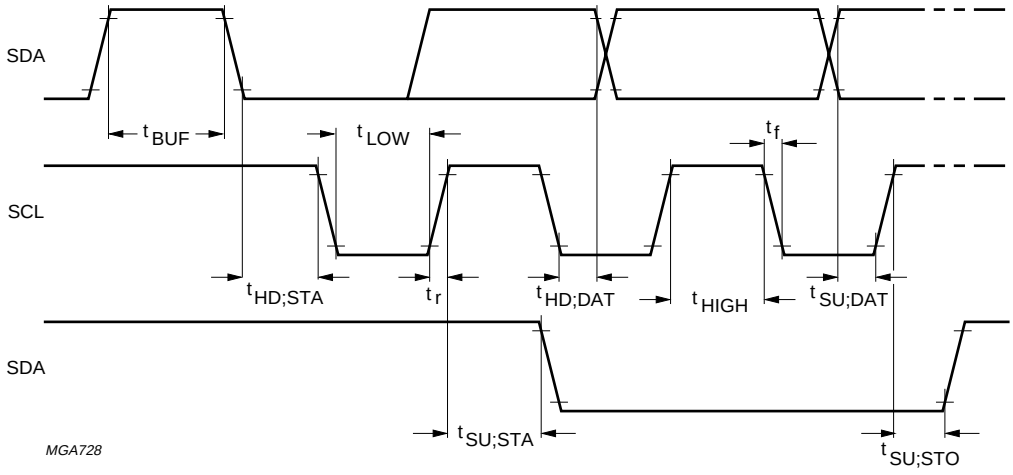


Fig.20 I²C-bus timing waveforms.

12 BONDING PAD LOCATIONS

Bonding pad locations (dimensions in μm)

All x and y coordinates are referenced to centre of chip (see Fig.22).

SYMBOL	PAD	x	y
SDAACK	1	−1079.20	−594.40
SDA	2	−839.20	−594.40
SDA	3	−759.20	−594.40
SCL	4	−599.20	−594.40
SCL	5	−519.20	−594.40
CLK	6	−414.80	−594.40
V_{DD}	7	−284.80	−594.40
$\overline{SYNC}$	8	+4.20	−594.40
OSC	9	+119.20	−594.40
A0	10	+249.20	−594.40
A1	11	+379.20	−594.40
A2	12	+581.20	−594.40
SA0	13	+711.20	−594.40
V_{SS}	14	+841.20	−594.40
V_{LCD}	15	+1099.60	−594.40
BP2	16	+1277.60	−594.40
BP0	17	+1357.60	−594.40
S0	18	+1437.60	−594.40
S1	19	+1517.60	−594.40
S2	20	+1597.60	−594.40
S3	21	+1677.60	−594.40
S4	22	+1757.60	−594.40
S5	23	+1837.60	−594.40
S6	24	+1917.60	−594.40
S7	25	+1997.60	−594.40
S8	26	+2077.60	−594.40
S9	27	+2157.60	−594.40
S10	28	+2237.60	−594.40
S11	29	+2317.60	−594.40
S12	30	+2357.60	+594.40
S13	31	+2277.60	+594.40
S14	32	+2197.60	+594.40
S15	33	+2117.60	+594.40
S16	34	+2037.60	+594.40
S17	35	+1957.60	+594.40
S18	36	+1877.60	+594.40
S19	37	+1797.60	+594.40

SYMBOL	PAD	x	y
S20	38	+1717.60	+594.40
S21	39	+1637.60	+594.40
S22	40	+1557.60	+594.40
S23	41	+1477.60	+594.40
S24	42	+1317.60	+594.40
S25	43	+1237.60	+594.40
S26	44	+1157.60	+594.40
S27	45	+1077.60	+594.40
S28	46	+997.60	+594.40
S29	47	+917.60	+594.40
S30	48	+837.60	+594.40
S31	49	+757.60	+594.40
S32	50	+677.60	+594.40
S33	51	+597.60	+594.40
S34	52	+437.60	+594.40
S35	53	+357.60	+594.40
S36	54	+277.60	+594.40
S37	55	+197.60	+594.40
S38	56	+117.60	+594.40
S39	57	+37.60	+594.40
S40	58	−42.40	+594.40
S41	59	−122.40	+594.40
S42	60	−202.40	+594.40
S43	61	−282.40	+594.40
S44	62	−362.40	+594.40
S45	63	−442.40	+594.40
S46	64	−602.40	+594.40
S47	65	−682.40	+594.40
S48	66	−762.40	+594.40
S49	67	−842.40	+594.40
S50	68	−922.40	+594.40
S51	69	−1002.40	+594.40
S52	70	−1082.40	+594.40
S53	71	−1162.40	+594.40
S54	72	−1242.40	+594.40
S55	73	−1322.40	+594.40
S56	74	−1402.40	+594.40

SYMBOL	PAD	x	y
S57	75	–1562.40	+594.40
S58	76	–1642.40	+594.40
S59	77	–1722.40	+594.40
S60	78	–1802.40	+594.40
S61	79	–1882.40	+594.40
S62	80	–1962.40	+594.40
S63	81	–2042.40	+594.40
S64	82	–2122.40	+594.40
S65	83	–2202.40	+594.40
S66	84	–2282.40	+594.40
S67	85	–2362.40	+594.40
S68	86	–2322.40	–594.40
S69	87	–2242.40	–594.40
S70	88	–2162.40	–594.40
S71	89	–2082.40	–594.40
S72	90	–2002.40	–594.40
S73	91	–1922.40	–594.40
S74	92	–1842.40	–594.40
S75	93	–1762.40	–594.40
S76	94	–1682.40	–594.40
S77	95	–1602.40	–594.40
S78	96	–1522.40	–594.40
S79	97	–1442.40	–594.40
BP3	98	–1362.40	–594.40
BP1	99	–1282.40	–594.40
Alignment marks			
C1	–	+2300.5	+55.0
C2	–	–2320.2	+107.0
F	–	–2208.3	–165.4
Dummy pads (connected to segments shown; note			
D1	(S11)	+2469.70	–594.40
D2	(S11)	+2549.70	–594.40
D3	(S12)	+2517.60	+594.40
D4	(S12)	+2437.60	+594.40
D5	(S67)	–2442.30	+594.40
D6	(S67)	–2522.30	+594.40
D7	(S68)	–2554.40	–594.40
D8	(S68)	–2474.40	–594.40
Chip corners (pre-sawing)			
Bottom left	–	–2695.00	–750.00
Top right	–	+2695.00	+750.00

Note

1. The dummy pads are not tested.

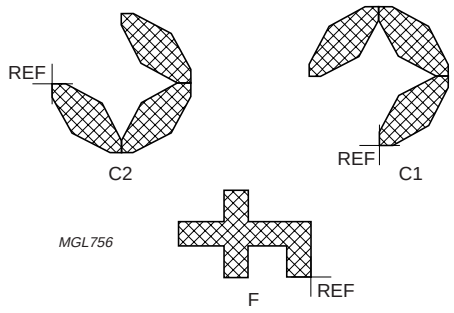


Fig.21 Alignment markers.

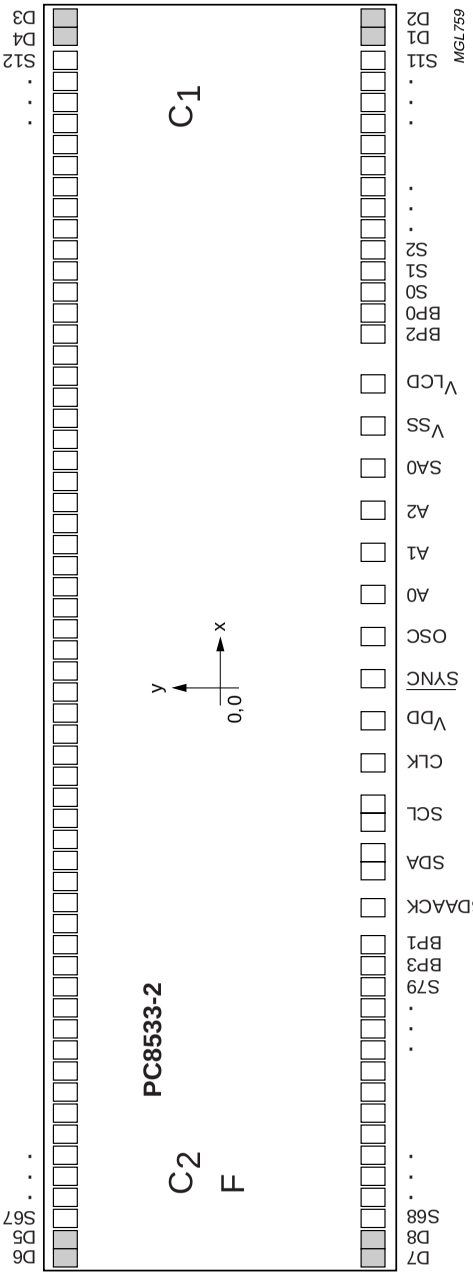


Fig.22 Bonding pad locations.

The position of the bonding pads is not to scale.
Chip dimensions: approximately 5.40 × 1.51 mm.
Bump dimensions: 90 × 50 × 17.5 µm.
Wafer thickness: 381 µm.

13 DEVICE PROTECTION

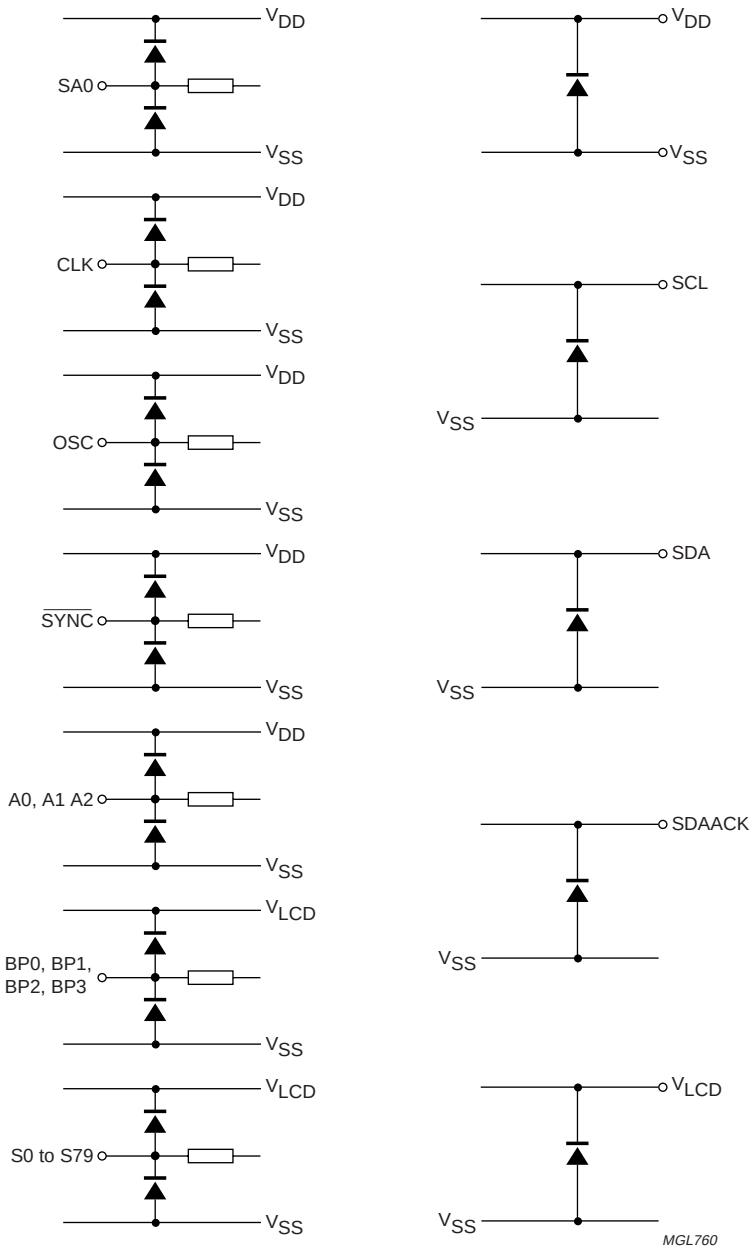
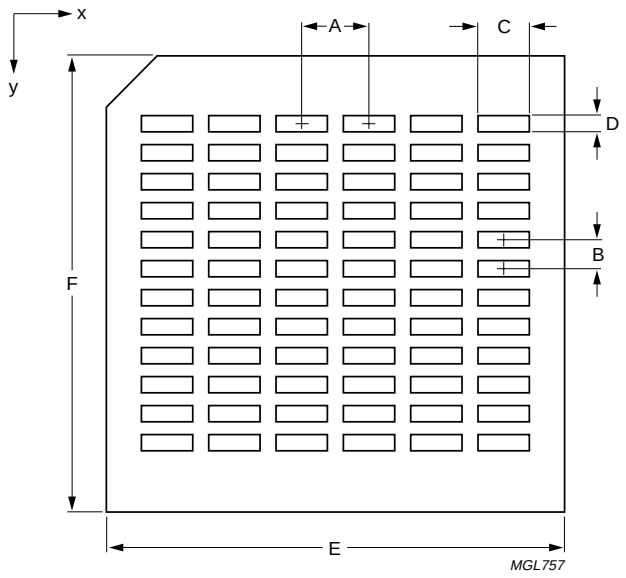


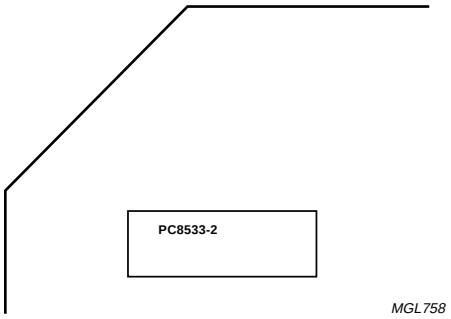
Fig.23 Device protection diagram.

14 TRAY INFORMATION



The dimensions are given in Table 16.

Fig.24 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.25 Tray alignment.

Table 16 Dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch, x direction	7.37 mm
B	pocket pitch, y direction	3.68 mm
C	pocket width, x direction	5.50 mm
D	pocket width, y direction	1.60 mm
E	tray width, x direction	50.8 mm
F	tray width, y direction	50.8 mm
x	no. pockets in x direction	6
y	no. pockets in y direction	12

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

17 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

18 BARE DIE DISCLAIMER

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