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PCM1712U

ADVANCED INFORMATION
SUBJECT TO CHANGE

Dual Voltage Output CMOS Delta-Sigma 16-Bit DIGITAL-TO-ANALOG CONVERTER With On-Chip Digital Filter

FEATURES

- DUAL MULTI-LEVEL NOISE SHAPING DAC WITH ON-CHIP DIGITAL FILTER
- HIGH PERFORMANCE:
THD+N: 0.0045% (-87dB) typ
Dynamic Range: 91dB typ
S/N RATIO: 106dB typ
- ANALOG VOLTAGE OUTPUT:
 $V_o = 3.10V_{p-p}$
- ON-CHIP ANALOG LOW PASS FILTER
- JITTER TOUGH AND LOW RADIO-FREQUENCY INTERFERENCE ENERGY ARCHITECTURE
- SYSTEM CLOCK 384fs
- ON-CHIP 8X OVERSAMPLING DIGITAL FILTER WITH MULTI FUNCTIONS:
Double Speed Dubbing Mode
Soft Mute and Attenuator
Digital De-Emphasis
- SINGLE +5V POWER SUPPLY OPERATION
- SMALL 28-PIN SOIC PACKAGE

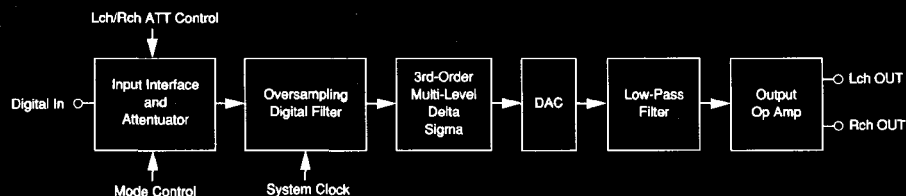
DESCRIPTION

The PCM1712 is a low cost, dual voltage output CMOS digital-to-analog converter. Incorporated into the PCM1712 is a unique multi-level 3rd-order Delta-Sigma architecture that eliminates influence from input clock jitter and RF interference resulting in truly superior performance.

The PCM1712 will accept 16-bit input data as well as normal/IIS (32BCK/fs, continuous 16-bit data) format data.

The on-chip digital filter of the PCM1712 has -35dB stop band attenuation and ± 0.17 dB ripple in the pass band.

The PCM1712 can be used in a wide variety of consumer audio applications. Its low cost, small size, and single +5V operation make it ideal for portable, automotive, CD players, BS tuners, music instruments, games, and other digital audio applications.



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SPECIFICATIONS

ELECTRICAL

All specifications at +25°C, +V_{cc} = +V_{oo} = +5V, f_s = 44.1kHz, and 16-bit data, SYSCLK = 384fs, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1712U			UNITS
		MIN	TYP	MAX	
RESOLUTION			16		Bits
DIGITAL INPUT/OUTPUT					
Logic Family					
Input Logic Level (except XTI)		2.0		0.8	VDC
V _{ih}					VDC
V _{il}					
Input Logic Current (except XTI)				200	μA
I _i					
Input Logic Level (XTI)		3.2		1.4	VDC
V _{ih}					VDC
V _{il}					
Input Logic Current (XTI)				±50	μA
I _i					
Output Logic Level (CLKO):		4.5			VDC
V _{oh}					VDC
V _{ol}				0.2	VDC
Output Logic Current					mA
I _o					
Data Format		±10 Normal/1's (see Timing) SELECTABLE			
Data Bit		16-Bit/MSB First, Two's Complements			
Sampling Frequency		32	44.1	48	kHz
System Clock Frequency	384fs	12.288	16.934	18.432	MHz
DC ACCURACY					
Gain Error			±5.0		% of FSR
Gain Mis-Match Channel-To-Channel			±5.0		% of FSR
Bipolar Zero Error	V _o = 1/2V _{cc} at Bipolar Zero		±20		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Gain Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE⁽¹⁾					
THD+N at F/S (0dB)	f _m = 991Hz		-87		dB
THD+N at -60dB	f _m = 991kHz		-31		dB
Dynamic Range	EIAJ A-weighted		91		dB
S/N Ratio	EIAJ A-weighted		106		dB
Channel Separation	f _m = 991Hz		90		dB
DIGITAL FILTER PERFORMANCE					
Pass Band Ripple ⁽¹⁾	Normal Mode		±0.17		dB
Pass Band Ripple ⁽²⁾	Double Speed Mode		±0.23		dB
Stop Band Attenuation ⁽¹⁾	Normal Mode		-36		dB
Stop Band Attenuation ⁽²⁾	Double Speed Mode		-35		dB
Pass Band ⁽¹⁾	Normal Mode		0.4535		fs
Pass Band ⁽²⁾	Double Speed Mode		0.4535		fs
Stop Band ⁽¹⁾	Normal Mode		0.5485		fs
Stop Band ⁽²⁾	Double Speed Mode		0.5485		fs
De-emphasis Error	(f _s 32kHz ~ 48kHz)	-0.2		+0.55	dB
ANALOG OUTPUT					
Voltage Range	F/S(0dB)OUT		3.10		Vp-p
Load Impedance		5K			Ω
Center Voltage			+1/2V _{cc}		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: +V _{cc}		+4.5	+5.0	+5.5	VDC
+V _{oo}		+4.5	+5.0	+5.5	VDC
Supply Current +V _{cc} +I _{oo}	+V _{cc} = +V _{oo} = +5.0V		45		mA
Power Dissipation	+V _{cc} = +V _{oo} = +5.0V		225		mW
TEMPERATURE RANGE					
Operation		-25		+85	°C
Storage		-55		+100	°C

NOTE: (1) Meter 400Hz HPF, 30kHz LPF On, Average Mode. (2)??

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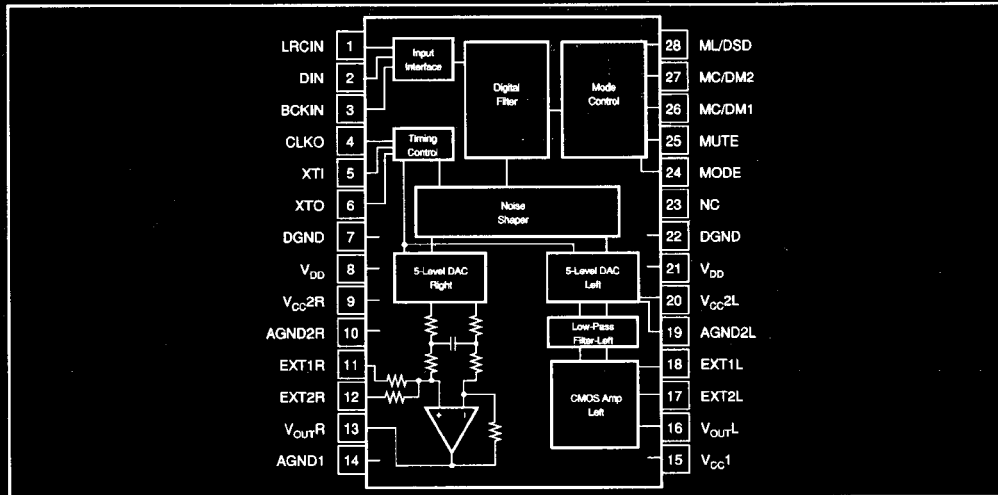
PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	LRCIN	Sample Rate Clock Input (fs)
2	DIN	Data Input
3	BCKIN	Bit Clock Input
4	CLKO	Buffered Output of Oscillator
5	XTI	Oscillator Input (External Clock Input)
6	XTO	Oscillator Output
7	DGND	Digital Ground
8	V _{DD}	Digital Power Supply (+5V)
9	V _{CC2R}	Analog (DAC) +V _{CC} , Rch
10	AGND2R	Analog (DAC) Ground, Rch
11	EXT1R	Output Amp Common, Rch
12	EXT2R	Output Amp Bias, Rch
13	V _{OUTR}	Rch Analog Output
14	AGND	Analog Ground

PIN	NAME	FUNCTION
15	V _{CC}	Analog Power Supply (+5V)
16	V _{OUTL}	Lch Analog Output
17	EXT2L	Output Amp Bias, Lch
18	EXT1L	Output Amp Common, Lch
19	AGND2L	Analog (DAC) Ground, Lch
20	V _{CC2L}	Analog (DAC) +V _{CC} , Lch
21	V _{DD}	Digital Power Supply, (+5V)
22	DGND	Digital Ground
23	NC	No Connection
24	MODE	Operation Mode Select, (H: Serial, L: Parallel)
25	MUTE	Mute Control (H:OFF, L:ON)
26	MD/DM1	Mode Control, Data/De-emphasis selection
27	MC/DM2	Mode Control, BCK/De-emphasis selection
28	ML/DSD	Mode Control, WDCK/Double speed selection

NOTE: (1) XTO (Pin 6) must be open when the external clock enter to XTI (Pin 5). (2) All input pins require pull up resistors.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6.5VDC
+V _{CC} to V _{DD} Voltage	±0.1V
Input Logic Voltage	-0.3V-V _{DD} +0.3V
Power Dissipation	400mW
Operating Temperature Range	-25°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C

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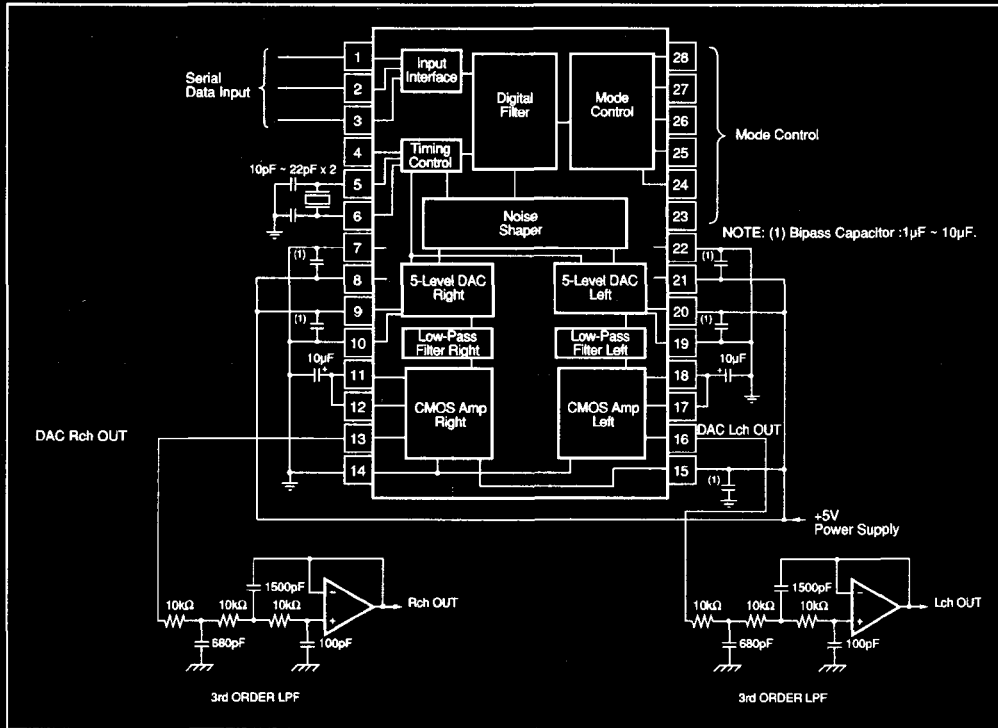
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CONNECTION DIAGRAM



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DATA INPUT TIMING

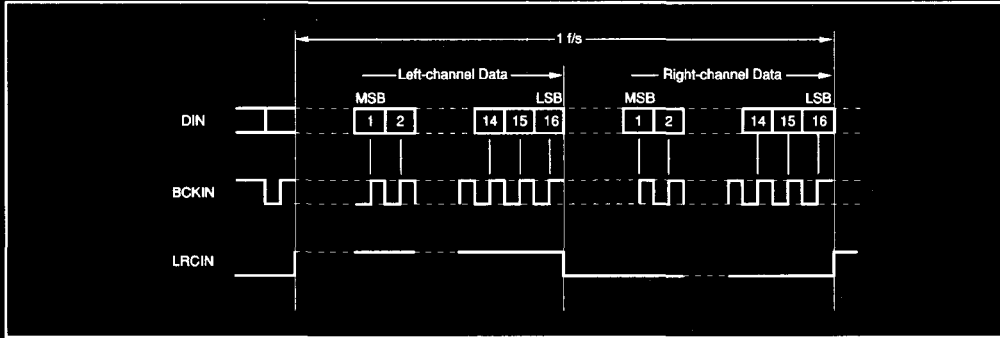


FIGURE 1. Normal Format, 16-Bit (LRCIN H: Lch).

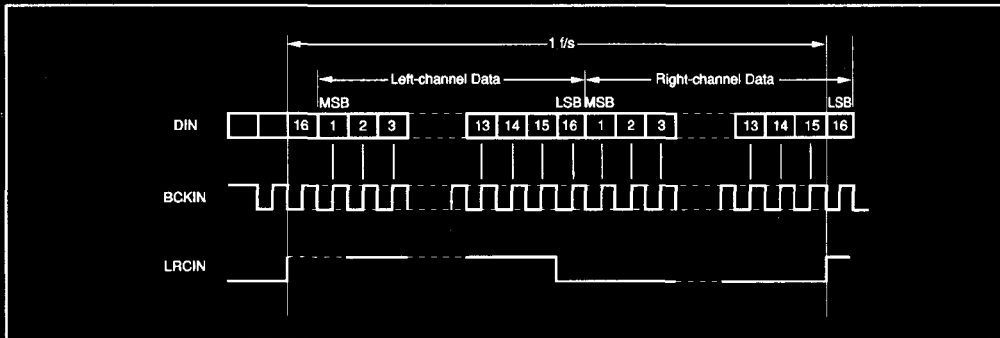


FIGURE 2 . IIS Format, 16-Bit (32 BCKIN/fs, continuous data).

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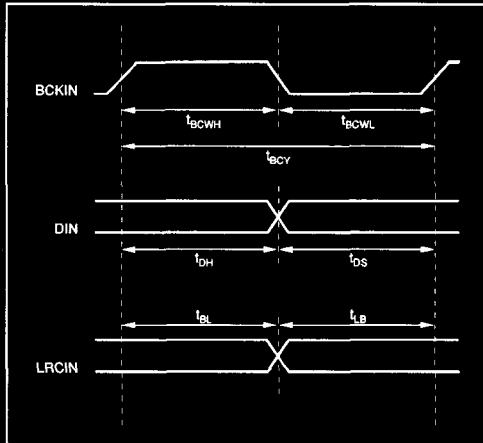


FIGURE 3. Data Input Timing.

BCK Pulsewidth (H Level)	t_{BCWH}	70ns (min)
BCK Pulsewidth (L Level)	t_{BCWL}	70ns (min)
BCK Pulse Cycle Time	t_{BCY}	140ns (min)
DIN Setup Time	t_{DS}	30ns (min)
DIN Hold Time	t_{DH}	30ns (min)
BCK Rising Edge → LRCI Edge	t_{BL}	30ns (min)
LRC I Edge → BCK Rising Edge	t_{LB}	30ns (min)

TABLE I. Data Input Timing Specifications.

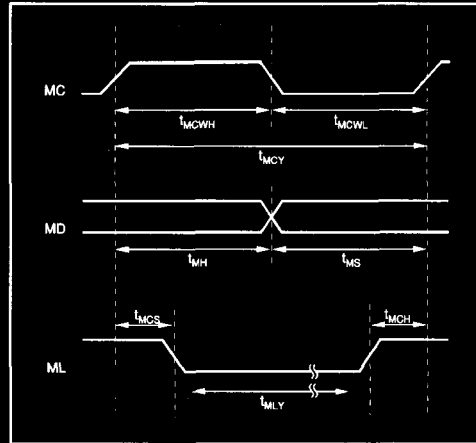


FIGURE 4. Serial Mode Control Timing.

MC Pulsewidth (H Level)	t_{MCWH}	50ns (min)
MC Pulsewidth (L Level)	t_{MCWL}	50ns (min)
MC Pulse Cycle Time	t_{MCY}	100ns (min)
MD Setup Time	t_{MS}	30ns (min)
MD Hold Time	t_{MH}	30ns (min)
ML Setup Time	t_{MCS}	30ns (min)
ML Hold Time	t_{MCH}	30ns (min)
ML Low-Level Time	t_{MLV}	1/sysclk + 20ns (min)

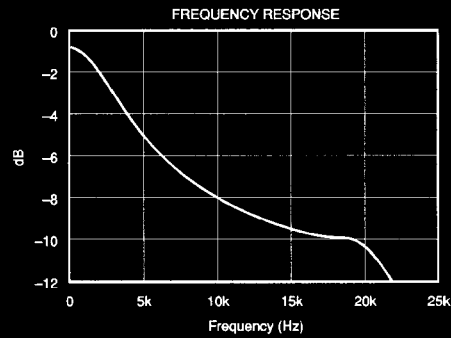
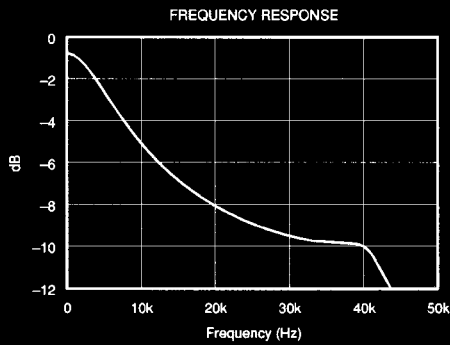
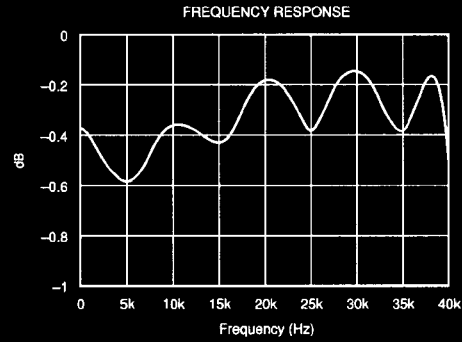
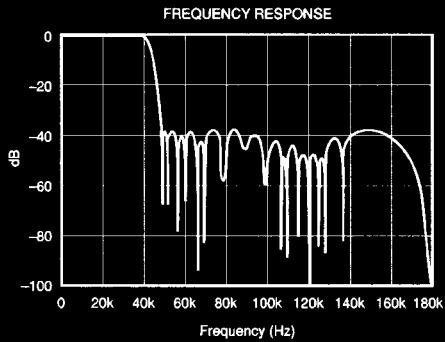
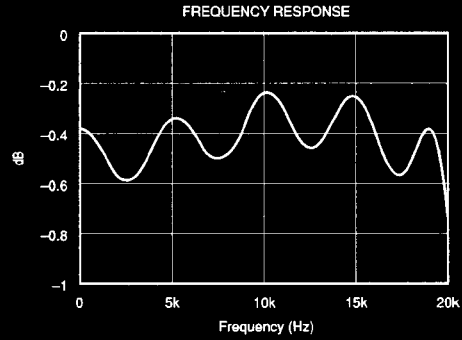
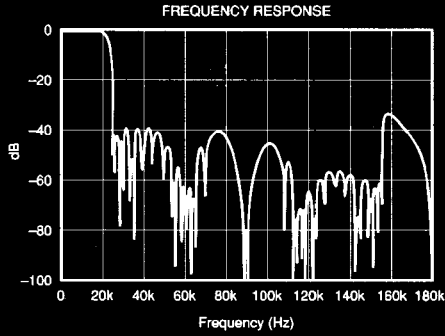
TABLE II. Serial Mode Control Timing Specifications.

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TYPICAL PERFORMANCE CURVES

All specifications at +25°C, +V_{CC} = +V_{DD} = +5V, f_s = 44.1kHz, f_{sig} = 384/256fs, and 16-bit data, unless otherwise noted.

DIGITAL FILTER



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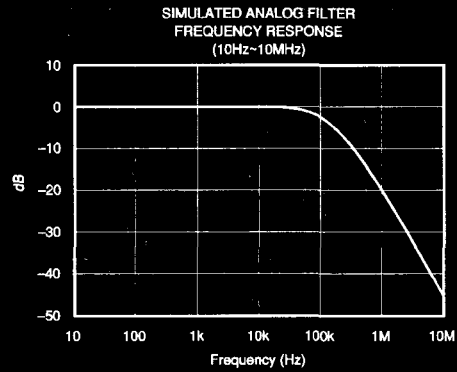
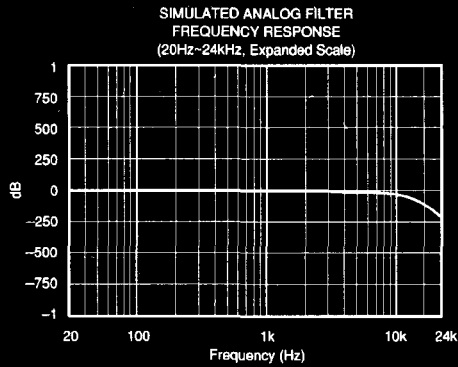


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TYPICAL PERFORMANCE CURVES (CONT)

All specifications at +25°C, +V_{CC} = +V_{DD} = +5V, f_s = 44.1kHz, f_{sys} = 384/256fs, and 16-bit data, unless otherwise noted.

ANALOG FILTER



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MODE CONTROL FUNCTION

The digital functions of PCM1712 are capable of Parallel Mode and Serial Mode. Control functions of both modes are shown below.

MODE CONTROL: SERIAL/PARALLEL SELECTION

MODE = H	Serial Mode
MODE = L	Parallel Mode

TABLE III. Serial and Parallel Mode are Selectable by MODE Pin (Pin 24).

MODE CONTROL: SELECTABLE FUNCTIONS

FUNCTION	SERIAL MODE (MODE = H)	PARALLEL MODE (MODE = L)
Input Data Format Selection	0	X(Normal Mode Fixed)
Input Data Bit Selection	X(16-bit Fixed)	X(16-bit Fixed)
Input LRCl Polarity Selection	0	X
De-emphasis Control	0	0
Mute	0	0
Attenuation	0	X
Double Speed Dubbing	0	0

NOTE: 0: Selectable, X: Not Selectable.

TABLE IV. Selectable Functions in Serial Mode and Parallel Mode.

PARALLEL-MODE: DE-EMPHASIS CONTROL (MODE: L, PIN 24)

DM1 (Pin 26)	DM2 (Pin 27)	De-emphasis
L	L	OFF
H	L	32kHz
L	H	48kHz
H	H	44.1kHz

TABLE V. De-emphasis (Pins 26 and 27).

PARALLEL-MODE: DOUBLE SPEED DUBBING CONTROL (MODE: L, PIN 28)

DSD = H	Normal Mode
DSD = L	Double Speed Dubbing Mode

TABLE VI. DSD (Pin 28).

SERIAL-MODE CONTROL INPUT FORMAT (MODE: H, PIN 24)

	B0	B1	B2	BITS	MODE FLAG	FUNCTION MODE SELECTION			MODE BY RESET		
						MODE	LH	SELECTED FUNCTION			
Mode 1	H	L	L	3	DEEM2	Sampling Frequency for De-emphasis		DEEM2		44.1kHz	
				4	DEEM1			0	1		
								DEEM1	0		48kHz
								1	32kHz		44.1kHz
				5	IIR	De-emphasis	L	De-emphasis OFF	0		
						H	De-emphasis ON				
6	MUTE	Mute	L	Mute OFF	0						
		H	Mute ON								
Mode 2	H	L	H	7	DSD	Double Speed	L	Double-speed OFF	0		
						H	Double-speed ON				
				3		Not Assigned					
				4	TST	Test Mode	H	Normal "H"	H		
				5		Not Assigned					
				6	LRPL	Polarity for LRCl	L	Lch:high/Rch:low	0		
						H	Lch:low/Rch:high				
7	IIS	Input Format	L	Normal	0						
		H	IIS								

TABLE VII. Mode Controls in Serial Mode.

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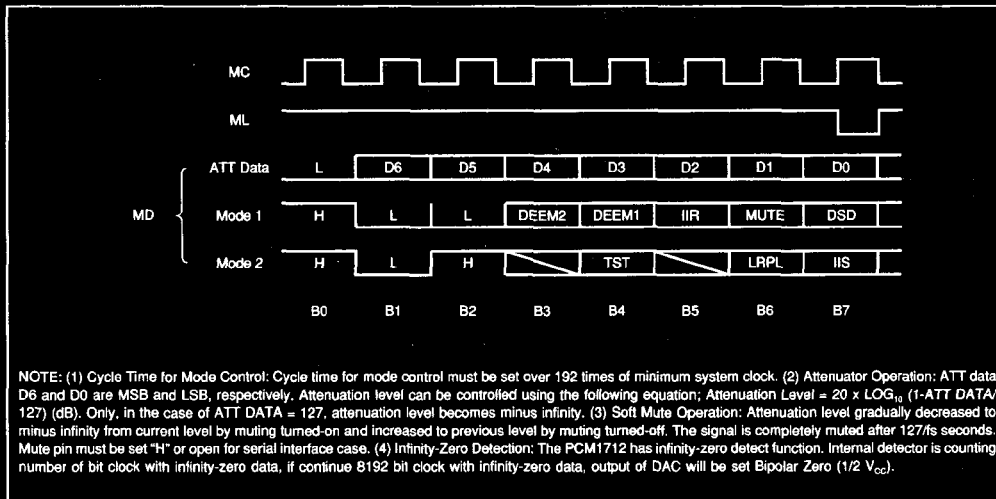


FIGURE 5. Mode Control Input Format, Serial Mode.

OPERATION INSTRUCTION FOR SYSTEM CLOCK

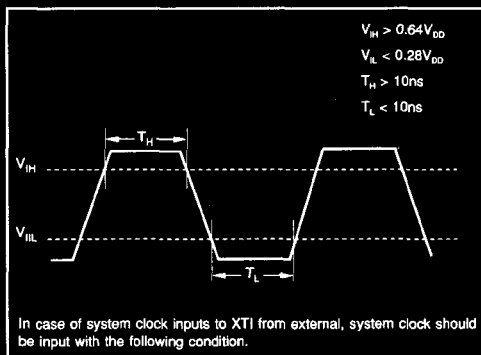


FIGURE 6. Mode Control Input Format, Serial Mode.

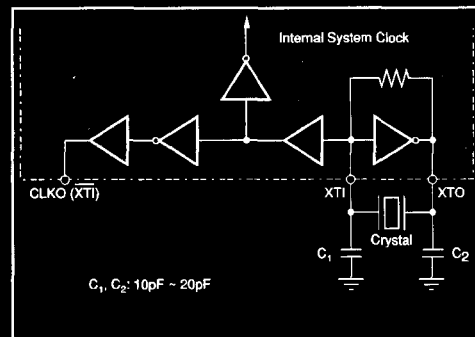


FIGURE 7. External Crystal Oscillator.

SYSTEM CLOCK IN NORMAL/DOUBLE SPEED MODE

The system clock frequency must be fixed at 16.9344MHz in both Normal and Double Speed Dubbing Mode. When the sampling frequency entered to LRCIN is named as "fs", the selection of system clock is shown as the below table.

PARAMETER	DSD	
	H (Normal)	L (Double Speed)
XTI Input Clock Frequency	384fs	192fs
XTI Frequency	16.9344MHz (fs = 44.1kHz)	16.9344MHz (fs = 88.2kHz)
CLKO Output Clock Frequency	384fs	192fs

TABLE VIII.

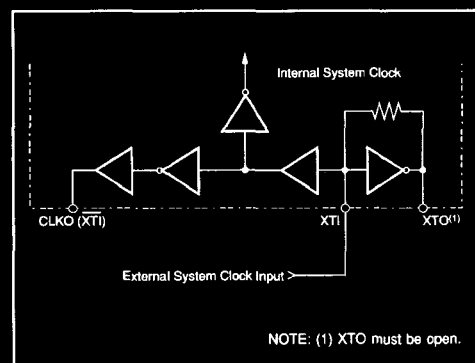


FIGURE 8. External System Clock.