Signetics

PNA7509
7-Bit Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analog-to-digital converter designed for video applications. The device converts the analog input signal into 7-bit binary coded digital words at a sampling rate of 22MHz.

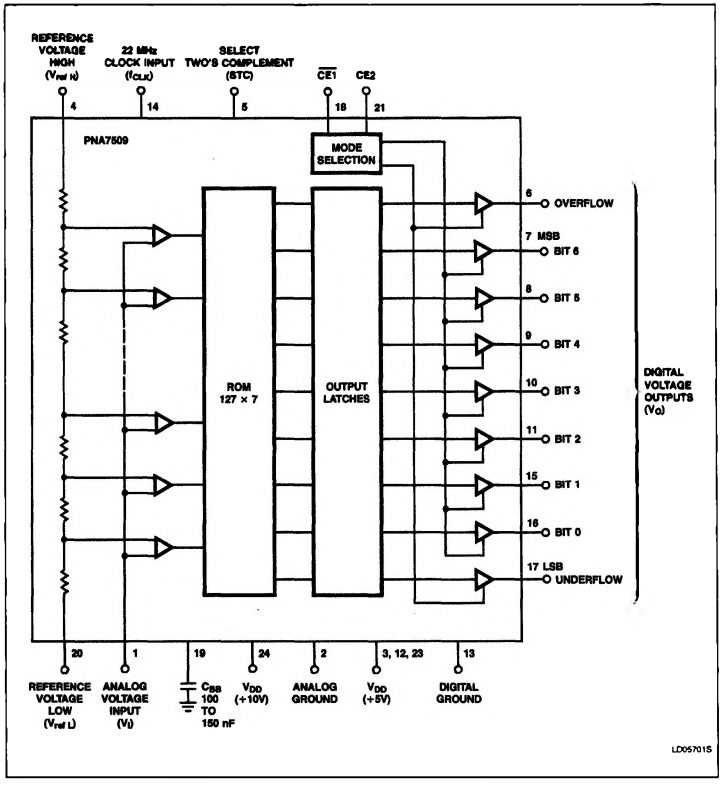
The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge-triggered and can be switched into 3-State mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

FEATURES

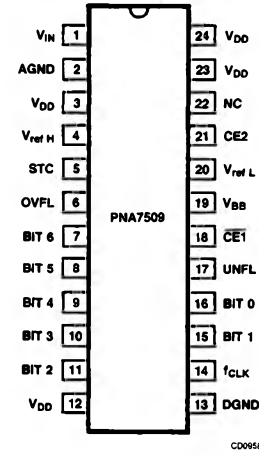
- **7-bit resolution**
- **22MHz clock frequency**
- **No external sample and hold required**
- **High input impedance**
- **Binary or two's complement 3-State TTL outputs**
- **Overflow and underflow 3-State TTL outputs**
- **Low reference current (250μA typ.)**
- **Positive supply voltages (+5V, +10V)**
- **Low power consumption (400mW typ.)**
- **Available in SO Package**

BLOCK DIAGRAM



PIN CONFIGURATION

D, N Packages



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PIN NO.	SYMBOL	DESCRIPTION
1	V_{IN}	Analog voltage input
2	AGND	Analog ground
3	V_{DD}	Positive supply voltage (+5V)
4	V_{REFH}	Reference voltage HIGH
5	STC	Select two's complement
6	OVFL	overflow
7	bit 6	Most-significant bit (MSB)
8	bit 5	
9	bit 4	
10	bit 3	
11	bit 2	
12	V_{DD}	Positive supply voltage (+5V)
13	DGND	Digital ground
14	f_{CLK}	22MHz clock input
15	bit 1	
16	bit 0	Least-significant bit (LSB)
17	UNFL	Underflow
18	$\overline{CE1}$	Chip enable input 1
19	V_{BB}	Back bias output
20	V_{REFL}	Reference voltage LOW
21	CE2	Chip enable input 2
22	NC	Not connected
23	V_{DD}	Positive supply voltage (+5V)
24	V_{DD}	Positive supply voltage (+10V)

APPLICATIONS

- **High-speed A/D conversion**
- **Video signal digitizing**
- **Radar pulse analysis**
- **High energy physics research**
- **Transient signal analysis**

7-Bit Analog-to-Digital Converter PNA7509

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	PNA7509N
24-Pin Plastic SO (SOT-101)	0 to +70°C	PNA7509D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pins 3, 12, 23)	7	V
V_{DD}	Supply voltage range (Pin 24)	12	V
V_{IN}	Input voltage range	7	V
V_{OUT}	Output current	5	mA
P_D	Power dissipation	400	mW
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS $V_{DD} = V_{3, 12, 23-13} = 4.5$ to 5.5V; $V_{DD} = V_{24-2} = 9.5$ to 10.5V; $C_{BB} = 100nF$; $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage (Pins 3, 12, 23)	4.5		5.5	V
V_{DD}	Supply voltage (Pin 24)	9.5		10.5	V
I_{DD}	Supply current (Pins 3, 12, 23)		60	TBD	mA
I_{DD}	Supply current (Pin 24)		10	TBD	mA
Reference voltages					
V_{REFL}	Reference voltage LOW (Pin 20)	2.4	2.5	2.6	V
V_{REFH}	Reference voltage HIGH (Pin 4)	5.0	5.1	5.2	V
I_{REF}	Reference current	175	250	375	mA
Inputs					
	Clock input (Pin 14)				
V_{IL}	Input voltage LOW	−0.3		0.8	V
V_{IH}	Input voltage HIGH	3.0		5.5	V
	Digital input levels (Pins 5, 18, 21)*				
V_{IL}	Input voltage LOW	0		0.8	V
V_{IH}	Input voltage HIGH	2.0		5.5	V
	Input current				
$-I_{5, 21}$	at $V_{5, 21-13} = 0V$	TBD		100	μA
I_{18}	at $V_{18-13} = 5V$	TBD		100	μA
	Input leakage current				
I_{LI}	(except Pins 5, 18, 21)			10	μA
	Analog Input levels (Pin 1)				
	at $V_{REFL} = 2.5V$; $V_{REFH} = 5.1V$				
$V_{IN\ P-P}$	Input voltage amplitude (peak-to-peak value)		2.6		V
V_{IN}	Input voltage (underflow)		2.5		V
V_{IN}	Input voltage (overflow)		5.1		V
$V_I - V_{REFL}$	Offset input voltage (underflow)		10		mV
$V_I - V_{REFH}$	Offset input voltage (overflow)		−10		mV
$C_{1, 2}$	Input capacitance	TBD		60	pF
Outputs					
	Digital voltage outputs (Pins 6 to 11 and 15 to 17)				
	Output voltage LOW				
V_{OL}	at $I_O = 2mA$	0		−0.4	V
	Output voltage HIGH				
V_{OH}	at $-I_O = 0.5mA$	2.4		V_{DD}	V

*When Pin 5 is LOW, binary coding is selected.
When Pin 5 is HIGH, two's complement is selected.
If Pins 5, 18 and 21 are open-circuit, Pins 5, 21 are HIGH and Pin 18 is LOW.
For output coding see Table 1; for mode selection see Table 2.

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{3, 12, 23-13} = 4.5$ to 5.5V; $V_{DD} = V_{24-2} = 9.5$ to 10.5V; $V_{REFL} = 2.5V$; $V_{REFH} = 5.1V$; $f_{CLK} = 22MHz$; $C_{BB} = 100nF$; $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Timing (see also Figure 1)					
	Clock input (Pin 14)				
f_{CLK}	clock frequency	1		22	MHz
t_{LOW}	clock cycle time LOW	20			ns
t_{HIGH}	clock cycle time HIGH	20			ns
	Input rise and fall times[1]				
t_R	rise time			3	ns
t_F	fall time			3	ns
	Analog input[1]				
BW	Bandwidth (−3 dB)				
	at $V_{1-2(P-P)} = 2.2V$	10			MHz
dG	Differential gain				
	at $f_I = \leqslant 4.5MHz$[2]			5	%
dp	Differential phase				
	at $f_I = \leqslant 4.5MHz$[2]			5	deg
P_E	Phase error				
	at $f_I = \leqslant 4.5MHz$[3]			± 10	deg
S/N	Signal-to-noise ratio				
	at $V_{1-2(P-P)} = 2.2V$;				
	$f_I = \leqslant 4.5MHz$; B = ± 1 MHz	36			dB
	Harmonics				
	at $V_{1-2(P-P)} = 2.2V$;				
	$f_I = 3.6MHz$				
f_0	Fundamental		0	0	dB
f_{2nd}	2nd harmonic			tbd	dB
f_{3rd}	3rd harmonic			tbd	dB
f_{4th}	4th harmonic			tbd	dB
f_{5th}	5th harmonic			tbd	dB
f_{6th}	6th harmonic			tbd	dB
f_{7th}	7th harmonic			tbd	dB
	Harmonics				
	at $V_{1-2(P-P)} = 2.2V$;				
	$f_I = 4.5MHz$				
f_0	Fundamental		0	0	dB
f_{2nd}	2nd harmonic			tbd	dB
f_{3rd}	3rd harmonic			tbd	dB
f_{4th}	4th harmonic			tbd	dB
f_{5th}	5th harmonic			tbd	dB
f_{6th}	6th harmonic			tbd	dB
f_{7th}	7th harmonic			tbd	dB
	Digital outputs[2, 4]				
t_{HOLD}	Output hold time	6	15		ns
t_D	Output delay time		20	28	ns
t_{CY}	Internal delay		3		clocks
	Propagation delay time				
t_{PD}	at $f_{CLK} = 20.25MHz$	154		176	ns
t_{DT}	3-State delay time (see Figure 2)	t_{BF}	10	20	ns
C_{OL}	Capacitive output load[2]	0		15	pF
	Transfer function				
	Non-linearity				
INL	integral			± 1	LSB
DNL	differential			± 1/2 = 0.4%	LSB

NOTES:

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sine wave (peak-to-peak value of the analog input voltage at $V_{IN} = 1.8V$) amplitude modulated with a sine wave voltage ($V_{IN} = 0.7V$) at $f_I \leqslant 4.5MHz$.
3. Sine wave voltage with increasing amplitude at $f_I \leqslant 4.5MHz$ (minimum amplitude $V_{IN} = 0.25V$; maximum amplitude $V_{IN} = 2.5V$).
4. The timing values of the digital output Pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1.5V.

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Table 1. Output Coding (V_{REFL} = 2.5V; V_{REFH} = 5.1V)

STEP	$V_{1, 2}$ (Typ)	UNFL	OVFL	BINARY Bit 6 – Bit 0	TWO's COMPLEMENT Bit 6 – Bit 0
Underflow	< 2.51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2.51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2.53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
126	5.03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5.05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
Overflow	⩾ 5.07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

Table 2. Mode Selection

CE1	CE2	BIT 0 to BIT 6	UNFL, OVFL
X	0	High impedance	High impedance
0	1	Active	Active
1	1	High impedance	Active

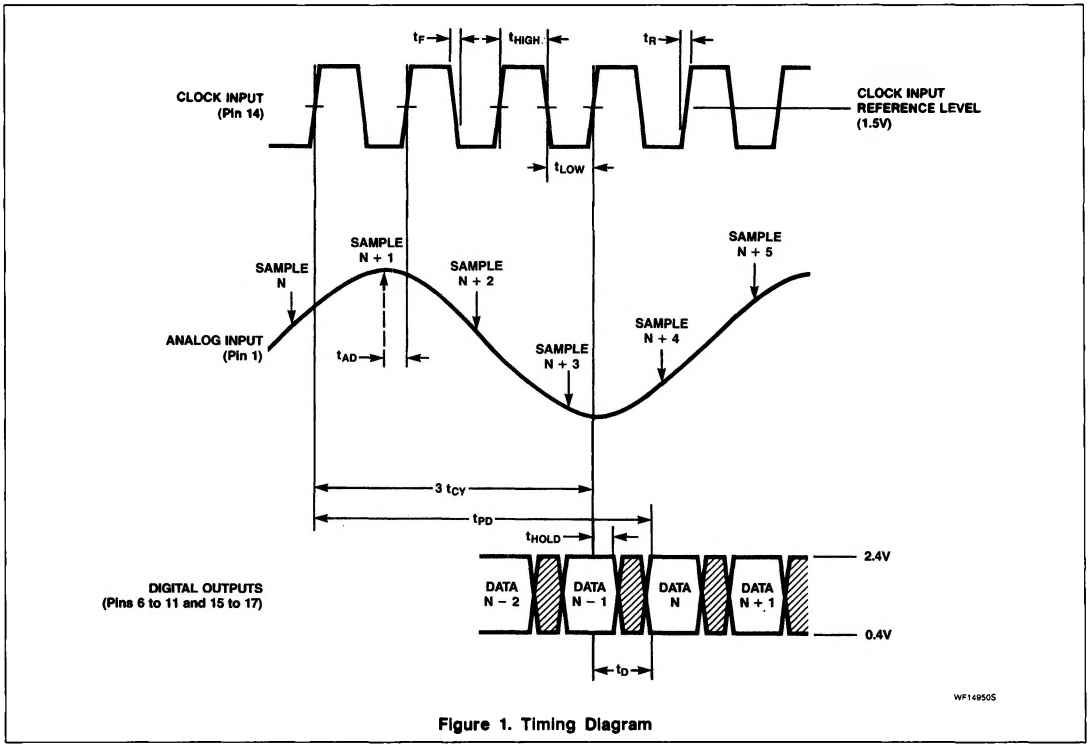

Figure 1. Timing Diagram

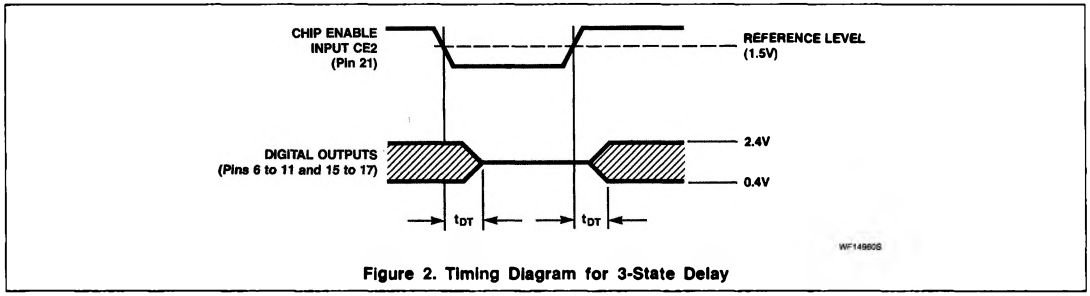

Figure 2. Timing Diagram for 3-State Delay

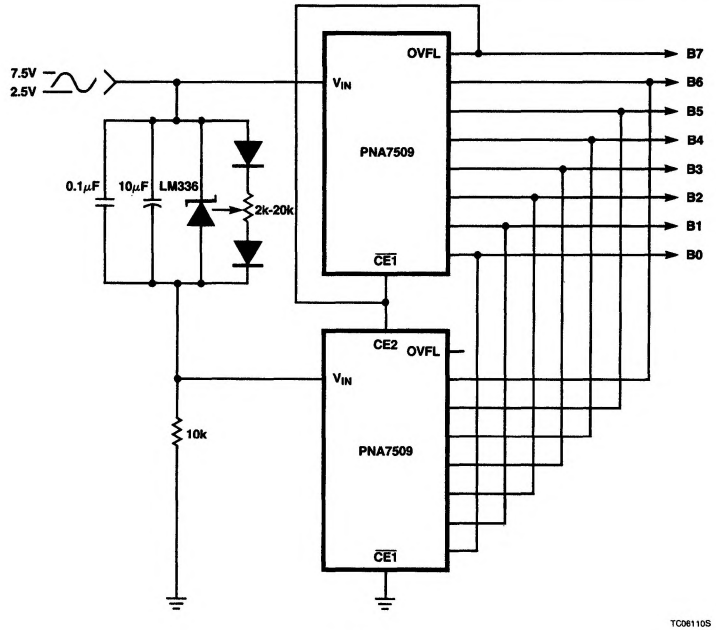
7.5V
2.5V
0.1μF
10μF
LM336
2k-20k
10k
OVFL
VIN
PNA7509
CE1
CE2
B7
B6
B5
B4
B3
B2
B1
B0
TC06110S

Figure 3