

## Features

- Low-noise Low Drop Out Voltage Regulator
- 2.8V Fixed Output Voltage
- 3V to 5.5V Supply Operation
- 130 mA Maximum Load Current
- Power-down Mode Consumption Less Than 1  $\mu$ A
- More Than 70 dB (Typical) PSRR at 1 kHz
- 29  $\mu$ V<sub>RMS</sub> Output Noise
- 0.35  $\mu$ m CMOS Technology
- Typical Application: Radio Section Supply in Mobile Terminals

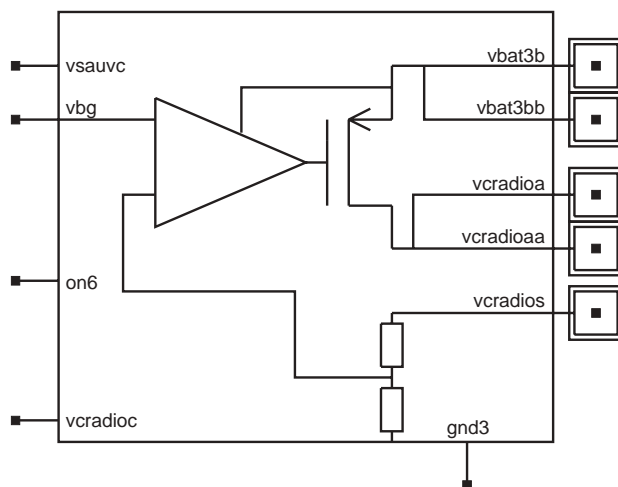
## Description

RE027 is a Low Drop Out (LDO) voltage regulator macrocell with a fixed 2.8V output voltage, rated for loads up to 130 mA. It is designed to be integrated with other analog cells, digital logic, microcontrollers, DSP cores and memory blocks into system-on-chip products.

The circuit consists of a PMOS pass device, an error amplifier and a feedback resistive network, sized to achieve the required closed loop gain. These blocks make up the regulating loop. An over-current and short circuit protection circuit has been included to limit the output current delivered by the regulator, thus avoiding destruction in case of a short circuit.

An external reference voltage (bandgap voltage) is necessary for correct functionality. The target reference voltage is 1.231V delivered, for example, by BG019. Double pads on the supply voltage  $V_{BAT3B}/V_{BAT3BB}$  and output voltage  $V_{CRADIOA}/V_{CRADIOAA}$  are used to reduce the total output resistance. Current reference is generated inside the cell through a circuit supplied by a  $2.5V \pm 0.1V$  regulated input voltage on  $V_{SAUVC}$ . Remote sense terminal  $V_{CRADIOS}$  provides regulation at the load by connecting it to the output terminal near a critical point to improve performance of the regulator (e.g., connecting them at the package pin by double-bonding, thus avoiding the bonding resistance influence). A capacitor of 2.2  $\mu$ F connected from  $V_{CRADIOA}/V_{CRADIOAA}$  to ground is needed as external compensation.

Figure 1. Symbol<sup>(1)</sup>



Note: 1. Pin names are written as they appear on the user screen when the symbol is opened in the design tool environment.



**Embedded ASIC  
Macrocell:  
Power  
Management for  
Mobile  
Terminals (PM)**

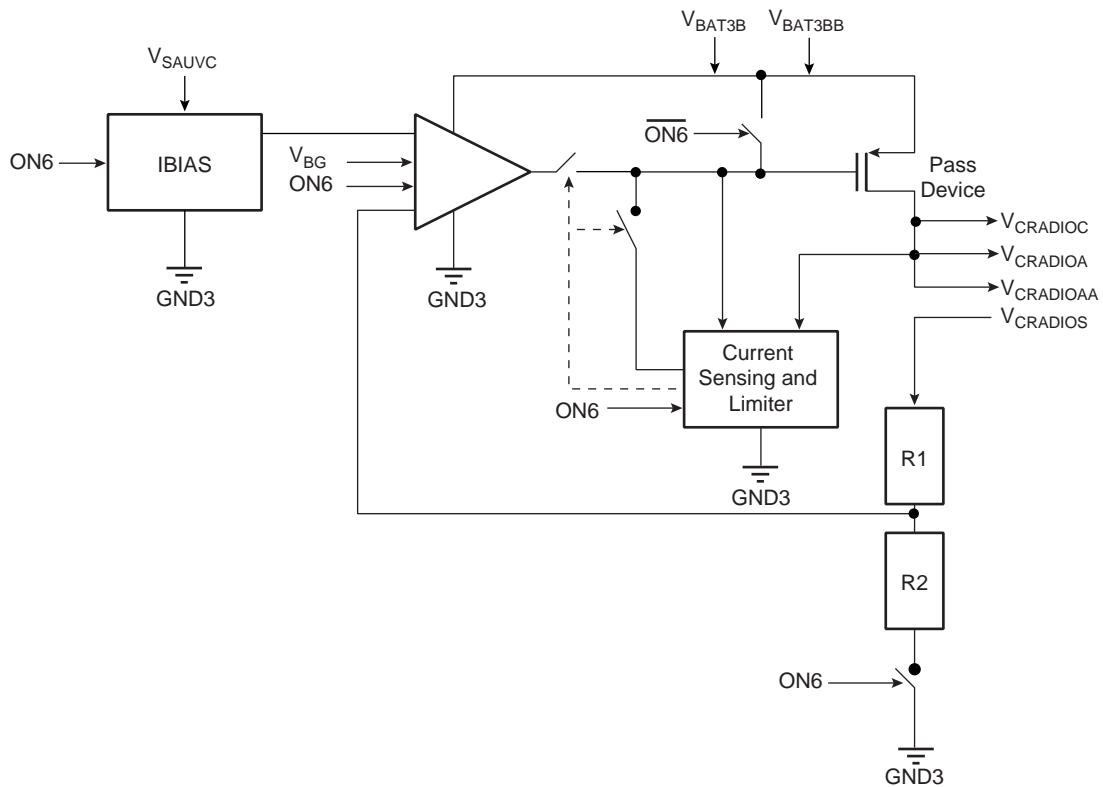
**RE027  
Fixed 2.8V  
130 mA  
Low-noise LDO  
Voltage  
Regulator**

Rev. 2701B-PMGMT-02/03



## Functional Diagram

Figure 2. Functional Diagram



## Pin Description

Pin Name	I/O	Type	Function	Value
$V_{BAT3B}$	Power supply	External pad	Power supply	3V to 5.5V
$V_{BAT3BB}$	Power supply	External pad	Power supply	3V to 5.5V
$V_{CRADIOA}$	Analog output	External pad	Output voltage	2.75V to 2.85V
$V_{CRADIOAA}$	Analog output	External pad	Output voltage	2.75V to 2.85V
$V_{CRADIOS}$	Analog input	External pad	Sense voltage	2.75V to 2.85V
$V_{CRADIOC}$	Analog output	Internal pin	Output voltage	2.75V to 2.85V
GND3	Ground	Internal pin	Ground	0
$V_{SAUVC}$	Power supply	Internal pin	Power supply	$2.5V \pm 0.1V$
$V_{BG}$	Analog input	Internal pin	Voltage reference	1.231V
ON6	Digital input	Internal pin	Enable command	0V or $V_{BAT3B}/V_{BAT3BB}$

# RE027 2.8V 130 mA LDO Voltage Regulator

## Absolute Maximum Ratings\*

$V_{IN}$ .....	-0.3V to 6.5V
Digital Signals.....	-0.3V to 5.5V
Output Current.....	Internally Limited
Junction Temperature .....	-40°C to 150°C

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Electrical Specifications<sup>(1)</sup>

$T_J = -20^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{BAT3B}/V_{BAT3BB} = 3\text{V}$  to  $5.5\text{V}$  unless otherwise specified, output capacitance =  $2.2\ \mu\text{F}$ .

**Table 1.** Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
$V_{BAT3B}/V_{BAT3BB}$	Operating Supply Voltage		3		5.5	V	
$V_{SAUVC}$	Auxiliary Operating Supply Voltage		2.4	2.5	2.6	V	
$T_J$	Junction Temperature Range		-20		125	°C	
$V_{CRADIOA}/V_{CRADIOAA}$	Output Voltage		2.75	2.8	2.85	V	
$I_{CRADIOA}/I_{CRADIOAA}$	Output Current				130	mA	
$I_{QQ}$	Quiescent Current			195	236	μA	
$\Delta V_{DC}$	Line Regulation	$I_{CRADIOA}/I_{CRADIOAA} = 130\ \text{mA}$		2	3	mV	
$\Delta V_{TRAN}$	Transient Line Regulation	$I_{CRADIOA}/I_{CRADIOAA} = 130\ \text{mA}$ rise time = fall time = $5\ \mu\text{s}$		2	3	mV	
$\Delta V_{DC}$	Load Regulation	10% - 90% of max $I_{CRADIOA}/I_{CRADIOAA}$ ; $V_{BAT3B}/V_{BAT3BB} = 5.5\text{V}$		2	3	mV	
$\Delta V_{TRAN}$	Transient Load Regulation	10% - 90% of max $I_{CRADIOA}/I_{CRADIOAA}$ ; rise time = fall time = $5\ \mu\text{s}$		2	3	mV	
PSRR	Power Supply Rejection Ratio at Full Load	$V_{BAT} = 3\text{V}$	@ 100 Hz		-75		dB
			@ 1 kHz		-75		dB
			@ 20 kHz		-50		dB
			@ 100 kHz		-40		dB
		$V_{BAT} = 4.25\text{V}$	@ 100 Hz		-75		dB
			@ 1 kHz		-75		dB
			@ 20 kHz		-70		dB
			@ 100 kHz		-55		dB
		$V_{BAT} = 5.5\text{V}$	@ 100 Hz		-75		dB
			@ 1 kHz		-75		dB
			@ 20 kHz		-70		dB
			@ 100 kHz		-55		dB

**Table 1.** Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_N$	Output Noise <sup>(2)</sup>	Bandwidth = 10 Hz to 100 kHz; output current = 130 mA		29	37	$\mu V_{RMS}$
$T_R$	Rise Time	100% of $I_{CRADIOA}/I_{CRADIOAA}$ ; 10% - 90% of $V_{CRADIOA}/V_{CRADIOAA}$			50	$\mu s$
$I_{SD}$	Shut Down Current				1	$\mu A$
$I_{CC}$	Short-circuit Current Threshold				460	mA

Notes: 1. Obtained by considering the parasitics of a TFBGA100 Package.  
2. Obtained by using BG019 as reference voltage generator.

# RE027 2.8V 130 mA LDO Voltage Regulator

## Control Modes

All digital signals are referred to the supply voltage  $V_{BAT3B/BAT3BB}$ .

**Table 2.** Truth Table

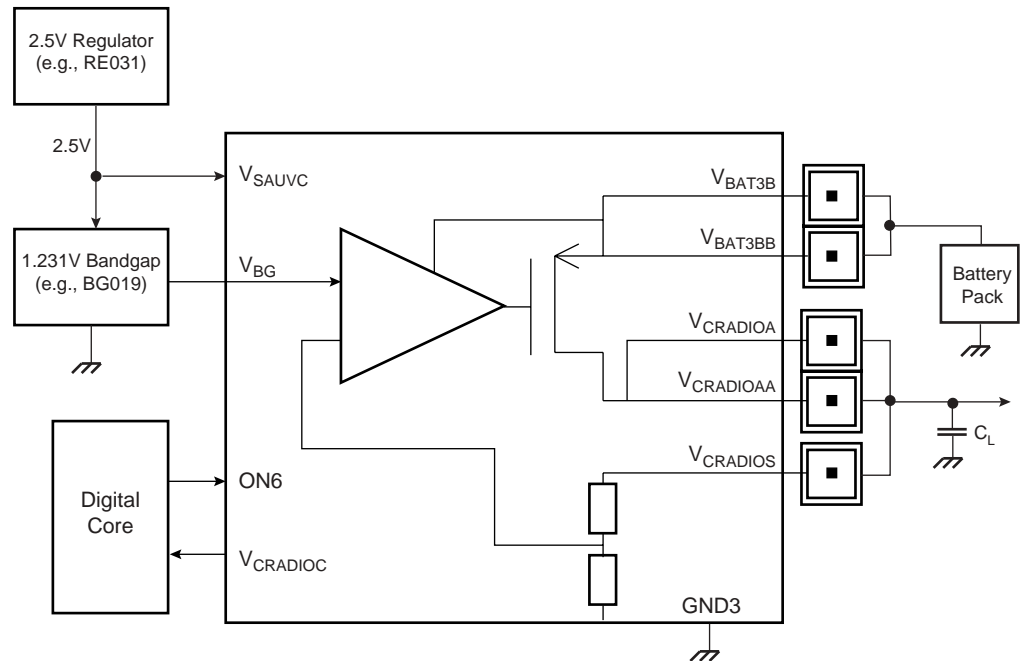
ON6	$V_{CRADIOA}/V_{CRADIOAA}$
0	Power down (High-Z)
1	Power on, $V_{CRADIOA}/V_{CRADIOAA} = 2.8V$

## Application Example

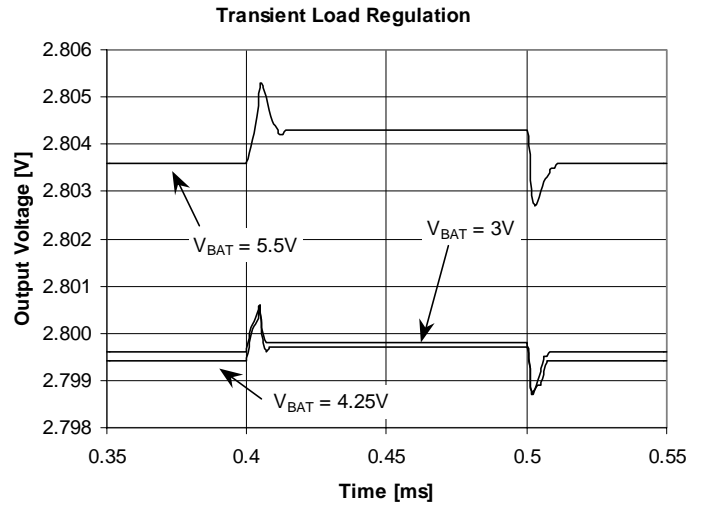
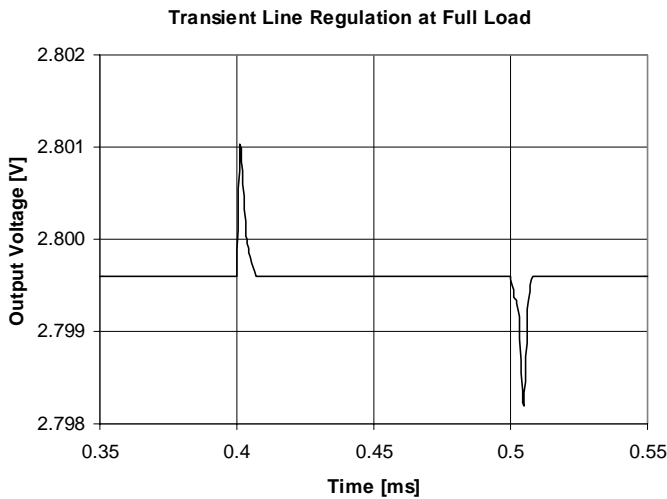
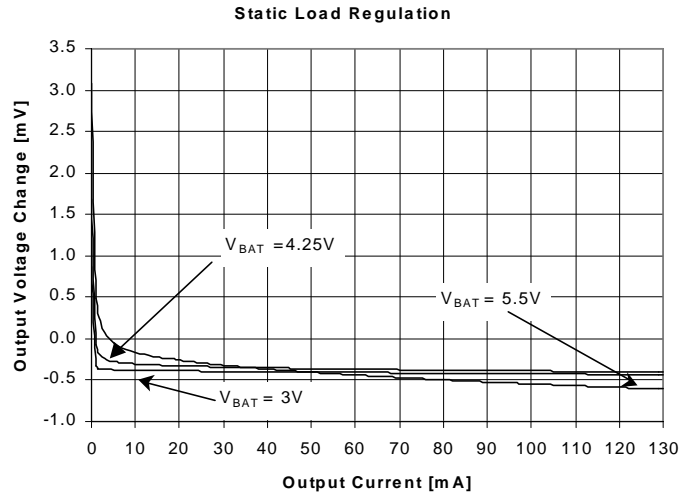
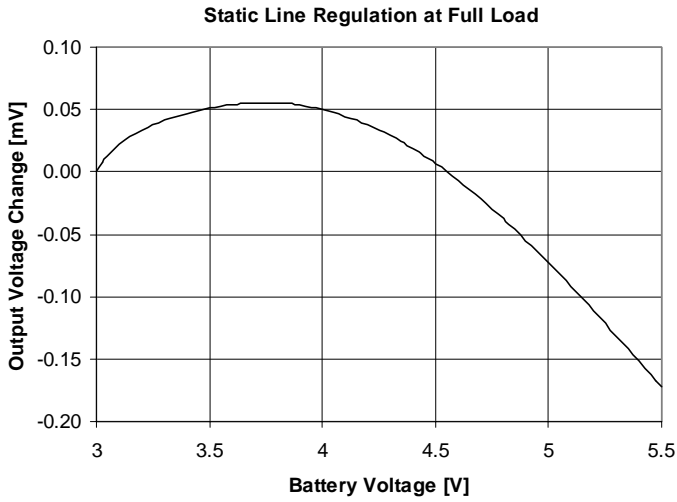
A ceramic capacitor of 2.2  $\mu F$  with ESR between 20 m $\Omega$  and 250 m $\Omega$  connected from  $V_{CRADIOA}/V_{CRADIOAA}$  to ground is needed for external compensation.

Description	Min	Typ	Max	Units
Capacitor ( $C_L$ )	1.8	2.2	2.6	$\mu F$

**Figure 3.** Application Example



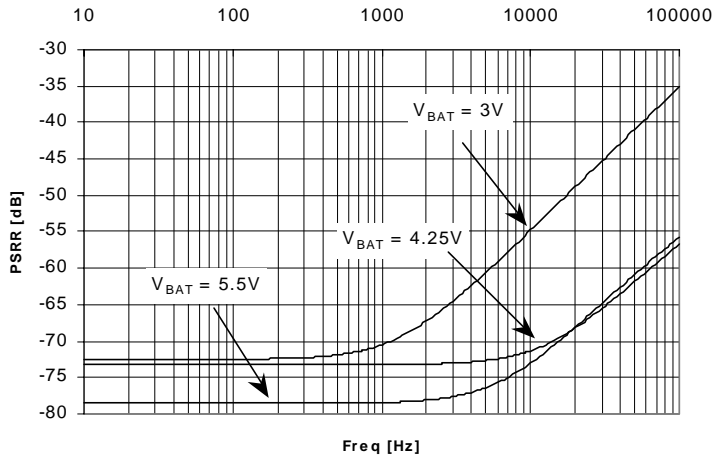
## Typical Performance Characteristics (Conditions specified on page 8)



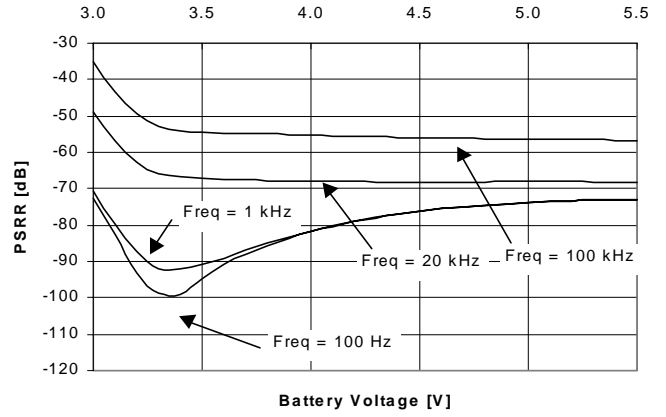
# RE027 2.8V 130 mA LDO Voltage Regulator

## Typical Performance Characteristics (Conditions specified on page 8)

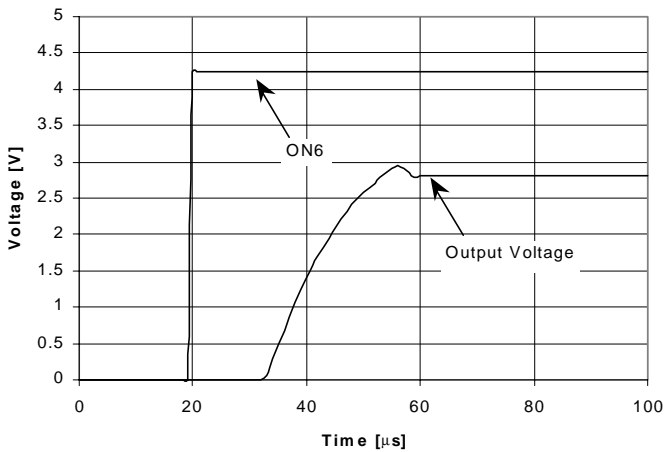
Power Supply Rejection Ratio at Full Load



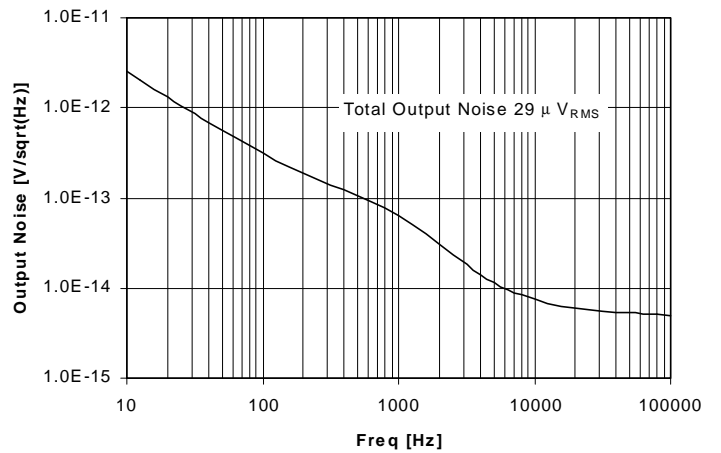
Power Supply Rejection Ratio at Full Load versus Battery Voltage



LDO Startup at Full Load for  $V_{BAT} = 4.25V$



Output Noise Spectrum at Full Load and  $V_{BAT} = 4.25V$

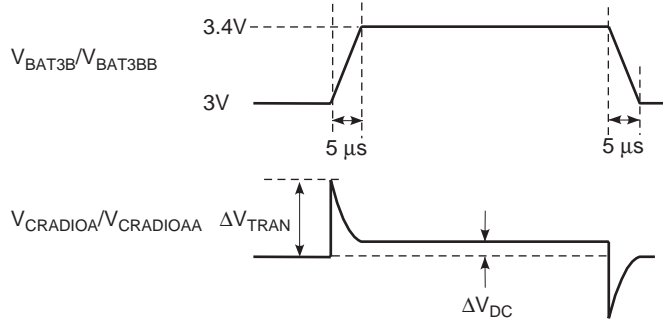


## Terminology

### Line Regulation

Measures the maximum transient and DC variations of the output voltage of the LDO when the supply changes between two specified values with fixed load current; minimum rise time and fall time is 5  $\mu$ s.

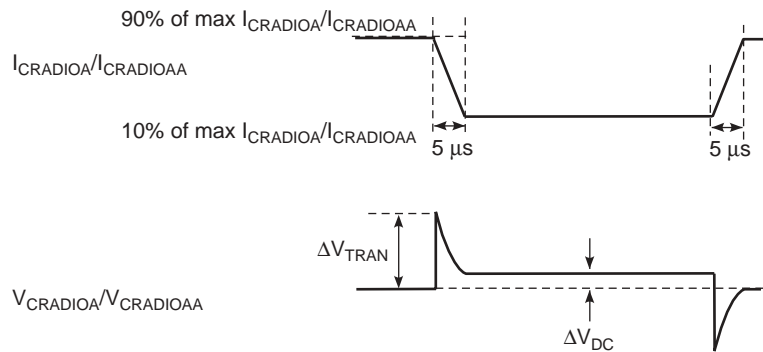
**Figure 4.** Line Regulation



### Load Regulation

Measures the maximum transient and DC variations of the output voltage of the LDO when the load current changes between two specified values with fixed power supply; minimum rise time and fall time is 5  $\mu$ s.

**Figure 5.** Load Regulation







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