DYNAMIC NFC INTERFACE TRANSPONDER

FEATURES

- **NFC Type-4 Tag**
- **ISO14443B Compliant 13.56-MHz RF Interface Supports up to 848 kbps**
- **SPI or I^2C Interface to Write and Read NDEF Messages to Internal SRAM**
- **Operating Voltage Range: 3.0 V to 3.6 V**

DESCRIPTION

The Texas Instruments Dynamic NFC Interface Transponder RF430CL330H is a NFC Tag Type 4 device that combines a wireless NFC interface and a wired SPI or I^2C interface to connect the device to a host. The NDEF message in the SRAM can be written and read from the integrated SPI or I^2C serial communication interface and can also be accessed and updated wirelessly via the integrated ISO14443B-compliant RF interface that supports up to 848 kbps.

This allows NFC connection handover for an alternative carrier like *Bluetooth*™, *Bluetooth* Low Energy (BLE), and Wi-Fi as an easy and intuitive pairing process or authentication process with only a tap. As a general NFC interface, the RF430CL330H enables end equipments to communicate with the fast-growing infrastructure of NFC-enabled smart phones, tablets, and notebooks.

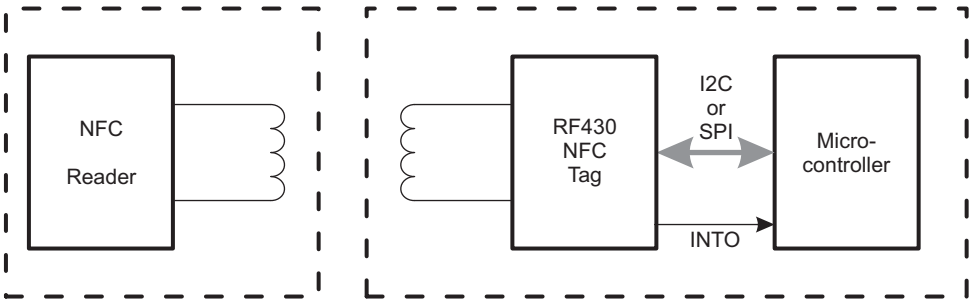


Figure 1. Typical Application

Table 1. Ordering Information(1)

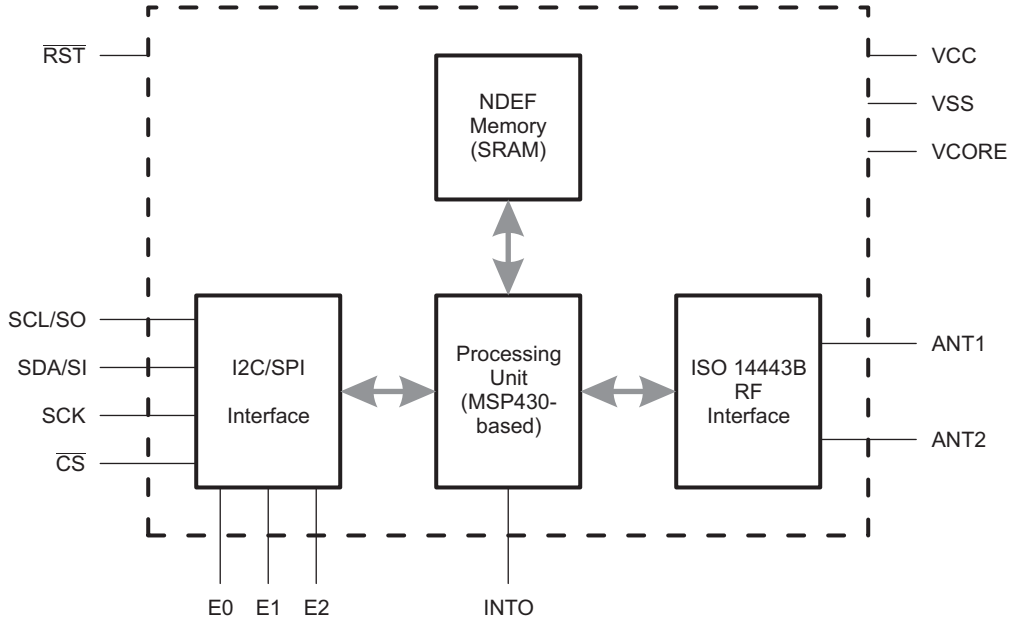
T_A	PACKAGED DEVICES(2)
	PLASTIC 14-PIN TSSOP (PW)
0ºC to 70ºC	RF430CL330HCPWR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

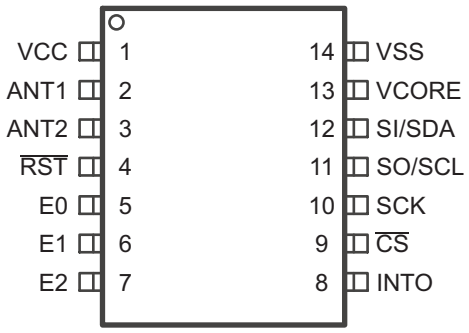
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

PRODUCT PREVIEW

Functional Block Diagram



PW PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

Table 2. Terminal Functions

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
VCC	1	PWR	3.3-V power supply
ANT1	2	RF	Antenna input 1
ANT2	3	RF	Antenna input 2
$\overline{RST}$	4	I	Reset input (active low)(2)
E0 (TMS)	5	I	I2C address select 0(3) (JTAG test mode select(4))
E1 (TDO)	6	I (O)	I2C address select 1(3) (JTAG test data output(4))
E2 (TDI)	7	I	I2C address select 2(3) (JTAG test data in(4))
INTO (TCK)	8	O	Interrupt output (JTAG test clock(4))
$\overline{CS}$	9	I	SPI mode select(5) Chip select (SPI mode) (active low)
SCK	10	I	SPI clock input (SPI mode)
SO/SCL	11	I/O	SPI slave out (SPI mode) I2C clock (I2C mode)
SI/SDA	12	I/O	SPI slave in (SPI mode) I2C data (I2C mode)
VCORE	13	PWR	Regulated core supply voltage
VSS	14	PWR	Ground supply

(1) I = Input, O = Output, PWR = Power, RF = RF Antenna
(2) With integrated pullup
(3) Tie low in SPI mode to avoid floating inputs.
(4) This device does not provide JTAG-compliant boundary scan test.
(5) Selects I2C or SPI mode during power-up and initialization (see). Tie low to select I2C mode.

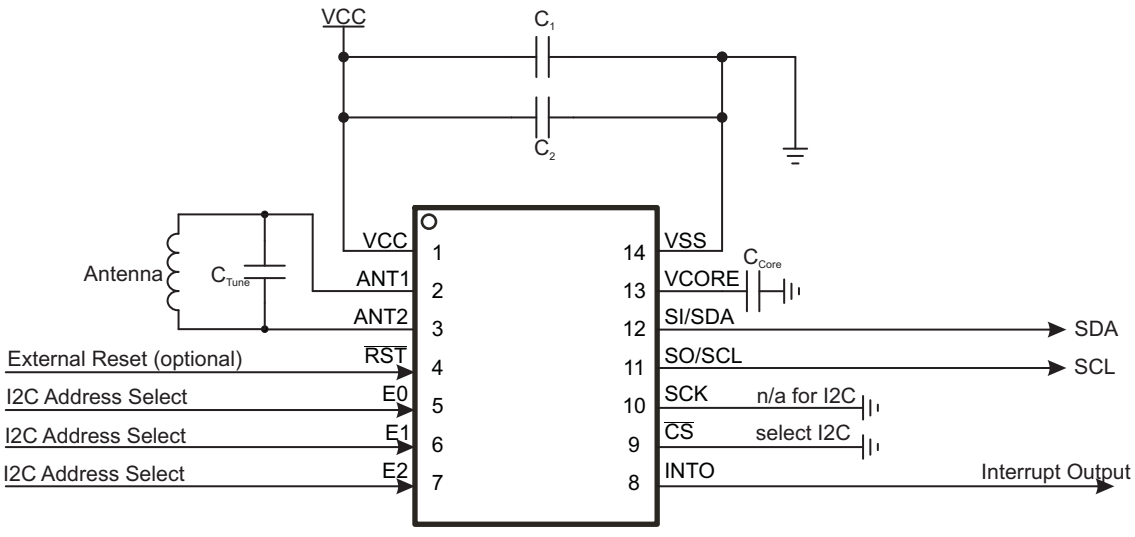


Figure 2. Example Application Diagram (I2C Operation)

PRODUCT PREVIEW

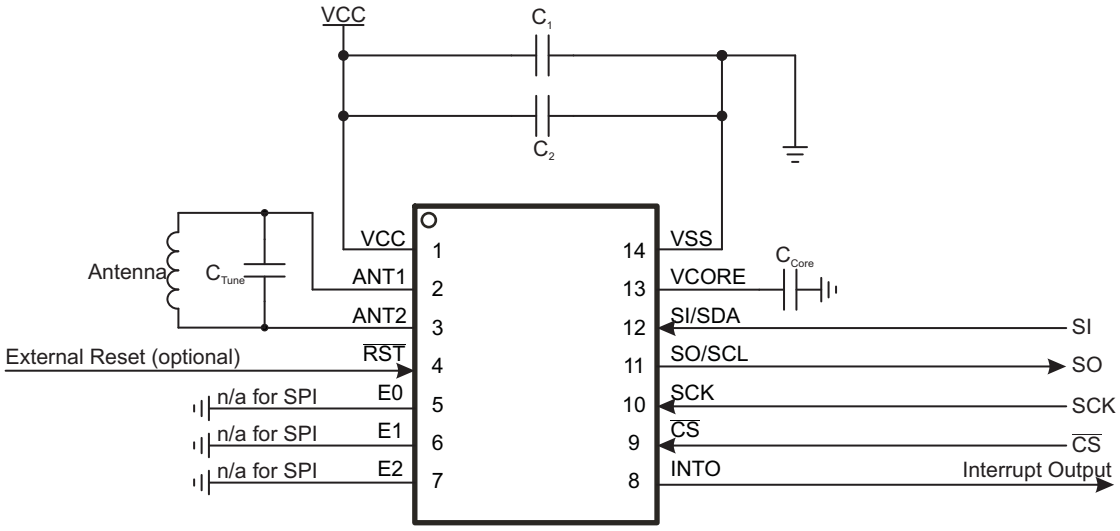


Figure 3. Example Application Diagram (SPI Operation)

PRODUCT PREVIEW

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