DESCRIPTION

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. N74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with N74121.

The output pulse is primarily a function of the external capacitor and resistor. For C_{ext} > 1000pF, the output pulse width (t_W) is defined as:

$$t_W = 0.32\ R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

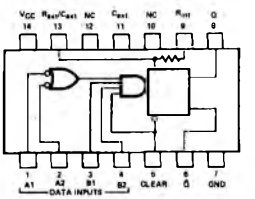
R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_W is in ns

For pulse widths when $C_{ext} \leq$ 1000pF, see Figure B.

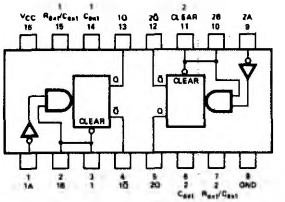
These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one shot is 115 milliwatts; typical average propagation delay time to the Q output is 21 nanoseconds. The N74122 and N74123 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

54/74123 B,F,W PACKAGE



74122 A,F PACKAGE



†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE (See Note A)

N74122

INPUTS				OUTPUTS	
A_1	A_2	B_1	B_2	Q	Q̄
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎍
L	X	H	↑	⎍	⎍
X	L	H	H	L	H
X	L	↑	H	⎍	⎍
X	L	H	↑	⎍	⎍
H	↓	H	H	⎍	⎍
↓	↓	H	H	⎍	⎍
	H	H	H	⎍	⎍

S54123,N74123

INPUTS		OUTPUTS	
A	B	Q	Q̄
H	X	L	H
X	L	L	H
L	↑	⎍	⎍
↓	H	⎍	⎍

NOTES:

A. H = high level (steady-state), L = low level (steady-state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎍ = one low-level pulse, X = irrelevant (any input, including transitions).

B. NC = No internal connection.

C. To use the internal timing resistor of N74122 (10kΩ nominal), connect R_{int} to V_{CC}.

D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

RECOMMENDED OPERATING CONDITIONS

		S54123, N74122, N74123			UNIT
		MIN	NOM	MAX	
Supply Voltage V_{CC}		4.75	5	5.25	V
Normalized Fan-Out from each Output, N	High Logic Level			20	
	Low-Logic Level			10	
Input data setup time, t_{setup} (See Note 3)		40†			ns
Input data hold time, t_{hold} (See Note 4)		40†			ns
Width of Clear Pulse, $t_{w(clear)}$		40†			ns
External Timing Resistance		5		50	kΩ
External Capacitance		No Restriction			
Wiring Capacitance at R_{ext}/C_{ext} Terminal				50	pF
Operating Free-Air Temperature, T_A		0	25	70	°C

†These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

NOTES:
1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the N74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.
5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at Q, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open. C_{ext} = 0.02μF, and R_{ext} = 25kΩ. R_{int} of S54122/N74122 is open.
7. I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open. C_{ext} = 0.02μF, and R_{ext} = 25kΩ. R_{int} of S54122/N74122 is open.

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

	PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = -12mA			-1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 5	I_{OH} = -800μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 5	I_{OL} = 16mA,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4V			40	μA
		clear input					80	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
		clear input					-3.2	
I_{OS}	Short-circuit output current†		V_{CC} = MAX,	See Note 5	-10		-40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7	N74122		23	28	mA
				N74123		46	66	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input				22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				19	28	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input	C_{ext} = 0, C_L = 15pF,	R_{ext} = 5kΩ, R_L = 400Ω,		30	40	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				27	36	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input				18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output, from clear input				30	40	ns
$t_{w(min)}$	Minimum width of Q output pulse				45	65	ns
t_w	Width of Q output pulse	C_{ext} = 1000pF, C_L = 15pF,	R_{ext} = 10kΩ R_L = 400Ω	3.08	3.42	3.76	μs

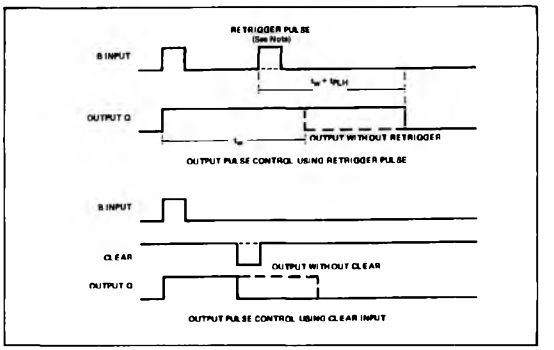
* For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DESCRIPTION

These monolithic TTL retriggerable monostable multivibrators feature dc triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

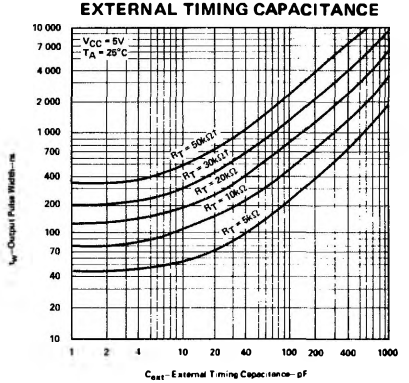
Figure A illustrates triggering the one-shot with the high-level-active (B) inputs.

TYPICAL INPUT/OUTPUT PULSES (Figure A)

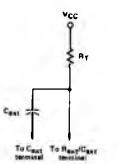


TYPICAL CHARACTERISTICS (Figure B)

OUTPUT PULSE WIDTH VS EXTERNAL TIMING CAPACITANCE



† These values of resistance exceed the maximums recommended for use over the full temperature range of the S54122 and S54123.



NOTE:
When using electrolytic capacitor, insure that minimum rating is 20 volts so that 5% reverse voltage rating is 1.0 volt or greater.