8-BIT SHIFT REGISTER

S54166
N74166

S54166–B,F,W • N74166–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

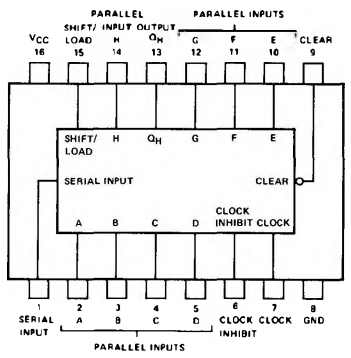
These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of -55°C to 125°C. Series 74 devices are characterized for operation from 0°C to 70°C.

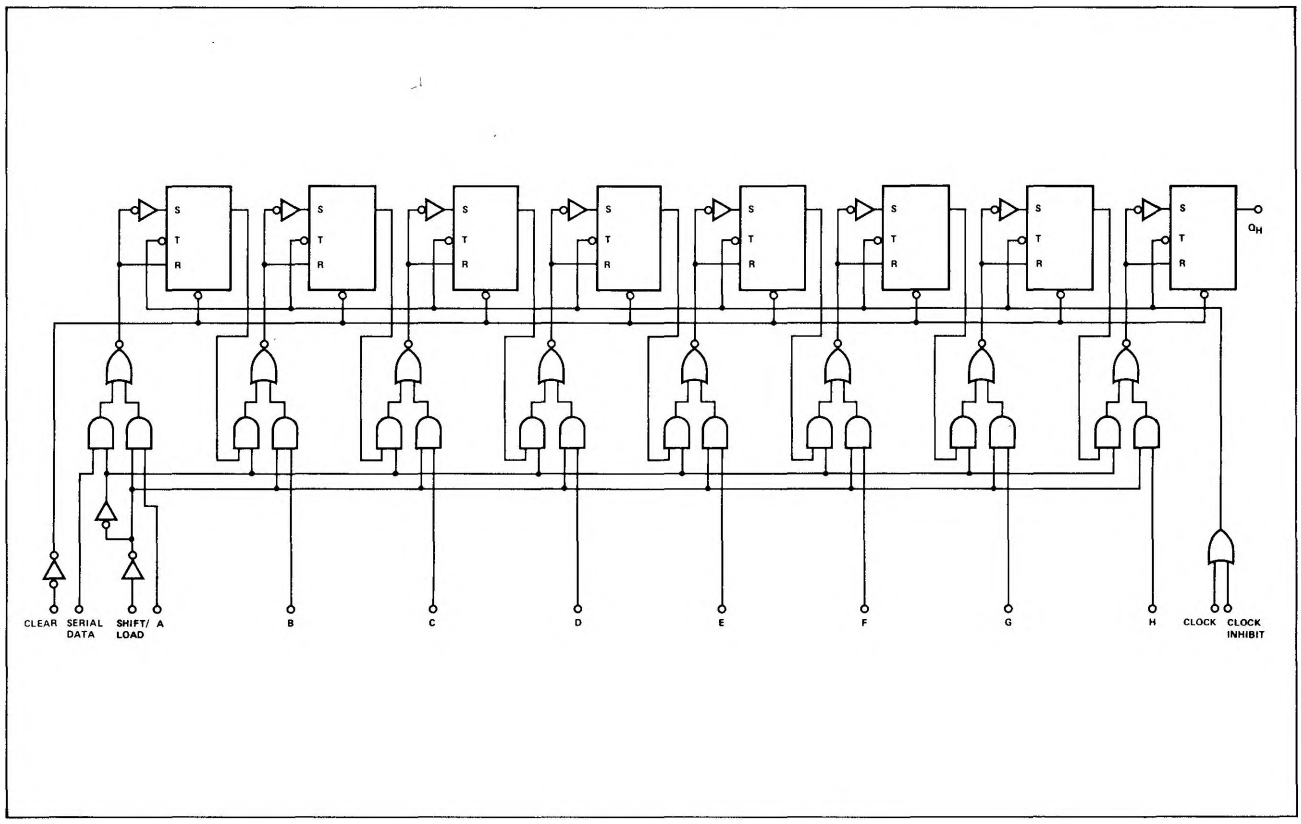
These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the gate input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock and sets all flip-flops to zero. Average power dissipation per gate is typically 4.7 mW.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54166			N74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Count Frequency, f_{count}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Mode-Control Setup Time, t_{setup}	30			30			ns
Data Setup Time, t_{setup}	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	S54166			N74166			UNIT
			MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	-20		-57	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX, Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC} (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54166, N74166	Serial Input	Clock	All other inputs