DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

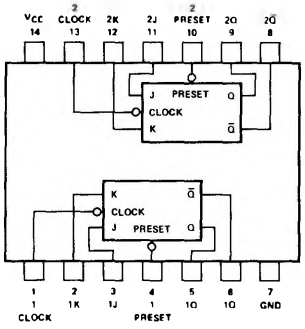
S54S113
S54S114
N74S113
N74S114

S54S113–A,F,W • S54S114–A,F,W • N74S113–A,F• N74S114–A,F

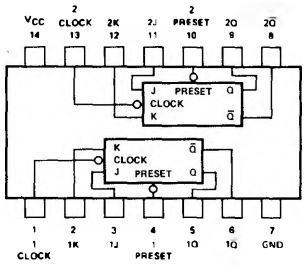
DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS

Q PACKAGE



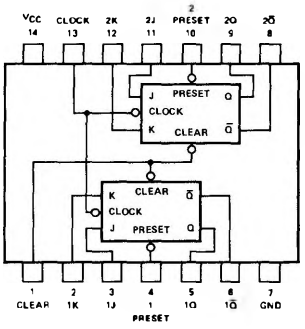
A,F PACKAGE



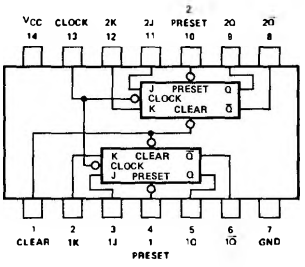
S54S113, N74S113

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



S54S114, N74S114

DESCRIPTION

The S54S113 and N74S113 offer individual J, K, preset, and clock inputs. The S54S114 and N74S114 offer common clock and common clear inputs and individual J, K, and preset inputs.

These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative-going edge of the clock pulse.

TRUTH TABLE

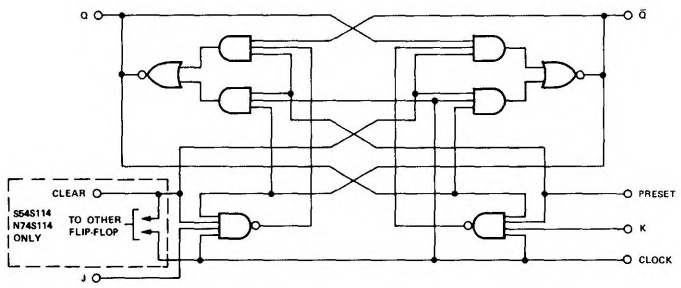
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:

A. t_n = bit time before clock pulse

B. t_{n+1} = bit time after clock pulse

LOGIC DIAGRAM (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

	S54S113, S54S114			N74S113, N74S114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		80	0		80	MHz
Width of Clock Pulse, $t_{w(clock)}$	6			6			ns
Width of Preset Pulse, $t_{w(preset)}$	8			8			ns
Width of Clear Pulse, $t_{w(clear)}$: S54S114, N74S114	8			8			ns
Input Setup Time, t_{setup}	3			3			ns
Input Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54S113 N74S113			S54S114 N74S114			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2			-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -1mA	Series 54S	2.5	3.4		2.5	3.4		V
			Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V,	I_{OL} = 20mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	J or K input			50			50	μA
			Clock			100			200	
			Preset			100			100	
			Clear						200	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	J or K input			-1.6			-1.6	mA
			Clock			-4			-8	
			Preset			-7			-7	
			Clear						-14	
I_{OS}	Short circuit output current†	V_{CC} = MAX		-40		-100	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 1		30	50		30	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF, R_L = 280Ω	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset		2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 64 through 69 of the Series 54H/74H section for test circuits.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 1: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5V.