

DESCRIPTION

These high-performance monolithic, positive-edge-triggered flip-flops utilize Schottky TTL technology to implement D-type flip-flop logic. All have a direct clear input, and the S54S175 and N74S175 feature complementary outputs from each flip-flop. Pin assignments for these Schottky flip-flops are identical to the standard TTL versions meaning that these Schottky versions can be utilized to upgrade existing system performance in most cases.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FEATURES

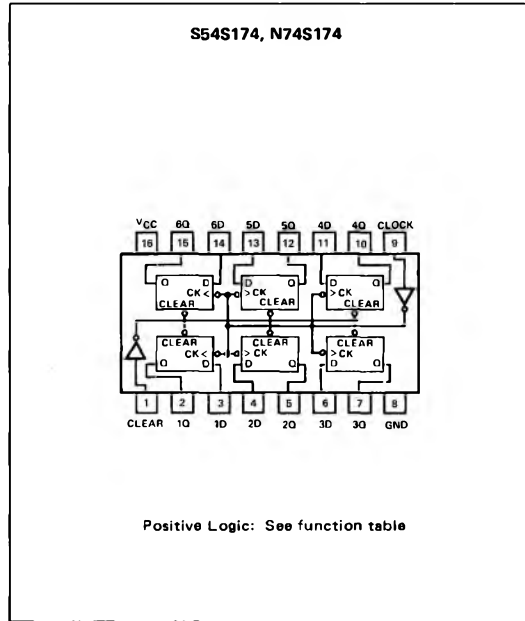
- FULL SCHOTTKY CLAMPING TO ACHIEVE TYPICAL MAXIMUM TOGGLE RATES OF 110 MHz
- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO THE SERIES 54/74 COUNTERPARTS AND CAN BE USED TO UPGRADE EXISTING SYSTEMS WITH SIGNIFICANT IMPROVEMENT IN SPEED
- FULLY COMPATIBLE WITH OTHER TTL CIRCUITS
- S54S174 AND S54S175 OPERATE OVER FULL MILITARY TEMPERATURE RANGE OF -55°C TO 125°C
- FOR USE IN HIGH-PERFORMANCE:
 - BUFFER/STORAGE REGISTERS
 - SHIFT REGISTERS
 - COUNTERS
 - PATTERN GENERATORS

FUNCTION TABLE (EACH FLIP-FLOP)

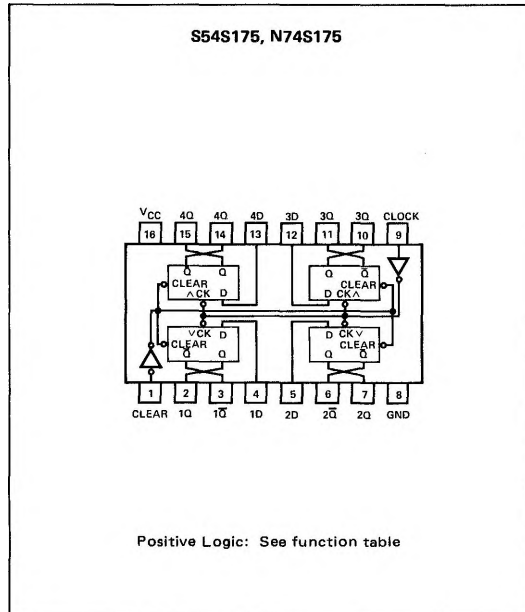
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	\bar{Q} †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

H = High level (steady state)
 L = Low level (steady state)
 X = Irrelevant
 † = Transition from low to high level
 Q_0 = The level of Q before the indicated steady-state input conditions were established
 † ≠ S54S175 and N74S175 only

PIN CONFIGURATION



PIN CONFIGURATION



DIGITAL 54/74 TTL SERIES ■ S54S174, S54S175, N74S174, N74S175

RECOMMENDED OPERATING CONDITIONS

		S54S174, S54S175			N74S174, N74S175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level	20			20			
	Low logic level	10			10			
Input clock frequency, f_{clock}		0			75			MHz
Width of clock or clear pulse, t_w		12			12			ns
Setup time, t_{setup}	Data input	8			8			ns
	Clear inactive-state	15			15			
Data hold time, t_{hold}		2			2			ns
Operating free-air temperature, T_A		-55			125			°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$				-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	Series 54S	2.5	3.4		V
			Series 74S	2.7	3.4		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$				0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				50	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$				-2	mA
I_{OS}	Short-circuit output current ‡	$V_{CC} = \text{MAX}$		-40		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 1	S54S174, N74S174	90			mA
			S54S175, N74S175	60			

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

‡ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

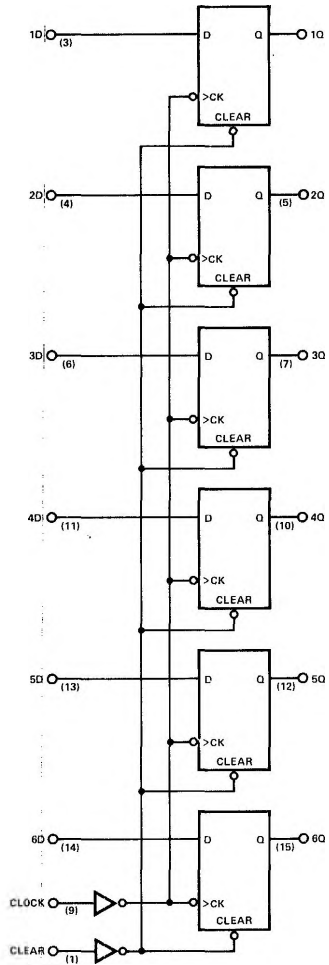
SWITCHING CHARACTERISTICS, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}, N = 10$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	$C_L = 15 \text{ pF},$ $R_L = 280 \Omega,$ See Note 2	75	110		MHz
t_{PLH}	Propagation delay time, low-to-high-level Q output from clear (S54S175, N74S175 only)			13		ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			13		ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			9		ns
t_{PHL}	Propagation time, high-to-low-level output from clock			11		ns

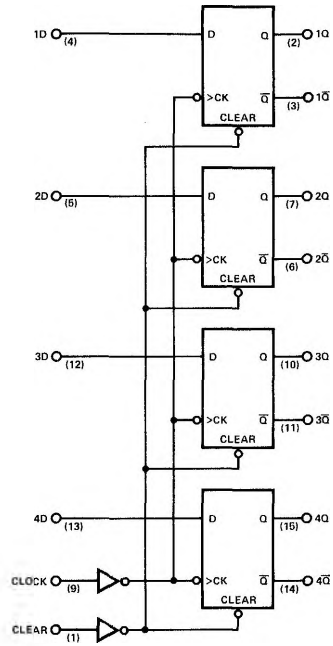
NOTE 2: See load circuit and waveforms shown on page 2-293

FUNCTIONAL BLOCK DIAGRAMS

S54S174, N74S174



S54S175, N74S175



 Dynamic input activated by a transition from a high level to a low level.