Signetics

SAA5030
Teletext Video Processor

Product Specification

Linear Products

DESCRIPTION

The SAA5030 is a monolithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext TV data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control Circuit SAA5040. A 6MHz crystal-controlled, phase-locked oscillator is incorporated which drives the Timing Chain Circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronize the timing chain.

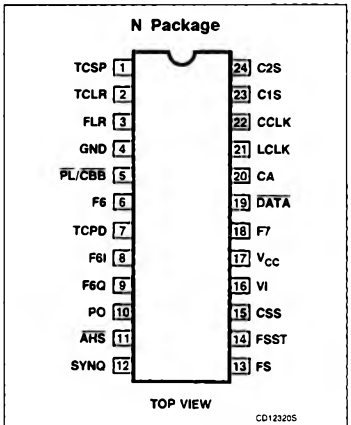
FEATURES

- **Slices digital data embedded in the composite video signal**
- **Generates a synchronized clock for the sliced data**
- **Generates a system display clock, locked with the incoming video signal**
- **On-chip signal quality detector**
- **On-chip adaptive sync separator**

APPLICATIONS

- **Teletext**
- **Data slicer**
- **Phase-locking with incoming video (when used with SAA5025D)**
- **Telecaptioning**

PIN CONFIGURATION

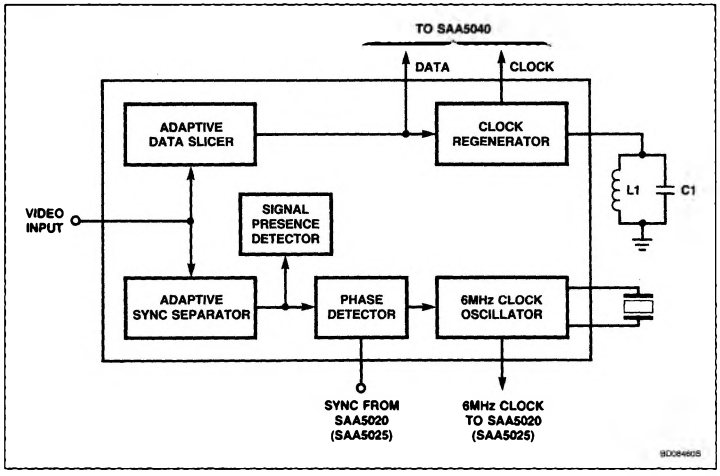


PIN NO.	SYMBOL	DESCRIPTION
1	TCSP	To signal presence time constant components
2	TCLR	Line reset time constant
3	FLR	Fast line reset output
4	GND	Ground (0V)
5	PL/$\overline{CBB}$	Sandcastle input
6	F6	6MHz output
7	TCPD	To phase detector time constant components
8	F6I	6MHz crystal oscillator input
9	F6Q	6MHz crystal oscillator output
10	PO	Picture-on input
11	$\overline{AHS}$	After-hours sync input
12	SYNQ	Sync output to TV
13	FS	Field sync output
14	FSST	Field sync separator timing
15	CSS	To sync separator capacitor
16	VI	Composite video input
17	V_{CC}	+12V supply
18	F7	Clock output
19	$\overline{DATA}$	Data output
20	CA	Clock phase capacitor
21	LCLK	Clock regenerating coil
22	CCLK	To clock pulse timing capacitor
23	C1S	Peak detector capacitor pin
24	C2S	Peak detector capacitor pin

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	−20°C to +70°C	SAA5030N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage V_{17-4}	13.2	V
V_I	Input voltages V_{5-4}	9	V
V_I	V_{10-4}	V_{CC}	V
V_I	V_{11-4}	7.5	V
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

DC AND AC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, $V_{CC} = 12V$, and with external components as shown in Figure 3, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	10.8	12.0	13.2	V
I_{CC}	Supply current (V_{CC} = 12.0V)		110		mA
Video input and sync separator					
$V_{16VIDEO(P-P)}$	Video input amplitude (sync to white); see Figure 2	2.0	1.4	3.0	V
$\|Z_S\|$	Source impedance, f = 100kHz			250	Ω
$V_{16SYNC(P-P)}$	Sync amplitude	0.07	0.7	1.0	V
t_D	Delay through sync separator		0.5		µs
t_D	Delay between field sync datum at Pin 12 and the leading edge of separated field sync at Pin 13[1] (see Figure 2)	32	48	62	µs
Field sync output					
V_{OL}	V_O (Low) (I_{13} = 20µA)			0.5	V
V_{OH}	V_O (High) ($-I_{13}$ = 100µA)	2.4			V
f_{F6}	Frequency		6.0		MHz
	Holding range	1.5	3.0		kHz
	Catching range	1.5	3.0		kHz
	Control sensitivity of phase detector measured as voltage at Pin 7 with respect to phase difference between separated syncs and phase-locked pulse $\overline{PL}$		0.3		mV/ns
	Control sensitivity of oscillator measured as change in 6MHz phase shift from Pin 8 to Pin 9 with respect to voltage at Pin 7		2		deg/mV
	Gain of sustaining amplifier, V_{9-8} measured with input voltage of 100mV_{P-P} and phase detector immobilized	2.5			V/V
	Output voltage of 6MHz signal at Pin 6, measured into 20pF load capacitance; peak-to-peak value		5.5		V
t_R, t_F	Output rise and fall times at Pin 6 into 20pF load			30	ns

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) At $T_A = 25°C$, $V_{CC} = 12V$, and with external components as shown in Figure 3, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Data slicer and clock regenerator					
	Teletext data input amplitude, Pin 16 (see Figure 2); peak-to-peak value[2]		1.1		V
	Data input amplitude at Pin 16 required to enable amplitude gate flip-flop; peak-to-peak value		0.46		V
	Attack rate, measured at Pins 23 and 24 with a step to Pin 16 (positive) (negative)		 15 9		 V/μs V/μs
	Decay rate, measured at Pins 23 and 24 with a step input to Pin 16	48	100	144	mV/μs
	Width of clock coil drive pulses from Pin 21 when clock amplitude is not being controlled[3]		40		ns
	Clock hangover measured at Pin 18 as the time the clock coil continues ringing after the end of data[4]	20			Clock Periods
	Clock and data output voltages at Pins 18 and 19 measured with 20pF load capacitance; peak-to-peak value		5.5		V
t_R, t_F	Output rise and fall times at Pins 18 and 19 into 20pF loads			30	ns
Sandcastle input					
	Sandcastle detector thresholds, Pin 5 phase-locked pulse (PL) on phase-locked pulse off blanking pulse ($\overline{CBB}$) on blanking pulse off	 2 4.5 	 	 3 5.5	 V V V V
Dual polarity sync buffer					
	After-hours sync ($\overline{AHS}$) pulse input Pin 11 threshold for $\overline{AHS}$ active threshold for $\overline{AHS}$ off	 1.0 	 	 2.0	 V V
	Picture-on (PO) input, Pin 10 threshold for PO active threshold for PO off	 1.0	 	 2.0 	 V V
	Sync output, Pin 12 $\overline{AHS}$ output with Pin 10 < 1V[5]; peak-to-peak value composite sync output with Pin 10 > 2V[5, 6]; peak-to-peak value output current	 	 0.7 0.7 	 1 3	 V V mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) At $T_A = 25°C$, $V_{CC} = 12V$, and with external components as shown in Figure 3, unless otherwise stated.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Line reset and signal presence detectors					
	Schmitt trigger threshold on Pin 2 to inhibit line reset output at Pin 3 (syncs coincident)		6.2		V
	Schmitt trigger threshold on Pin 2 to permit line reset output at Pin 3 (syncs non coincident)		7.8		V
	Line reset output V_{OL} ($I_3 = 20\mu A$)			0.5	V
	Line reset output V_{OH} ($-I_3 = 100\mu A$)	2.4			V
	Signal presence Schmitt trigger threshold on Pin 2 below which the circuit accepts the input signal		6.0		V
	Signal presence Schmitt trigger threshold on Pin 2 above which the input signal is rejected		6.3		V
Crystal-controlled, phase-locked oscillator					
	C_1		27.5		pF
	C_0		6.8		pF
	C_L		20		pF
	Trimability (C_L increased to 30pF)	750			Hz
	Fundamental ESR			50	Ω

NOTES:

1. This is measured with the dual polarity buffer external resistor connected to give negative-going syncs. The measurement is made after adjustment of the potential divider at Pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two-level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375Mbit/s. The use of odd parity for the 8-bit bytes ensures that there are never more than 14-bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into Pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive-going centered on +2.3V. With the resistor connected to the supply rail, syncs are negative-going centered on +9.7V.
6. When the composite sync is being delivered, the level is substantially the same as that at the video input.

APPLICATION DATA

The function is quoted against the corresponding pin number

1 Signal Presence Time Constant — A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2 Line Reset Time Constant — A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see Pin 3).

3 Fast Line Reset Output (FLR) — Positive-going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{CBB}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase-locked loop.

4 Ground (0V)

5 Sandcastle Input ($\overline{PL}$ and $\overline{CBB}$) — This input accepts a sandcastle waveform which is formed from $\overline{PL}$ and $\overline{CBB}$ from the timing chain SAA5020. $\overline{PL}$ is obtained by slicing the waveform at 2.5V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase-locked loop. When the loop has locked up, the edges of $\overline{PL}$ are nominally 2μs before and 2μs after the leading edge of separated line syncs.

CBB is obtained by slicing the waveform at 5V, and is used to prevent the data slicer from being offset by the color burst.

6 6MHz Output (F6) — This is the output of the crystal oscillator (see Pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7 Phase Detector Time Constant — The integrating components for the phase detector of the phase-locked loop are connected between this pin and supply.

8, 9 6MHz Crystal — A 6MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on Pin 7, which forms part of the phase-locked loop.

10 Picture On Input (PO) — The PO signal, from the acquisition and control circuits SAA5040 series, is fed to this input and is used to determine whether the input video (Pin 16) or the AHS waveform (Pin 11) appears at Pin 12.

11 After Hours Sync ($\overline{AHS}$) — A composite sync waveform $\overline{AHS}$ is generated in the timing chain circuit SAA5020 and is used to synchronize the TV (see Pin 10).

12 Sync Output to TV — The input video of $\overline{AHS}$ is available at this output dependent on whether the PO signal is High or Low. In addition, either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13 Field Sync Output (FS) — A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14 Field Sync Separator Timing — A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15 Sync Separator Capacitor — A capacitor connected to this pin forms part of the adaptive sync separator.

16 Composite Video Input (VI) — The composite video is fed to this input via a coupling capacitor.

17 Supply Voltage (+12V)

18 Clock Output — The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuits SAA5040 series via a series capacitor.

19 Data Output — The teletext data is sliced off the video waveform, squared up, and latched within the SAA5030. The latched output is fed to the acquisition and control circuits SAA5040 series via a series capacitor.

20 Clock Decoupling — A 1nF capacitor between Pin 20 and ground is required for clock decoupling.

21 Clock Regenerator Coil — A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see Pin 22).

22 Clock Pulse Timing Capacitor — Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to Pin 21. Resulting oscillations are limited and taken to the acquisition and control circuits SAA5040 series via Pin 18.

23, 24 Peak Detector Capacitors — The teletext data is sliced with an automatic data slicer, having a slicing level at the mid-point of two peak detectors working on the video signal. Storage capacitors are connected to these pins for the negative and positive peak detectors.

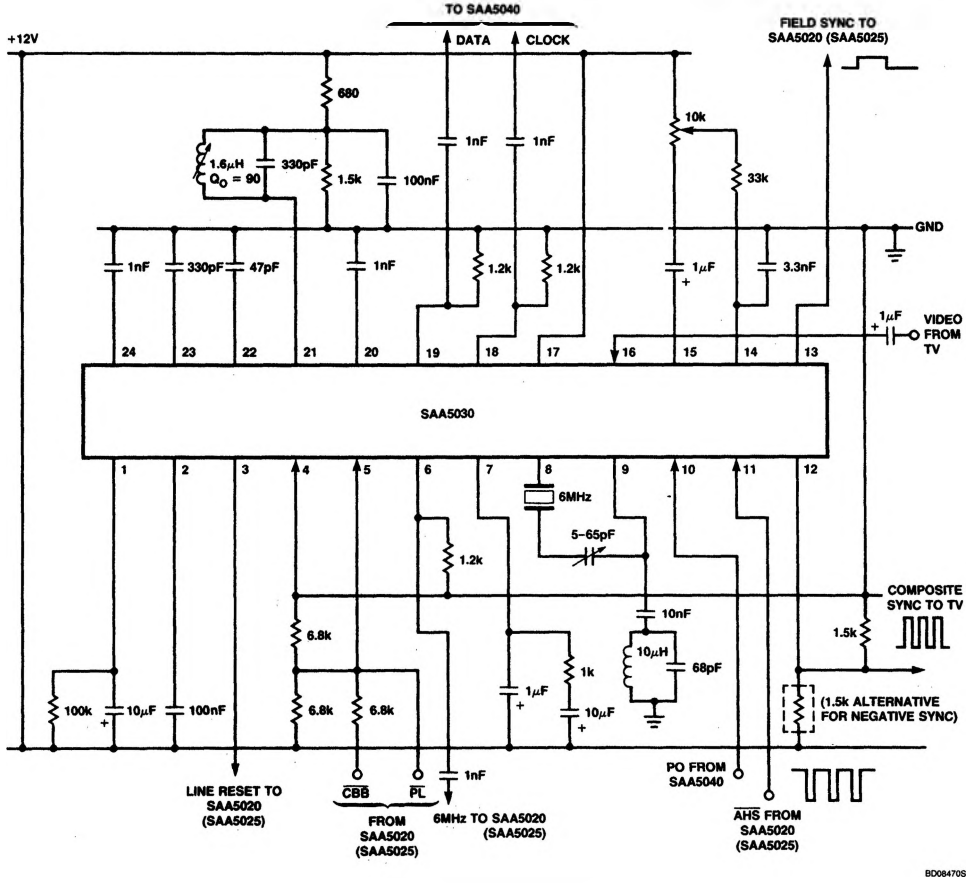


Figure 1. Peripheral Circuit

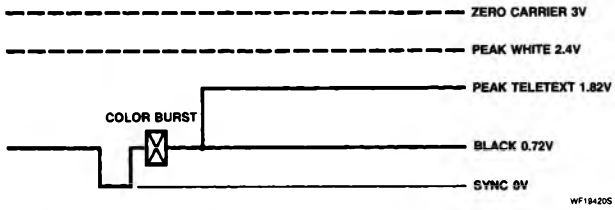


Figure 2. Part of Teletext Line, With Burst Showing Nominal Levels

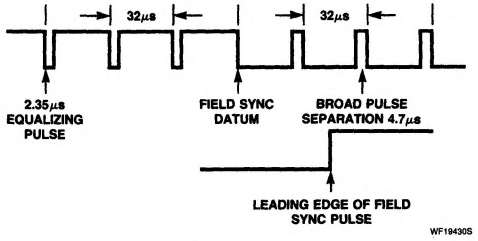


Figure 3. Details of Idealized Composite Sync Waveform