DATA SHEET

SAA7707H
Car radio Digital Signal Processor (CDSP)

Preliminary specification
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Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

1.1 Hardware

- Bitstream 3rd-order Sigma-Delta Analog-to-Digital Converters (ADCs) with anti-aliasing broadband input filters
- Digital-to-Analog Converters (DACs)with four times oversampling and noise shaping
- Digital stereo decoder
- Improved digital Interference Absorption Circuit (IAC)
- RDS processing with optional 16-bit buffer via separate channel (two-tuner radio possible)
- Auxiliary analog CD input (CD-walkman, speech, economic CD-changer, etc.)
- Two separate full I^2S-bus CD and DCC high performance interfaces
- Expandable with additional Digital Signal Processors (DSPs) for sophisticated features through an I^2S-bus gateway
- Audio output short-circuit protected
- I^2C-bus controlled
- Analog tape input
- Operating ambient temperature from −40 to +85 °C.

1.2 Software

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter and de-emphasis
- Electronic adjustments: FM/AM level, FM channel separation and Dolby level
- Baseband audio processing (treble, bass, balance, fader and volume)
- Dynamic loudness or bass boost
- Stereo one-band parametric equalizer
- Audio level meter for an automatic leveller (in combination with microcontroller)
- Tape equalization (DCC analog playback)
- Music Search detection for Tape (MSS)
- Pause detection for RDS updates
- Dolby-B tape noise reduction
- Adjustable dynamics compressor
- CD and DCC de-emphasis processing
- Signal level, noise and multi-path detection for RDS (I^2C-bus command)
- Improved AM reception.

2 APPLICATIONS

- Car radio
- Car audio systems.

3 GENERAL DESCRIPTION

The SAA7707H performs all the signal functions in front of the power amplifiers and behind the AM and FMMPX demodulation of a car radio or the tape input.
These functions are:

- Interference absorption
- Stereo decoding
- RDS decoding
- FM and AM weak signal processing (soft mute, sliding stereo, etc.)
- Dolby-B tape noise reduction
- The audio controls (volume, balance, fader, tone and dynamics compression).

Some functions have been implemented in hardware (stereo decoder, RDS decoder and IAC) and are not freely programmable. Digital audio signals from external sources with I^2S-bus formats are accepted. There are four independent analog output channels. This enables, in special system configurations, separate tone and equalization control for front and rear speakers.

The CDSP contains a basic program that enables a set with:

- AM/FM reception
- Sophisticated FM weak signal functions
- Music Search detection for Tape (MSS)
- Dolby-B tape noise reduction system
- CD play with compressor function
- Separate bass and treble tone control and fader/balance control.

For high-end sets with special and more sophisticated features, an additional Digital Signal Processor (DSP) can be connected. Examples of such features are:

- Noise-dependent volume control
- 10-band graphic equalizer
- Audio spectrum analyzer on display
- Signal delay for concert hall effects.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(tot)}$	total DC supply voltage	all supply pins	4.75	5	5.5	V
$I_{DDD(tot)}$	total DC supply current	maximum activity of the DSP; f_{xtal} = 36 MHz	–	160	200	mA
P_{tot}	total power dissipation	maximum activity of the DSP; f_{xtal} = 36 MHz	–	0.8	1.1	W
S/N	level ADC signal-to-noise ratio	RMS value; unweighted; B = 0 to 29 kHz; maximum input	48	54	–	dB
	ADC signal-to-noise ratio	not multiplexed; B = 19 kHz; V_i = 1 V (RMS)	81	85	–	dB
		multiplexed; unweighted; B = 19 kHz; 1 V (RMS)	72	76	–	dB
	ADC signal-to-noise ratio for FM-RDS	RMS value; B = 6 kHz; unweighted; f_c = 57 kHz	56	–	–	dB
V_{iFS}	ADC full-scale input voltage	V_{DDA1} = 4.75 to 5.5 V	$1.05V_{DDA1}$	$1.1V_{DDA1}$	$1.15V_{DDA1}$	V
THD	total harmonic distortion pins 62 and 71 to 75	f_i = 1 kHz; V_i = 1 V (RMS)	–	–71	–61	dB
			–	0.03	0.09	%
$V_{imc(rms)}$	maximum conversion input voltage level pins 62 and 71 to 75 (RMS value)	THD < 1%	1.1	–	–	V
RES	DAC resolution		–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio for DAC and operational amplifiers	R_L > 5 kΩ AC; R_{fb} = 2.7 kΩ; f_i = 1 kHz; R_{ref} = 18 kΩ; V_{oFS} = 2.8 V (p-p); maximum I^2S-bus signal	–	–70	–60	dB
DR	dynamic range of DAC	f_i = 1 kHz; –60 dB; A-weighted	92	102	–	dB
DS	digital silence of DAC	f_i = 20 Hz to 17 kHz; A-weighted	–	–110	–100	dB
$f_{xtalDSP}$	crystal frequency DSP part		–	36.86	–	MHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7707H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 29 × 2.8 mm	SOT318-2

6 BLOCK DIAGRAM

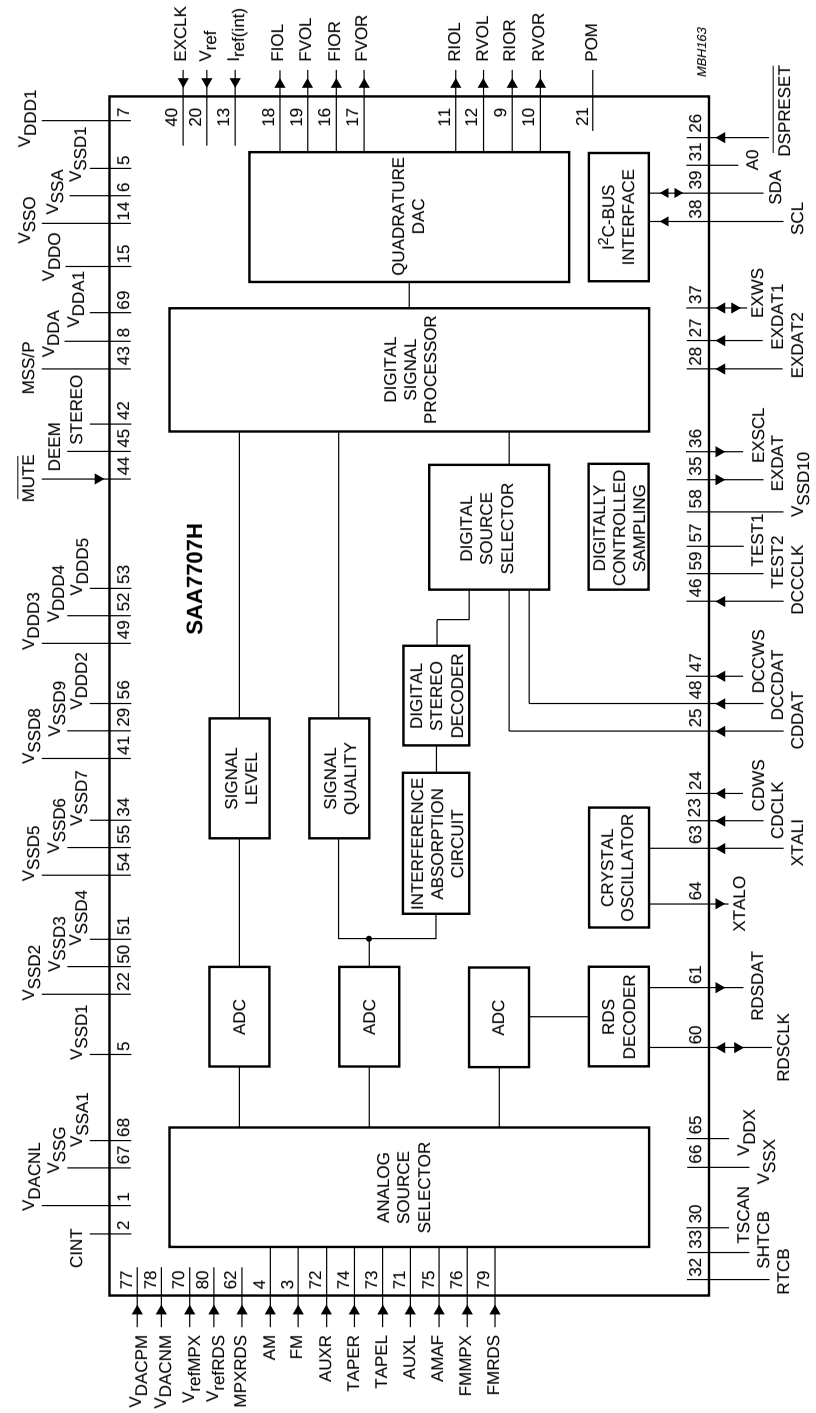


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{DACNL}	1	–	internal ground reference voltage for the level ADC
CINT	2		level ADC switch-mode integrator connector
FM	3	I	FM level input; via this pin, the level of the received FM radio signal is fed to the CDSP, the level information is required to enable correct functioning of the weak signal behaviour
AM	4	I	AM level input; via this pin, the level of the received AM radio signal is fed to the CDSP
V_{SSD1}	5	–	ground supply 1 for the DACs digital circuitry
V_{SSA}	6	–	ground supply for the DACs analog circuitry
V_{DDD1}	7	–	positive supply 1 for the DACs digital circuitry
V_{DDA}	8	–	positive supply for the DACs analog circuitry
RIOR	9	O	analog audio current output for rear right speaker
RVOR	10	O	analog audio voltage output for rear right speaker
RIOL	11	O	analog audio current output for rear left speaker
RVOL	12	O	analog audio voltage output for rear left speaker
$I_{ref(int)}$	13	I	internal reference current source input for the DACs
V_{SSO}	14	–	ground supply for DAC output operational amplifiers
V_{DDO}	15	–	positive supply for DAC output operational amplifiers
FIOR	16	O	analog audio current output for front right speaker
FVOR	17	O	analog audio voltage output for front right speaker
FIOL	18	O	analog audio current output for front left speaker
FVOL	19	O	analog audio voltage output for front left speaker
V_{ref}	20	I	voltage input for the internal reference buffer amplifier of the DAC
POM	21		activates the Power-on mute; timing is determined with an external capacitor
V_{SSD2}	22	–	ground supply 2 for the digital circuitry
CDCLK	23	I	clock input for CD digital audio source (I^2S-bus)
CDWS	24	I	Word Select input for CD digital audio source (I^2S-bus)
CDDAT	25	I	left/right data input for CD digital audio source (I^2S-bus)
$\overline{\text{DSPRESET}}$	26	I	input to reset DSP core (active LOW)
EXDAT1	27	I	external input data channel 1 (front) from extra DSP chip (I^2S-bus)
EXDAT2	28	I	external input data channel 2 (rear) from extra DSP chip (I^2S-bus)
V_{SSD9}	29	–	ground supply 9 for the digital circuitry
TSCAN	30		scan control (active HIGH)
A0	31		I^2S-bus selection for slave sub-address
RTCB	32		asynchronous reset test control block (active HIGH)
SHTCB	33		shift clock test control block (active HIGH)
V_{SSD7}	34	–	ground supply 7 for the digital circuitry
EXDAT	35	O	output data for extra external DSP chip (I^2S-bus)
EXSCL	36	O	output clock for extra external DSP chip (I^2S-bus)
EXWS	37	I/O	word select input/output for extra external DSP chip (I^2S-bus)

SYMBOL	PIN	I/O	DESCRIPTION
SCL	38	I	serial clock input (I^2C-bus)
SDA	39	I/O	serial data input/output (I^2C-bus)
EXCLK	40	I	external reference clock input to generate $4f_{as}$ and f_{as} synchronization; to be used if the I^2S-bus inputs are not suitable
V_{SSD8}	41	–	ground supply 8 for the digital circuitry
STEREO	42		FM stereo indication (active HIGH)
MSS/P	43		FM pause detector/MSS detector (active HIGH); also for IAC trigger output
$\overline{MUTE}$	44	I	MUTE input pin (active LOW); only for FM mode
DEEM	45		de-emphasis; CD and DCC (active HIGH) (I^2S-bus)
DCCCLK	46	I	DCC digital audio source clock input (I^2S-bus)
DCCWS	47	I	DCC digital audio source Word Select input (I^2S-bus)
DCCDAT	48	I	DCC digital audio source left/right data input (I^2S-bus)
V_{DDD3}	49	–	positive supply 3 for the digital circuitry
V_{SSD3}	50	–	ground supply 3 for the digital circuitry
V_{SSD4}	51	–	ground supply 4 for the digital circuitry
V_{DDD4}	52	–	positive supply 4 for the digital circuitry
V_{DDD5}	53	–	positive supply 5 for the digital circuitry
V_{SSD5}	54	–	ground supply 5 for the digital circuitry
V_{SSD6}	55	–	ground supply 6 for the digital circuitry
V_{DDD2}	56	–	positive supply 2 for the digital circuitry
TEST1	57		test pin 1 (this pin should be left open-circuit)
V_{SSD10}	58	–	ground supply 10 for the digital circuitry
TEST2	59		test pin 2 (this pin should be left open-circuit)
RDSCLK	60	I/O	radio data system bit clock input/output
RDSDAT	61	O	radio data system data output
MPXRDS	62	I	in FM mode, selects between FMMPX and RDSMPX input signal to the MPX decimation filter
XTALI	63	I	crystal oscillator input; can also be used as forced input in slave mode
XTALO	64	O	crystal oscillator output
V_{DDX}	65	–	positive supply crystal circuitry
V_{SSX}	66	–	ground supply crystal circuitry
V_{SSG}	67	–	ground guards for ADCs
V_{SSA1}	68	–	analog ground supply for ADCs
V_{DDA1}	69	–	analog positive supply for ADCs
V_{refMPX}	70	I	common mode reference voltage input for MPX ADC and buffers
AUXL	71	I	analog input for auxiliary left signal
AUXR	72	I	analog input for auxiliary right signal
TAPEL	73	I	analog input for tape left signal
TAPER	74	I	analog input for tape right signal
AMAF	75	I	analog input for AM audio frequency
FMMPX	76	I	analog input for FM multiplex signal

SYMBOL	PIN	I/O	DESCRIPTION
V_{DACPM}	77	I	supply voltage for the DACs switch capacitor of the FMMPX ADC and FMRDS ADC
V_{DACNM}	78	I	ground supply for the DACs switch capacitor of the FMMPX ADC and FMRDS ADC
FMRDS	79	I	analog FMMPX input for RDS decoding
V_{refRDS}	80	I	common mode reference voltage input for RDS ADC, level ADC and buffers

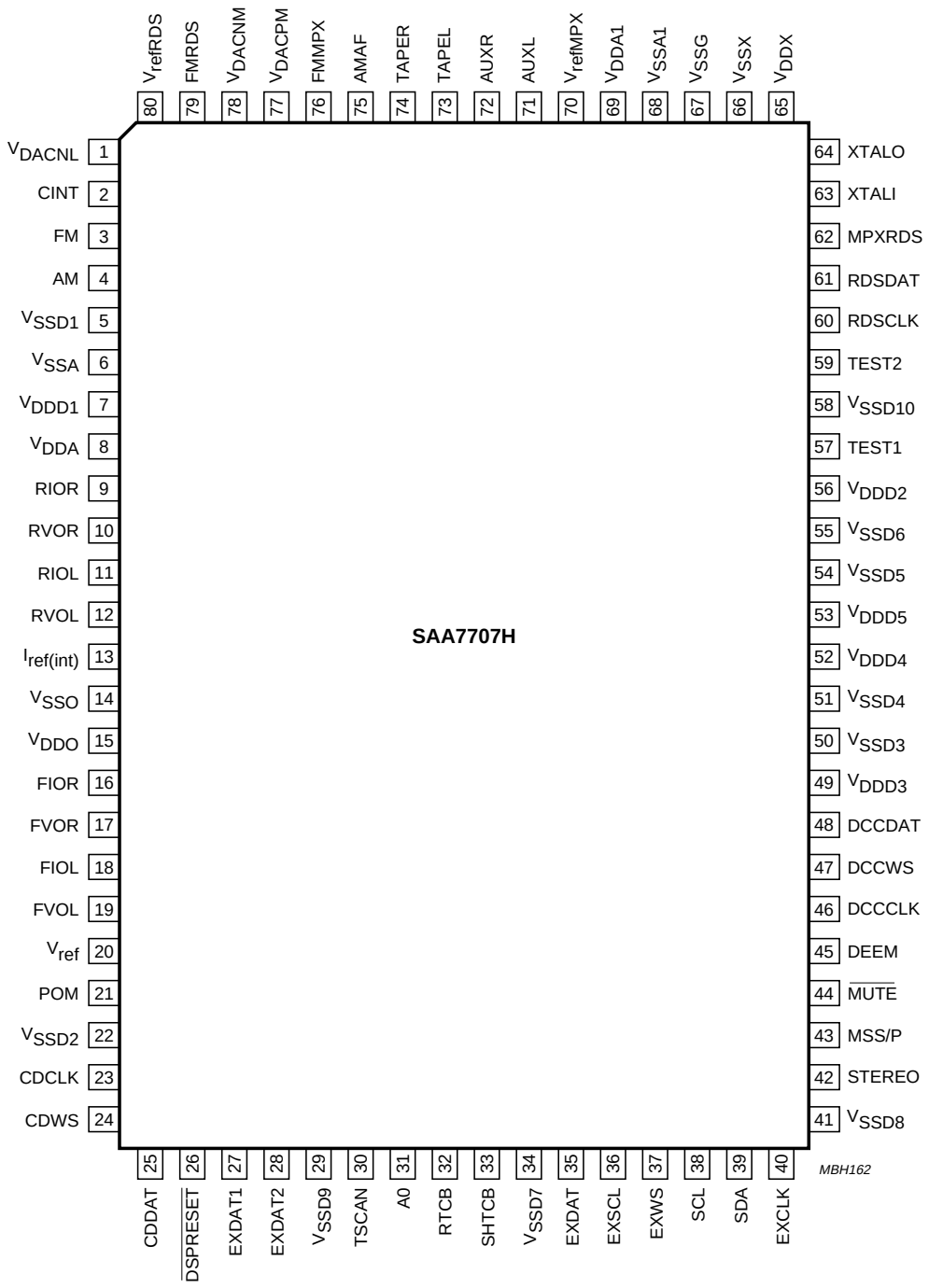


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 Signal path for level information

An FM and AM level input is implemented for FM weak signal processing [for AM, FM and RDS search purposes (absolute level and multi-path)]. A DC input signal is converted by a bitstream 1st-order Sigma-Delta analog-to-digital converter and then filtered by a decimation filter.

The input signal has to be obtained from the radio part. Two different circuits for AM and FM reception are possible:

1. A circuit with two separate input signals, one for FM level and one for AM level
2. A combined circuit with AM and FM level information on the FM level input. The AM level input can then be connected to another signal, which can be converted in the non-radio mode.

The input is selected via the input selector control register.

The input signal for level control must be in the range of 0 to 5 V. The 11-bit level ADC converts this input voltage in steps with a resolution better than 10 mV over the 5 V range. The tolerance on the gain is less than 10%.
The MSB is always logic 0, to represent a positive level.

The decimation filter reduces the bandwidth of the incoming signal to a frequency range of 0 to 29 kHz, with a resulting sampling frequency (f_s) of 76 kHz.
The response curve is illustrated in Fig.3.

The level information is sub-sampled by the DSP core to obtain a field strength and a multi-path indication. These values are stored in the coefficient or data RAM. They can be read and used in other microcontroller programs via the I^2C-bus.

8.2 Level ADC switch mode integrator (pin CINT)

The level ADC has an internal current summation point of the input level and the switch capacitor DAC. When used as an integrator, an external capacitor of 1000 pF should be connected between this pin and the analog ground at pin V_{SSA1}. The summation voltage is used as an input for the analog-to-digital comparator level.

8.3 Internal ground reference for the level ADC (pin V_{DACNL})

This pin serves as the internal ground reference for the switch capacitor DAC and the level ADC and has to be connected to the analog ground (pin V_{SSA1}).

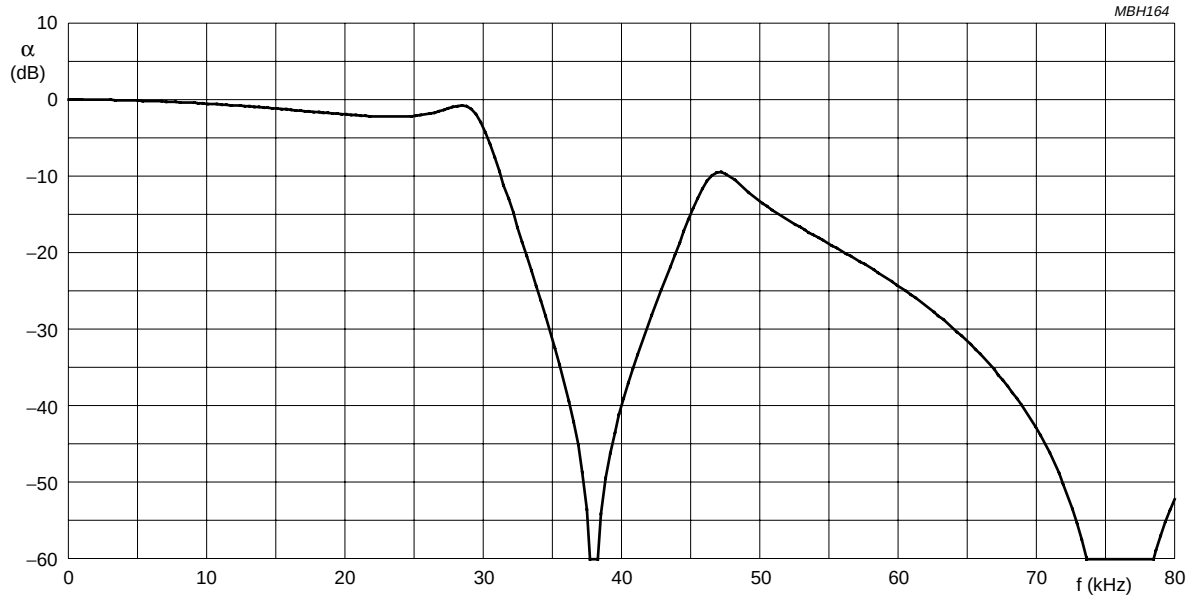


Fig.3 Frequency response of the level ADC and decimation filter.

8.4 Common mode reference voltage for RDS ADC, ADC level and buffers (pin V_{refRDS})

The middle reference voltage of the RDS ADC can be filtered via this pin. This middle reference voltage is used as a positive reference for the level ADC of the switch capacitor DAC and as half supply reference for the RDS ADC, the switch capacitor DACs and buffers. An external capacitor (connected to V_{SSA1}) prevents crosstalk between the switch capacitor DACs of the RDS ADC, level ADC and buffers, and improves the power supply rejection ratio.

8.5 Signal path for audio/MPX and stereo decoder

The SAA7707H has four analog audio source inputs; two single-multiplex channel inputs for AM and FM radio and two stereo inputs for tape and auxiliary. The auxiliary input can be used for functions such as an analog CD changer or speech applications. The stereo inputs are multiplexed so that they can share the same filters as the multiplexed FM signal. The selection between the AM, FM, TAPE and AUX input is made via the input selector control register.

The input signal behind the source selector is digitized by a bitstream 3rd-order Sigma-Delta ADC. The first decimation filter reduces the sample rate. This is followed by the sample-and-hold switch of the IAC and the 19 kHz regeneration circuit. From here, the wide-band noise detector signal HP2 (High-Pass 2) with a frequency range of 60 to 240 kHz is derived. A second decimation filter reduces the output of the IAC to a lower sample rate.

This filter has two outputs, one for the multiplex signal with a frequency range of 0 to 60 kHz (low-pass) and one for the small-band noise detector signal HP1 (High-Pass 1) with a frequency range of 60 to 120 kHz. The overall low-pass frequency response of the decimation filters is illustrated in Fig.4.

In the FM mode, the RDS ADC can be used as an input for the MPX decimation filter. This can be selected via the RDSMPX input at pin 62.

The outputs from this signal path to the DSP, which are all at a sample frequency of 38 kHz, are as follows:

- Pilot presence indication: Pilot-I. This 1-bit signal is LOW for a pilot frequency deviation of less than 4 kHz and HIGH for a pilot frequency deviation greater than 4 kHz. It is AND locked on a pilot tone.
- Pilot quality indication: Pilot-Q. This 10-bit signal contains information about the signal quality and is derived from the quadrature component of the pilot-I signal.
- ‘Left’ and ‘Right’: This is the 18-bit output of the stereo decoder after the matrix decoding. For AM reception, the ‘Right’ signal contains the AM-mono signal. For tape or auxiliary signals, the output of the stereo decoder contains sum and difference signals, but with other crosstalk properties than on FM. Therefore, a different matrix correction, as shown in Table 1, has to be applied to these signals in the DSP program. The overall frequency response of the demultiplexed signal at the output of the stereo decoder is illustrated in Fig.5.

Table 1 Overview of the signals to the CDSP

MODE	LEFT	RIGHT
AM	0	mono
FM	$\frac{1}{2}(R - L)$	$R + L$
TAPE/AUX	$\frac{1}{2}(R + L) \times 4/\pi$	$R + L$

Apart from the aforementioned theoretical response, the non-flat frequency response of the ADC must also be compensated for in the DSP program.

8.6 Mono/stereo switching

After division, the Digitally Controlled Sampling (DCS) clock generates a clock signal with a frequency which is a multiple of 19 kHz plus or minus a few Hertz. For mono reception, the DCS circuit generates a preset frequency of $n \times 19$ kHz ± 2 Hz. For stereo reception, the frequency is exactly $n \times 19$ kHz (DCS locked to $n \times$ pilot tone).
The detection of the pilot and the stereo indication is performed in the DSP program.

8.7 The automatic lock system

The VCO operates at 19 kHz ± 2 Hz exactly for no-pilot. For stereo reception, the phase error is zero for a pilot tone with a frequency of exactly 19 kHz. Therefore, no switch is required to preset the clock to 19 kHz. With auxiliary sources (tape, CD, etc.), the DCS circuit has to be preset to a fixed value.

8.8 Input sensitivity for FM

The FM input sensitivity is optimally designed for an FM front-end with an output voltage of 200 mV (RMS) at a modulation depth of 22.5 kHz of a 1 kHz tone. Due to the full-scale 1.2 V (RMS) handling capacity of the ADC, the maximum allowed modulation depth of a transmitter, for a THD of 10%, is 135 kHz. Full performance is possible for transmitters with a modulation depth of up to 110 kHz.

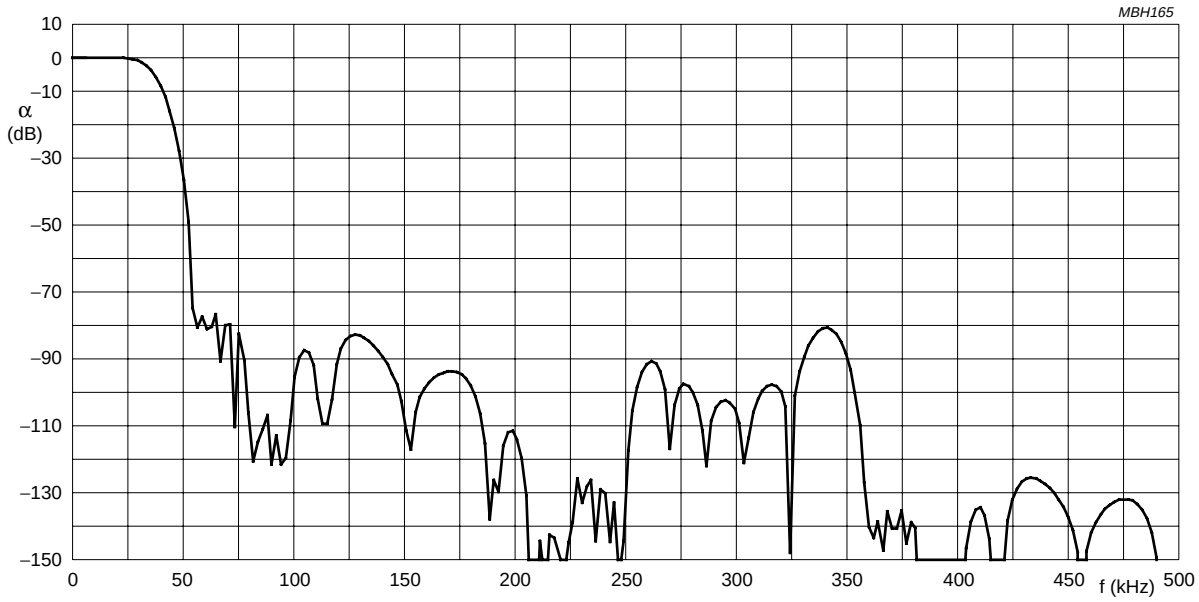


Fig.4 Overall frequency response multiplex ADC and decimation filters.

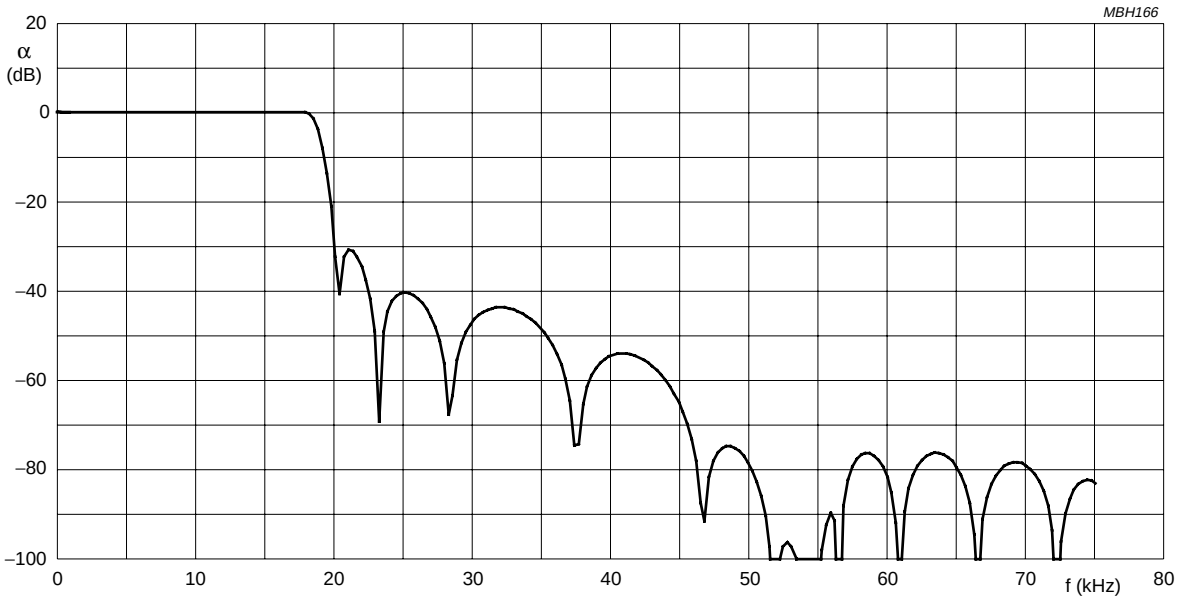


Fig.5 Transfer of MPX signal at the output of the stereo decoder.

8.9 Common mode reference voltage for MPX ADC and buffers (pin V_{refMPX})

The middle reference voltage of the MPX ADC can be filtered via this pin. This middle reference voltage is used as a half supply voltage reference for the MPX ADC, switch capacitor DACs and buffers. An external capacitor (connected to V_{SSA1}) prevents crosstalk between the switch capacitor DACs and buffers and improves the power supply rejection ratio.

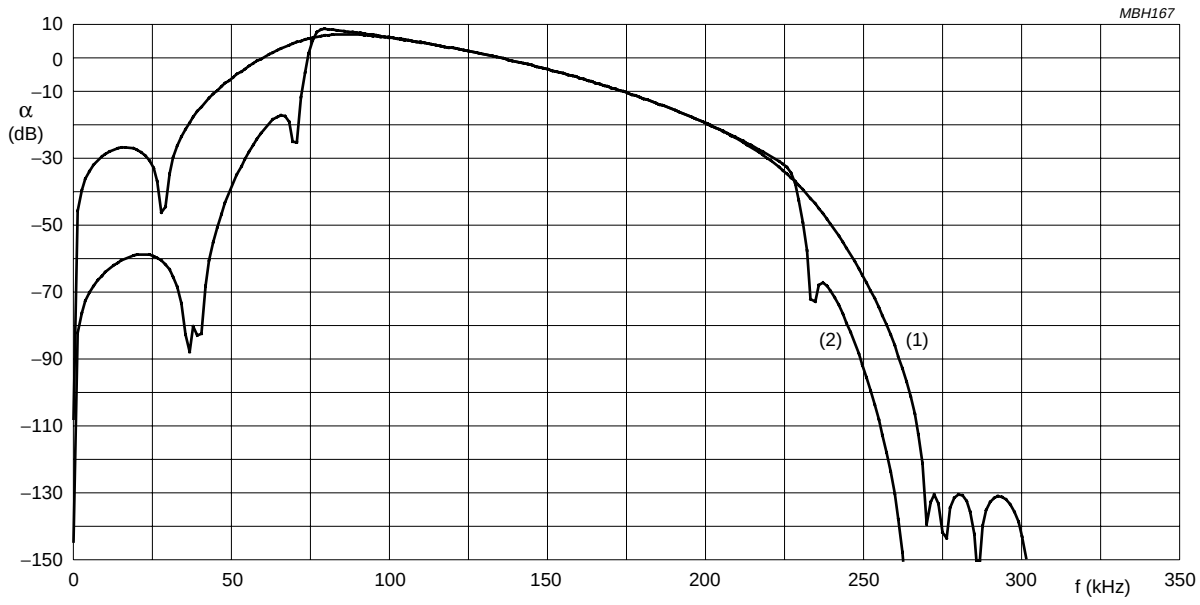
8.10 Supply voltages for the switch capacitor DACs of the FMMPX ADC and FMRDS ADC (pins V_{DACNM} and V_{DACPM})

These pins are used as ground and positive supply voltage reference for the MPX ADC, RDS ADC and the switch capacitor DACs. For optimum performance they must be connected directly to V_{SSA1} and V_{DDA1}.

8.11 Noise level

The High-Pass 1 (HP1 or narrow-band noise level filter) output of the second MPX decimation filter, in a frequency band from 60 to 120 kHz, is detected with an envelope detector and decimated to a frequency of 38 kHz.

The response time of the detector is 100 ms.
Another option is the High-Pass 2 (HP2 or wide-band noise level filter). This output from the first MPX decimation filter is in a frequency band from 60 to 240 kHz. It has the same properties as the HP1 and is also decimated to 38 kHz. Which signal is used (HP1 or HP2) is determined by the input selector control register. The noise level can be detected and filtered in the DSP core and can be used to optimize the FM weak-signal processing. The transfer curves of both filters before decimation are illustrated in Fig.6.



(1) Narrow-band noise level filter.
(2) Wide-band noise level filter.

Fig.6 Frequency response of noise level before decimation.

8.12 TAPE/AUX de-multiplex

The auxiliary and tape inputs also use the stereo decoder. Because of this, the left and right channels are multiplexed with a 38 kHz square wave to obtain a signal similar to the FM multiplexed signal. Auxiliary inputs can be e.g. TV-sound, remote players (tape deck, CD-changer with analog output etc.). The signal-to-noise ratio from such sources is limited by the ADC in the SAA7707H (>75 dB). The decimation filter of the ADC attenuates the harmonic signals from this stereo encoder. For an optimum channel separation, the 38 kHz switch signal has to be phase corrected to compensate for the delay of the ADC and decimation filters. This can be adjusted with the 3-bit group delay compensation in the IAC control register. Signal frequencies above 19 kHz at the input of the multiplexer are converted to the audio base-band and are therefore not allowed.

8.13 Signal-to-noise considerations

Due to the pre-emphasis of FM broadcasts, the theoretical signal-to-noise ratio is approximately 3 dB higher for FM stereo in comparison with multiplexed inputs.

To avoid aliasing into the tape channel, the tape noise from the pre-amplifier must be attenuated before analog-to-digital conversion with a 1st-order 10 kHz low-pass filter. The frequency response is equalized after the stereo decoder in the DSP program before the Dolby decoder software. Using this filter, the signal-to-noise ratio of this channel is degraded by 3 dB. This results in a signal-to-noise ratio that is overall 6 dB lower than a tape input with respect to FM stereo.

8.14 Channel separation correction

The channel separation is approximately 50 dB at 1 kHz and 35 dB at 15 kHz. Because the frequency response of the ADC has some deviation from the flat curve around 38 kHz, a perfect channel separation cannot be obtained. Therefore, the de-multiplexed signal is corrected for crosstalk in the DSP program.

8.15 Input selection switches

A schematic diagram of the input selection is illustrated in Fig.5. The input selection is controlled by bits in the input selector control register. The relationship between these bits and the switches is indicated in Table 2.

Table 2 Analog input selection

I^2C-BUS SELECTION BIT			SWITCH			
AM/FM	AUX/ RADIO	TAPE/ AUX	SFM	SAM	SAUX	SAUX
0	0	x	1	0	0	0
1	0	x	0	1	0	0
x	1	0	0	0	1	0
x	1	1	0	0	0	1

8.16 Analog inputs supply

The analog input circuit has its own separate power supply connections to allow maximum filtering. These pins are V_{SSA1} for the analog ground and V_{DDA1} for the analog power supply. V_{SSG} is the connection to the guard ring which isolates the analog part from the digital filters. This pin has to be connected to the analog ground.

8.17 Digitally controlled sampling clock (DCS)

The crystal clock generates a continuous clock signal for the internal DSP core. In the radio mode, the stereo decoder, the RDS decoder, the ADCs and the level decimation filters have to run synchronously with the 19 kHz pilot. Therefore, a clock signal with a controlled frequency with a multiple of 19 kHz (9.728 MHz = 512 $\times$ 19 kHz) is required.

In the SAA7707H, the patented method of a non-continuous digitally controlled sampling clock has been implemented. A frequency of 9.728 MHz is generated by a special dividing mechanism of the master crystal clock. Since the dividing mechanism is fixed, only a crystal frequency of 36.86 MHz can be used.

The DCS system is controlled by up/down information from the stereo decoder. For mono transmissions, the DCS clock is still controlled by the stereo decoder loop. The output keeps the DCS free-running at a multiple frequency of 19 kHz $\pm$2 Hz. In TAPE/AUX and AM mode, the DCS clock must always be put in preset mode by the input selector control register.

8.18 Survey of the DCS clock settings in different modes

The DCS clock behaves as shown in Table 3.

Table 3 DCS clock/mode

MODE	DCS CLOCK
FM stereo	locked on 19 kHz pilot of received FM signal
FM mono	free running
AM analog inputs TAPE/AUX	fixed preset
I^2C-bus inputs DCC/CD	fixed preset

8.19 Synchronization with the core

A 38 kHz synchronization signal is derived from the DCS clock and divided by 256.

If the external I^2S-bus DCC CD is selected, the rising edge of the Word Select input signal is used to synchronize with the core.

8.20 Interference absorption circuit

The Interference Absorption Circuit (IAC) detects and suppresses ignition interference. This hardware IAC is a modified and digital version of the analog circuit that has already been in use for many years.

The input signal to the IAC circuit is derived from the output signal of the decimation filter. The interference detector analyses the high frequency content of this MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic-like algorithm and is based on probability calculations. This logic will send appropriate pulses to an MPX mute switch.

At Power-on, the nominal setting for an IAC with good performance characteristics is selected (all IAC control bits are 0). If an adjustment is needed, the characteristics can be adapted as described in the application manual.

8.21 IAC testing

The internal IAC trigger signal is visible on the MSS/P pin (pin 43) if the IAC trigger output bit of the IAC control register is set. In this mode, the effect of the parameter settings on the IAC performance can be verified.

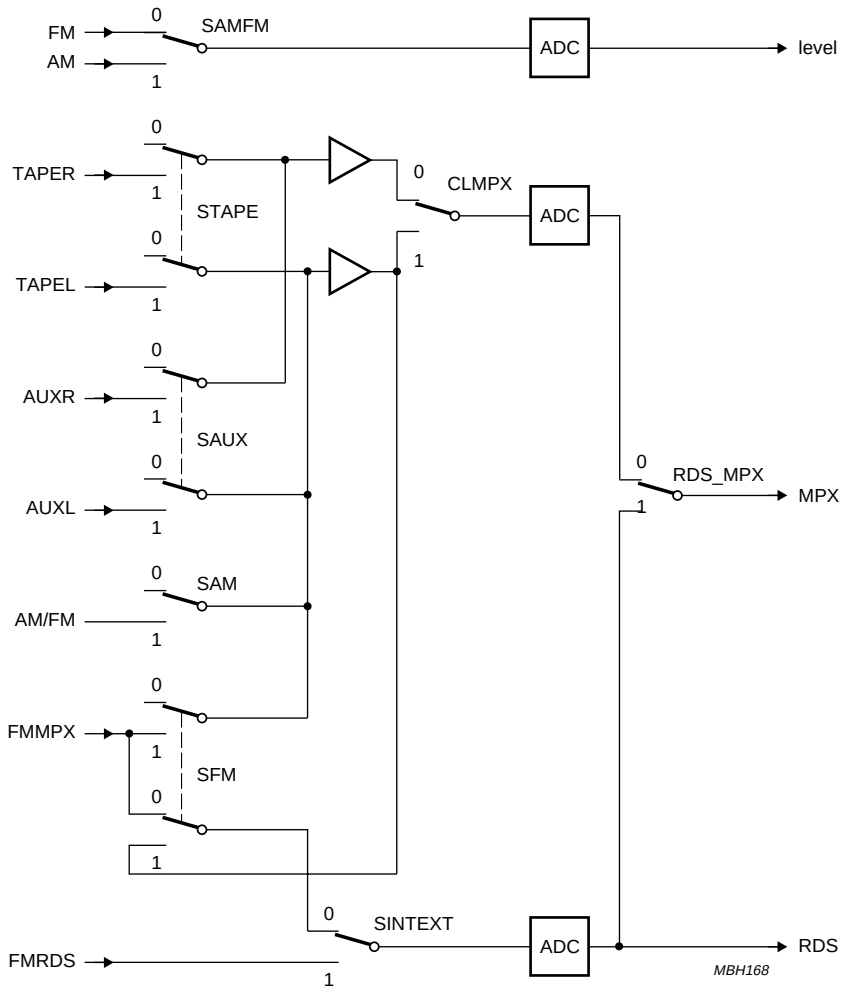


Fig.7 Schematic diagram of input selection.

- The SAMFM switch is controlled by the SEL-LEV-AM/FM bit
- The SINTEXT switch is controlled by the SEL-RDS-EXT/INT bit
- The CLMPX switch is controlled by the 38 kHz clock derived from the DCS, but is not active in FM and AM mode.

In the FM radio mode, the MPXRDS pin overrides the following switches when set to logic HIGH:

If SEL-AM/FM = 0 and SEL-AUX/RADIO = 0 and pin MPXRDS = 1, then SFM = 0, SINTEXT = 1 and MPXRDS = 1.

9 ANALOG OUTPUTS

9.1 Digital-to-analog converters

Each of the four low-noise high dynamic range DACs consists of a 15-bit signed magnitude DAC with current output, followed by a buffer operational amplifier.

The five higher bits (bits 10 to 14) are used to control the total coarse current ratio of the 32 coarse current sources via a thermometer decoder. The nine lower bits (bits 1 to 9) are derived from a 512 transistor matrix, which acts as a passive 9-bit current divider for one of the coarse currents. The MSB (bit 15) is used as a sign bit for the signed magnitude converter and controls the direction of the total output current. A separate converter is used for each of the four audio output channels. The value of each coarse current is adjusted by the current through the external resistor connected to pin 13 ($I_{ref(int)}$).

Each converter output is connected to the inverting input of one of the four internal CMOS operational amplifiers. The non-inverting input of this operational amplifier is connected to the internal reference voltage. Together with an external resistor, the current-to-audio output voltage conversion is achieved.

9.2 Upsample filter

To reduce spectral components above the audio band, a fixed 4 times oversampling and interpolating 18-bit digital IIR filter is used. It is realized as a bit serial design and consists of two consecutive filters. The data path in these filters is 22 bits, to prevent overflow and to maintain a theoretical signal-to-noise ratio greater than 105 dB. The filters give an attenuation of at least 29 dB. The filter is followed by a 5 bit 1st-order noise shaper, to expand the dynamic range to more than 105 dB.

The band around multiples of the sample frequency of the DAC ($4f_{as}$) is not affected by the digital filter. A capacitor can be added in parallel with the output resistor at the DAC output to further attenuate this out-of-band noise to an acceptable level.

The overall frequency spectrum at the DAC audio output without external capacitor/low-pass filter for the audio sampling frequencies (f_{as}) of 38 kHz is illustrated in Fig.8. The detailed spectrum around f_{as} is illustrated in Fig.9 for an f_{as} of 38 kHz, 44.1 kHz and 48 kHz. The pass-band bandwidth (at –3 dB) is $\frac{1}{2}f_{as}$.

The word clock for the upsample filter ($4f_{as}$) is derived from the audio source timing. If the internal audio source is selected, the sample frequency is fixed at 38 kHz.

For external digital sources (DCC and CD), a sample frequency from 32 to 48 kHz is possible. The sample frequency is automatically adjusted to the I²S-bus input by dividing the external bit clock. This clock is normally present in a DCC CD application. An internal digital PLL divides this clock with the integer factor needed to obtain the $4f_{as}$ word clock. Master synchronization of this divided clock signal is obtained with a reset of the divider on the Word Select signal (trailing edge) of the I²S-bus.

In the application, the I²S-bus signal from the external source should fulfil the following requirements:

- There is a continuous (is part of the basic I²S-bus specification) $n \times 4f_{as}$ ($4 < n < 128$) I²S-bus bit clock or
- If the I²S-bus bit clock is not continuous, another $n \times 4f_{as}$ ($4 < n < 128$) continuous clock signal has to be connected to the EXCLK pin (pin 40). The divide external clock mode has to be selected using the input selector control register.

The range of the internal 7-stage programmable divider of the PLL, to obtain $4f_{as}$, is large enough to handle 16-bit I²S-bus signals as well as master clocks up to 22 MHz from digital sources (CD, DCC, R-DAT and EBU interface) without any clock regeneration.

The PLL is used in a free-running mode to ensure that jitter on the I²S-bus signals (due to asynchronous clocking of the I²S-bus signals by the DSP core) will not influence the total harmonic distortion of the audio signal on the analog DAC part. This will, however, only operate if there is no jitter on the bit clock or when a crystal clock is used.

9.3 Volume control

The total volume control has a dynamic range of more than 100 dB. With the signed magnitude noise-shaped 15-bit DAC and the internal 18 bit registers of the DSP core, a useful digital volume control range of 100 dB is possible by calculating the corresponding coefficients. The step size is freely programmable and an additional analog volume control is not needed in this design. The signal-to-noise ratio of the audio output, at full-scale, is determined by the total 15 bits of the converter.

The noise at low outputs is fully determined by the noise performance of the DAC. Since it is a signed magnitude type, the noise at digital silence is also low.
The disadvantage is that the total THD is higher than conventional DACs. The typical signal and noise levels as a function of the output level and the typical signal-to-noise plus THD as a function of the output level are illustrated in Fig.10.

9.4 Power-on mute

To avoid any uncontrolled noise at the audio outputs after Power-on of the IC, the reference current source of the DAC is switched off. The capacitor connected to pin 21 (POM) determines the time after which this current has a soft switch-on. Consequently, at Power-on, the current audio signal outputs are always muted. The voltage output signals will show a small jump at switch-on due to the asymmetrical voltage supply of the output operational amplifiers. These types of disturbances must be eliminated via the application set-up. The output has to be set to digital silence before the POM pin is at logic HIGH. This is achieved via the DSP program control and/or a zero volume setting. The pin is internally connected to V_{DDO} with a high-ohmic resistor.

9.5 Power-off plop suppression

To avoid plops in a power amplifier, the supply voltage of the analog part of the DAC can be fed via a Schottky diode and an extra capacitor. In this situation, the output voltage will decrease gradually, allowing the power amplifier some extra time to switch off without audible plops.

9.6 Internal reference buffer amplifier of the DAC (pin V_{ref})

Using two internal resistors, half of the supply voltage (V_{DDO}) is obtained and coupled to an internal buffer. This reference voltage is used as a DC voltage for the output operational amplifiers and as a reference voltage for the DAC. In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground.

9.7 Internal DAC current reference

As a reference for the current at the DAC current source, a current is drawn from pin 13 ($I_{ref(int)}$) to the V_{SSO} ground. The voltage at this pin is $\frac{1}{2}V_{DDO}$ (typically 2.5 V). The maximum DAC current is equal to 4.5 times this current. When a reference resistor of 18 kΩ is used, the reference current from the DAC is 125 μA. This results in a peak current from the four current outputs of $4.5 \times 125 = 562.5$ μA.

9.8 Analog outputs supply

For an optimum signal-to-noise performance, supply ripple rejection and to suppress switch-off plops, the output operational amplifiers, the analog part of the DACs and the upsample filter plus digital part have separate power supply connections.

The operational amplifiers have the V_{SSO} and V_{DDO} pins as ground and positive supply. These pins also provide the supply for the reference circuits. The analog DAC part uses the V_{SSA} and V_{DDA} pins as ground and positive supply. The upsample filter and digital part of the DAC share the V_{SSD1} and V_{DDD1} as ground and positive supply connections.

9.9 Clock circuit and oscillator

The SAA7707H has an on-board crystal clock oscillator. The schematic of this Pierce oscillator is illustrated in Fig.11. The active element needed to compensate for the loss resistance of the crystal is the block ‘Gm’. This block is placed between the XTAL (output) and the OSC (sense) pins. The gain of the oscillator is internally controlled by the AGC block; this prevents excessive power loss in the crystal. The higher harmonics are then as low as possible.

The signal on the XTAL pin is amplified and divided by two. This 18.43 MHz signal is then used as the DSP clock signal (PH2). For the high frequency, as used in the SAA7707H, normally only third overtone crystals are available. With an external LC notch filter at the fundamental frequency, oscillation at this frequency can be avoided.The crystal frequency is chosen in such a way that the harmonics are outside the normal FM band. The crystal frequency used is 36.86 MHz.

9.10 Crystal oscillator supply

The power supply connections for the oscillator are separate from the other supply lines. This is to minimize the feedback from the ground bounce of the chip to the oscillator circuit. The V_{SSX} pin (pin 66) is used as ground supply and the V_{DDX} pin (pin 65) as positive supply.

9.11 External control pins

For external control, two input pins have been implemented. The status of these pins can be changed by applying a logic level, and is recorded in the internal status register. The functions of each pin are as follows:

- $\overline{\text{MUTE}}$ (pin 44). Mute input (0 = $\overline{\text{MUTE}}$)
- DEEM (pin 45). This pin activates the de-emphasis for CD and DCC. (1 = de-emphasis on).

To control external devices, two output pins are implemented. The status of these pins is controlled by the DSP program. The functions of each pin are as follows:

- STEREO (pin 42): Indicates whether an FM broadcast is in stereo (1 = stereo)
- MSS/P (pin 43): Indicates a pause in FM or tape search mode (1 = pause). This is also the IAC trigger output for IAC alignment if the corresponding I^2C-bus bit is set.

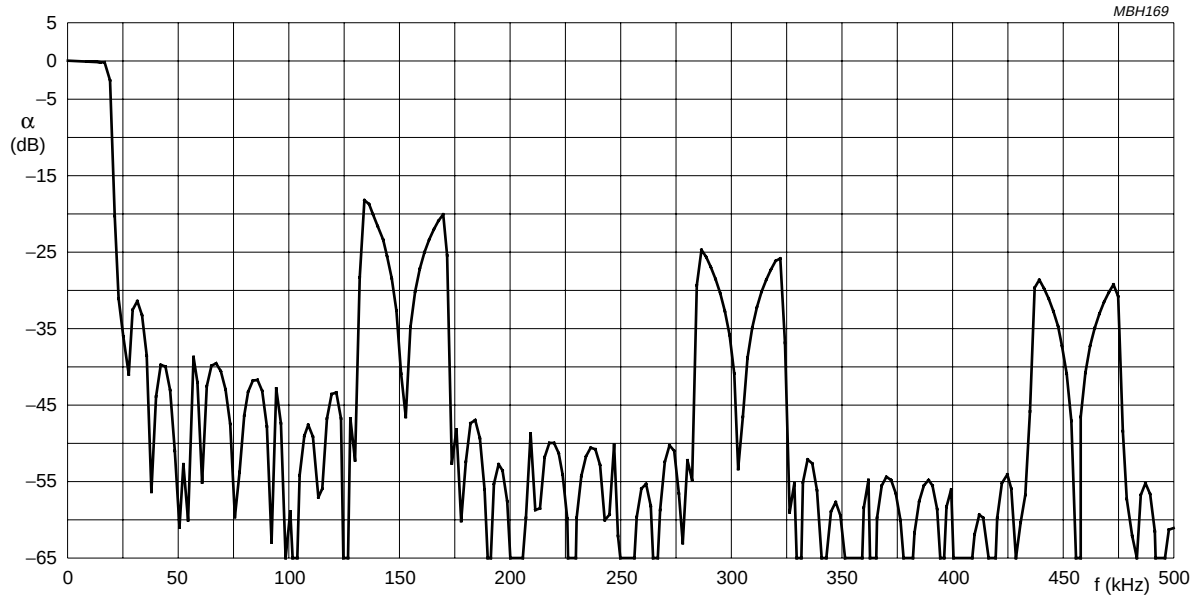


Fig.8 Overall frequency spectrum audio output (f_{as} = 38 kHz).

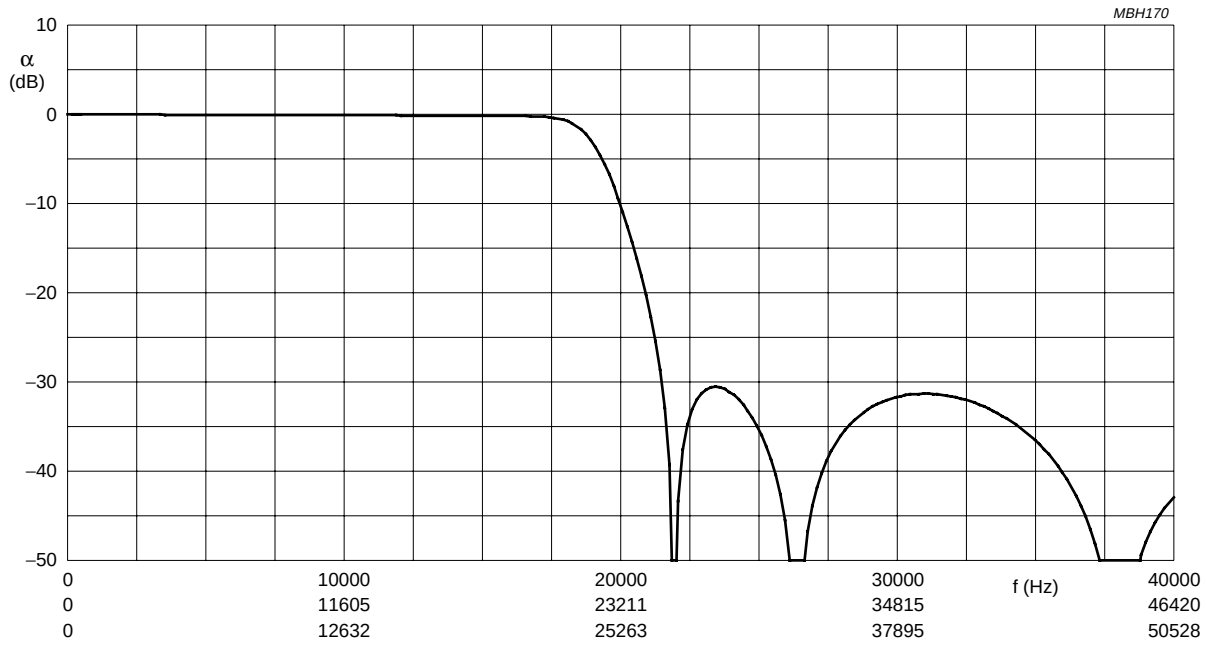
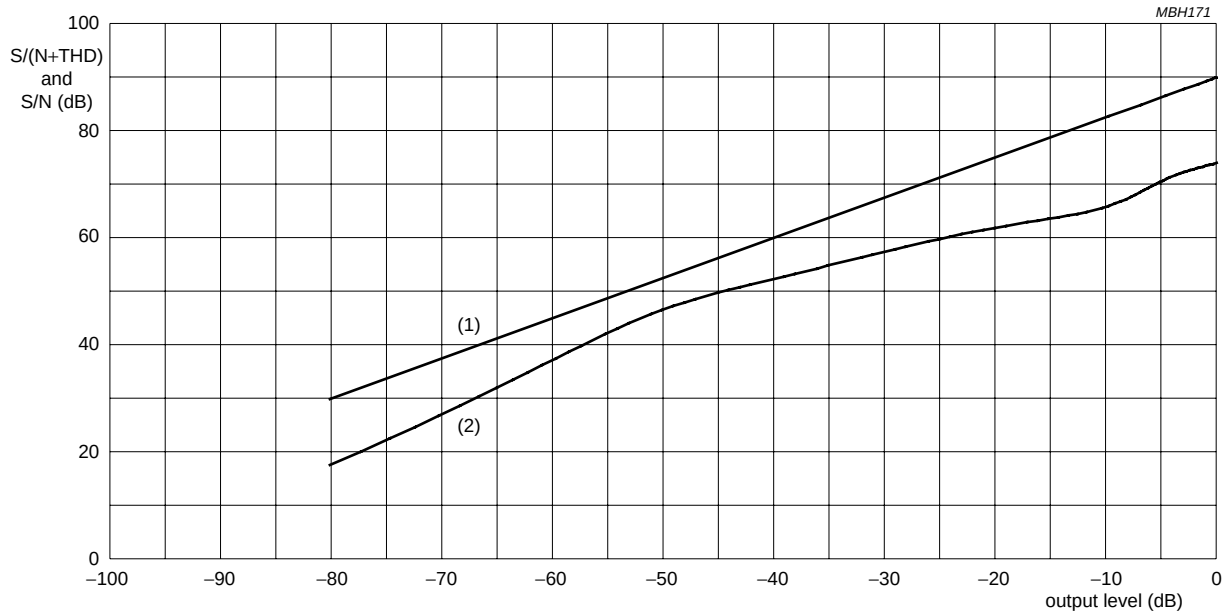


Fig.9 Detailed frequency spectrum of audio output.



(1) Signal-to-noise.
(2) Signal-to-noise + total harmonic distortion.

Fig.10 Typical signal-to-noise level and signal-to-noise plus THD as a function of output level.

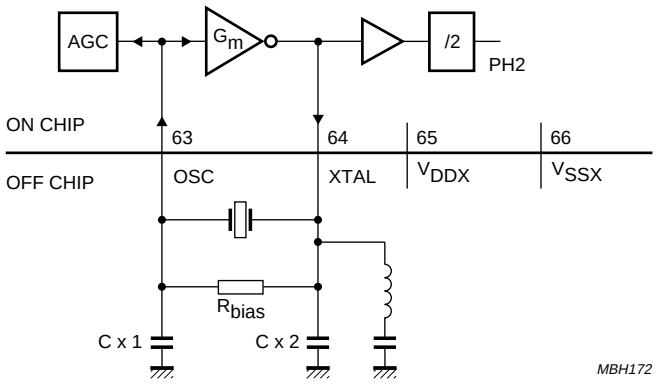


Fig.11 Schematic diagram of the oscillator circuit.

10 I²S-BUS DESCRIPTION

10.1 I²C-bus control (pins SCL and SDA)

For external control of the SAA7707H, a standard I²C-bus is implemented. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multi-path etc.)
- Instructions controlling the DATA flow, such as source selection, IAC control and clock speed.

10.2 I²S-bus description

For communication with external digital sources and/or additional external processors, the I²S-bus digital interface is used. It is a serial 3-line bus, having one line for Serial Data (SD), one line for Serial Clock (SCK) and one line for the Word Select (WS). For external processors, the CDSP acts as a master transmitter; for external digital sources the CDSP acts as a slave. The communication with the external processor and external digital sources are separated, to allow both features at the same time.

Figure 12 shows an extract of the Philips I²S-bus specification interface report regarding the general timing and format of the I²S-bus. Word select logic 0 means left channel word; word select logic 1 means right channel word.

The serial data is transmitted in twos complement with the MSB first. One clock period after the negative edge of the Word Select line, the MSB of the left channel is transmitted. Data is synchronized with the negative edge of the clock and latched at the positive edge.

As inputs from an external processor for the four audio channels, two data lines have been implemented.

10.3 Communication with external digital audio sources (DCC + CD-WS/CL/Data pins)

For communication with external digital audio sources, two additional I²S-bus inputs are available. They each have clock, data and Word Select input lines with a maximum useful data length of 18 bits. The external source is master and supplies the clock. The input selection and port selection is controllable via the input selector control register. The DSP program is synchronized with the external source via the Word Select signal.

The input allows a variety of clock frequencies, sample frequencies and word lengths.

The Word Select line automatically determines the SAA7707H sampling frequency.

Using the Digital Source Selector (see Fig.1), one of the three possible input sources is selected. The selected audio data channels are input to two 18-bit wide memory mapped I/O registers of the DSP named Input Left and Input Right.

Except for the $4f_{as}$ pulse to control the upsample filter (see Section 9.2), other synchronization signals such as internal Word Select are derived from the I²S-bus input signals.

The input bit clock is used as a bit clock for the external processor. As a consequence, a clock pulse input signal with less than 18 bits will result in a communication with an external processor of the same number of bits. In this event, the trailing bits of the 18-bit input registers will be zero.

If the I²S-bus driver outputs of the external digital source ICs have 3-state outputs, they can all be connected on one single I²S-bus input.

10.4 Communication with external processors and other devices (EXWS/CL/EXDAT1 and EXDAT2)

For communication with external processors, delay lines or other I²S-bus controllable devices, a complete dual-channel 18-bit output bus is implemented.

The SAA7707H acts as the master transmitter and the external device has to be synchronized with the Word Select line.

As input for the processed data, two data input lines have been implemented that are processed synchronously with the data output to the external processor (see Table 4). This enables, in total, a feedback of two stereo audio channels.

For this communication, the DSP core has the following 18-bit memory mapped I/O registers available:

Table 4 DSP core I/O registers

INPUT	OUTPUT
EXDAT1 left/right	EXDAT left/right
EXDAT2 left/right	

The DSP program moves data from the two external I²S-bus data output registers to the external processor and reads it back from the two or four external I²S-bus data input registers. The hardware of the bus can be enabled by the input control register.

To minimise electro magnetic interference (EMI), the output has to be disabled if the output is not used.

The timing diagram of the communication is illustrated in Fig.13.

10.5 Relationship between external input and external output

The stereo decoder output has an internal I^2S-bus format with 32 clock pulses per channel for 18 valid and 14 zero data bits. Providing that the stereo decoder output is used, the communication with the external processor will also have 32 clock pulses per channel for 18 valid and 14 zero data bits.

When an external digital source is selected, the number of valid bits and clock pulses of this source determines the output to the external processor. This relationship is shown in Table 5.

Table 5 Relationship between external input and external output.

INPUT CLOCK BITS	INPUT DATA BITS	OUTPUT CLOCK BITS	OUTPUT DATA BITS
>32	≥18	32	18
≥18 and ≤32	≥18	as input	18
≥18 and ≤32	<18	as input	18
<18	<18	as input	as input

10.6 RDS decoder (RDSCLK and RDSDAT)

The RDS decoder recovers the additional inaudible RDS information transmitted by FM radio broadcasting. The (buffered) data is provided as an output for further processing by a suitable decoder. The operational functions of the decoder are in accordance with EBU specification *EN 50067*.

The RDS decoder has three different functions:

1. Clock and data recovery from the MPX signal
2. Buffering of 16 bits, if selected
3. Interfacing with the microcontroller.

10.7 Clock and data recovery

The RDS chain has a separate input. This enables RDS updates during tape play and also the use of a second receiver for monitoring the RDS information of signals from another transmitter (double tuner concept).

In this way, it can be performed without interruption of the audio program. The MPX signal from the main tuner of the car radio can be connected to this RDS input via the built-in source selector.

The input selection is controlled by the input selector control register.

For FM stereo reception, the clock of the total chip is locked to the stereo pilot (19 kHz multiple). For FM mono, the DCS loop keeps the DCS clock around the same 19 kHz multiple. In all other cases, such as AM reception or tape, the DCS circuit has to be set to a preset position. Under these conditions, the RDS system is always clocked by the DCS clock in a 38 kHz (4×9.5 kHz) based sequence.

10.8 Timing of clock and data signals

The timing of the clock and data output is derived from the incoming data signal. Under stable conditions, the data will remain valid for 400 μs after the clock transition.
The timing of the data change is 100 μs before a positive clock change. This timing is suitable for positive and negative triggered interrupts on a microcontroller.
The RDS timing is illustrated in Fig.14.

During poor reception, it is possible that errors in phase may occur. Consequently the duty cycle of the clock and data signals will vary from a minimum of 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, errors in phase do not occur on a cyclic basis.

10.9 Buffering of RDS data

The repetition frequency of RDS data is approximately 1187 Hz. This results in an interrupt on the microcontroller every 842 μs. In a second mode, the RDS interface has a double 16-bit buffer.

10.10 Buffer interface

The RDS interface buffers 16 data bits. Each time 16 bits are received, the data line is pulled down and the buffer is overwritten. The control microcontroller has to monitor the input data line at least every 13.5 ms. This mode is selected by the input selector control register.
The interface signals from the RDS decoder and the microcontroller in the buffer mode are illustrated in Fig.15. When the buffer is filled with 16 bits, the data line is pulled down.

The data line will remain LOW until reading from the buffer is started, by pulling down the clock line. The first data bit is clocked out.

After 16 clock pulses, the buffer is read and the data line is set HIGH until the buffer is filled again. The microcontroller stops communication by pulling the clock line HIGH.

The data is written out just after the clock HIGH-to-LOW transition. The data is valid when the clock is HIGH.

When a new 16-bit buffer is filled before the other buffer is read from, that buffer will be overwritten and the old data will be lost.

10.11 $\overline{\text{DSP}}$ reset

The reset pin ($\overline{\text{DSP}}$) is active LOW and has an internal pull-up resistor. To allow a proper switch-on of the supply voltage, a capacitor should be connected between this pin (pin 26) and V_{SSD}. The value of the capacitor is such that the SAA7707H will remain in reset as long as the power supply is not stabilized. A more or less fixed relationship between the $\overline{\text{DSP}}$ reset and the POM (pin 21) time constant is obligatory. The voltage on the POM pin determines the current flowing in the DACs. At 0 V (at pin 21), the DAC currents are zero and therefore the DACs output voltages are also zero. At 5 V, the DAC currents are at their nominal (maximum) value.

Long before the DAC outputs reach their nominal output voltages, the DSP must be in the working mode (to reset the output register) therefore, the $\overline{\text{DSP}}$ time constant must be shorter than the POM time constant. For advised capacitors, see Figs. 24 and 25.

The $\overline{\text{DSP}}$ reset has the following functions:

- The bits of the IAC control register are set to logic 0
- The bits of the input selector control register are set to logic 0
- The program counter is set to address $0000.

When the level on the $\overline{\text{DSP}}$ is at logic HIGH, the $\overline{\text{DSP}}$ program starts to run.

10.12 Power supply connection and EMC

The digital part of the SAA7707H has 5 positive supply lines (V_{DDD1} to V_{DDD5}) and 10 ground connections (V_{SSD1} to V_{SSD10}). To minimize radiation, the SAA7707H should be put on a double-layer PCB with, on one side, a large ground plane. The ground supply lines should have a short connection to this ground plane. A coil/capacitor network in the positive supply line can be used as a high frequency filter.

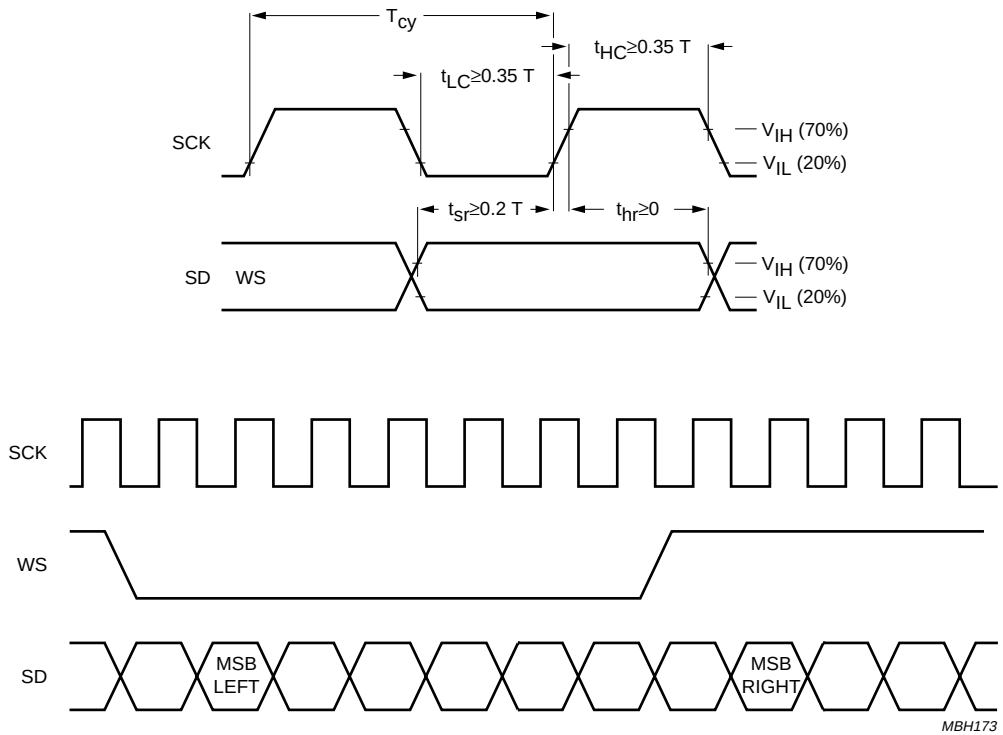


Fig.12 I^2S-bus timing and format.

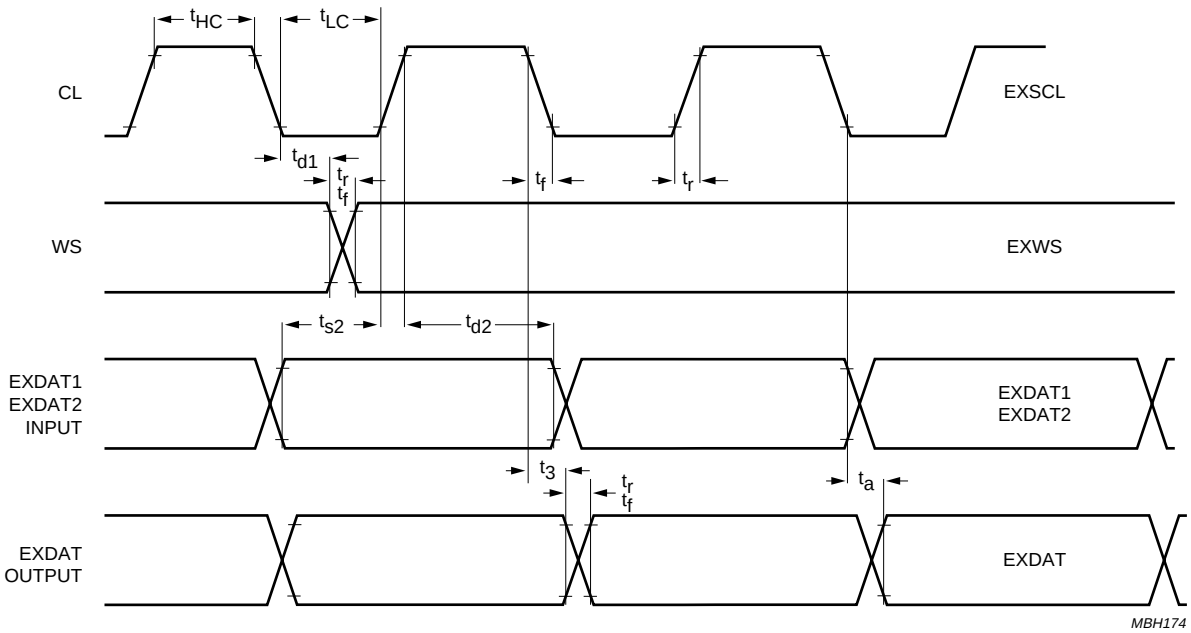


Fig.13 Timing diagram of the CDSP to external processor.

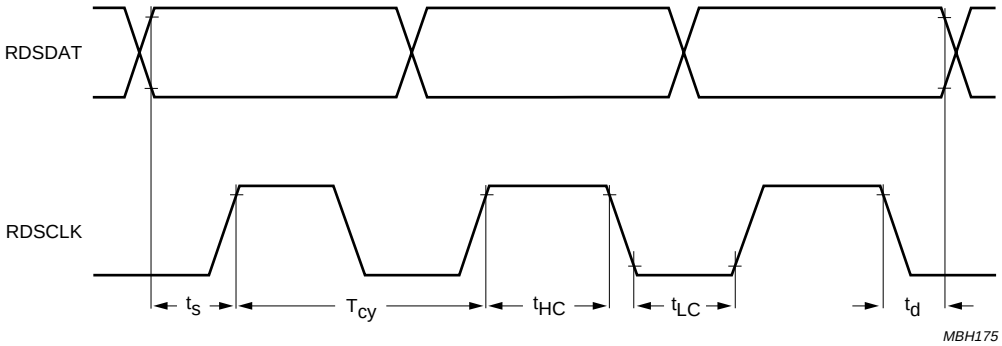


Fig.14 RDS timing diagram in direct output mode.

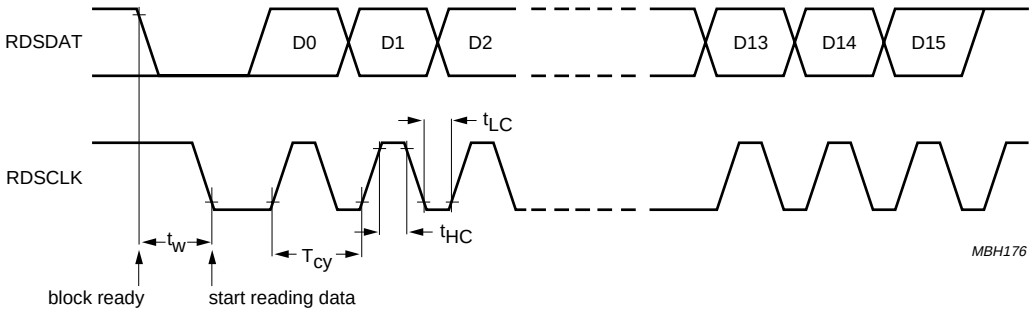


Fig.15 Interface signals RDS decoder and microcontroller.

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	DC supply voltage		–0.5	+6.5	V
ΔV_{DDD}	voltage difference between any two V_{DDX} pins		–	550	mV
I_{IK}	DC input clamp diode current	$V_I < -0.5$ V or $V_I > V_{DDD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamp diode current	output type 4 mA; $V_O < -0.5$ V or $V_O > V_{DDD} + 0.5$ V	–	±20	mA
I_O	DC output sink or source current	output type 4 mA; -0.5 V $< V_O < V_{DDD} + 0.5$ V	–	±20	mA
I_{DDD}	DC supply current per pin		–	±50	mA
I_{SSD}	DC ground supply current per pin		–	±50	mA
LTCH	latch-up protection	CIC specification/test method	100	–	mA
P_o	power dissipation per output		–	100	mW
P_{tot}	total power dissipation		–	1600	mW
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
V_{ESD}	electrostatic handling for all pins	note 1	3000	–	V
		note 2	300	–	V

Notes

1. Human body model: C = 100 pF; R = 1500 Ω; 3 pulses positive plus 3 pulses negative.
2. Machine model: C = 200 pF; L = 2.5 μH; R = 25 Ω; 3 pulses positive plus 3 pulses negative.

12 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air and V_{SSD} lead fingers 50, 51, 54 and 55 of the QFP80 soldered to a PCB copper plate of 36 cm^2	35	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air and V_{SSD} lead fingers 50, 51, 54 and 55 of the QFP80 not connected to a PCB copper plate	42	K/W

13 DC CHARACTERISTICS

V_{DDD} = 4.75 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part						
DIGITAL INPUTS AND OUTPUTS; NOTE 1						
$V_{DDD(tot)}$	total DC supply voltage	all V_{DDD} pins	4.75	5.0	5.5	V
$I_{DDD(tot)}$	total DC supply current	maximum activity of the DSP; f_{xtal} = 36 MHz	–	160	200	mA
P_{tot}	total power dissipation	maximum activity of the DSP; f_{xtal} = 36 MHz	–	0.8	1.1	W
V_{IH}	HIGH level input voltage; pins 23 to 25, 27, 28, 30 to 33, 38 to 40, 44 to 48, 60 and 62		$0.7V_{DDD}$	–	–	V
	HIGH level input voltage; pin 26		$0.8V_{DDD}$	–	–	V
V_{IL}	LOW level input voltage; pins 23 to 28, 30 to 33, 38 to 40, 44 to 48, 60 and 62		–	–	$0.2V_{DDD}$	V
V_{hys}	hysteresis voltage pin 26		–	$0.33V_{DDD}$	–	V
V_{OH}	HIGH level output voltage; pins 23, 35 to 37, 42, 43, 48, 57, 60 and 61	V_{DDD} = 4.75 V; I_O = –4 mA	4.25	–	–	V
V_{OL}	LOW level output voltage; pins 23, 35 to 37, 39, 42, 43, 48, 57, 60 and 61	V_{DDD} = 4.75 V; I_O = 4 mA	–	–	0.5	V
I_{LI}	input leakage current; pins 24, 25, 27, 28, 38 and 44 to 47	V_I = 0 or V_{DDD}	–	–	±1	µA
$\lvert I_{OZ} \rvert$	3-state output leakage current; pins 23, 35 to 37, 39, 42, 48, 57 and 60	V_O = 0 or V_{DDD}	–	–	±5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{pu}	internal pull-up resistor to V_{DDD} pin 26		17	–	134	kΩ
R_{pd}	internal pull-down resistor to V_{SSD} pins 30 to 33, 40 and 62	$V_i = V_{DDD}$	17	–	134	kΩ
t_r	input rise time	V_{DDD} = 5.5 V	–	6	200	ns
t_f	input fall time	V_{DDD} = 5.5 V	–	6	200	ns
t_r	output rise time for LOW-to-HIGH transition	V_{DDD} = 4.75 V; T_{amb} = 85 °C; pins 23, 48 and 60	–	–	1.43 + 0.24C_L	ns
		V_{DDD} = 4.75 V; T_{amb} = 85 °C; pins 43 and 61	–	–	4.75 + 0.28C_L	ns
		V_{DDD} = 4.75 V; T_{amb} = 85 °C; pins 35 to 37, 42 and 57	–	–	4.75 + 0.28C_L	ns
		V_{DDD} = 5.5 V; T_{amb} = −40 °C; pins 23, 48 and 60	0.351 + 0.097C_L	–	–	ns
		V_{DDD} = 5.5 V; T_{amb} = −40 °C; pins 43 and 61	1.302 + 0.101C_L	–	–	ns
		V_{DDD} = 5.5 V; T_{amb} = −40 °C; pins 35 to 37, 42 and 57	1.302 + 0.101C_L	–	–	ns
t_f	output fall time for HIGH-to-LOW transition	V_{DDD} = 4.75 V; T_{amb} = 85 °C; pins 23, 48 and 60	–	–	1.82 + 0.31C_L	ns
		V_{DDD} = 4.75 V; T_{amb} = 85 °C; pins 43 and 61	–	–	6.44 + 0.36C_L	ns
		V_{DDD} = 4.75 V; T_{amb} = 85 °C; pins 35 to 37, 42 and 57	–	–	6.44 + 0.36C_L	ns
		V_{DDD} = 5.5 V; T_{amb} = −40 °C; pins 23, 48 and 60	0.386 + 0.097C_L	–	–	ns
		V_{DDD} = 5.5 V; T_{amb} = −40 °C; pins 43 and 61	0.971 + 0.115C_L	–	–	ns
		V_{DDD} = 5.5 V; T_{amb} = −40 °C; pins 35 to 37, 42 and 57	0.971 + 0.115C_L	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
ANALOG INPUTS: V_{DDA1} = 5 V; T_{amb} = 25 °C						
V_{DDA1}	analog supply voltage for ADC		4.75	5.0	5.5	V
V_{refMPX}	common mode reference voltage MPX ADC pin 70	with respect to pins 68 and 69	$0.47V_{DDA1}$	$0.5V_{DDA1}$	$0.53V_{DDA1}$	V
V_{refRDS}	common mode reference voltage RDS ADC pin 80	with respect to pins 68 and 69	$0.47V_{DDA1}$	$0.5V_{DDA1}$	$0.53V_{DDA1}$	V
Z_O	output impedance at pins 70 and 80		–	600	–	Ω
V_{DACPM}	positive reference voltage for MPX ADC and RDS ADC		4.75	5.0	5.5	V
I_{VDACPM}	positive reference current for MPX ADC		–	–20	–	µA
V_{DACNM}	negative reference voltage for MPX ADC and RDS ADC		–0.3	0	+0.3	V
I_{VDACNM}	negative reference current MPX ADC		–	20	–	µA
V_{DACNL}	negative reference voltage level A/D		–0.3	0	+0.3	V
I_{VDACNL}	negative reference current for level ADC		–	5	–	µA
V_{IosMPX}	input offset voltage MPX		–	140	–	mV
V_{IosRDS}	input offset voltage RDS		–	140	–	mV
ANALOG OUTPUTS: $V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V; T_{amb} = 25 °C						
V_{DDD1}	digital supply voltage for upsample filter and digital DAC		4.75	5.0	5.5	V
V_{DDA1}	analog supply voltage for DAC		4.75	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage		4.75	5.0	5.5	V
V_{ref}	input voltage on pin 20	with respect to pins 14 and 15	$0.47V_{DDO}$	$0.5V_{DDO}$	$0.53V_{DDO}$	V
Z_{15-20}	impedance between pins 15 and 20		12	18	25	kΩ
Z_{14-20}	impedance between pins 14 and 20		12	18	25	kΩ
V_{13}	input voltage on pin 13	with respect to pins 14 and 15	$0.46V_{DDA}$	$0.5V_{DDA}$	$0.54V_{DDA}$	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{O(DAC;\ max)}$	maximum output current from DACs	reference resistance to pin 14 = 18 kΩ	490	570	650	μA
$V_{O(os)}$	DC offset voltage at DAC output	with respect to pin 20	–	5	–	mV
$V_{O(rms)}$	AC output voltage of operational amplifier outputs at maximum signal pins 10, 12, 17 and 19 (RMS value)	R_L > 5 kΩ; R_{fb} = 2.7 kΩ; note 2	0.94	1.09	1.24	V
$V_{O(av)}$	average DC output voltage at pins 10, 12, 17 and 19	R_L > 5 kΩ; R_{fb} = 2.7 kΩ; note 2	2.25	2.5	2.75	V
R_{POM}	pull-up resistor to pin 15		64	128	260	kΩ
Crystal oscillator: T_{amb} = 25 °C						
$V_{DD(osc)}$	oscillator supply voltage		4.75	5.0	5.5	V
Current per supply pin or pin group: T_{amb} = 25 °C; V_{DD} = 5 V (typ.); 5.5 V (max.)						
I_{DDD1}	digital supply current DACs pin 7		–	20	50	μA
I_{DDA}	analog supply current DAC pin 8		–	4	8	mA
I_{DDO}	supply current for operational amplifiers pin 15	no load	–	2	4	mA
I_{DDD}	supply current for digital circuitry and periphery pins 49, 52, 53 and 56		–	137.5	165	mA
I_{DDX}	supply current for crystal circuit pin 65		–	1.5	3	mA
I_{DDA1}	supply current for ADCs pin 69		–	15	20	mA

Notes

1. The values for the capitative load C_L are given in pF.
2. R_L is the AC impedance of the external circuitry at 1 kHz, connected to the audio outputs in the application. There is also no DC current flowing through R_L.

14 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog DC inputs (LEVEL-FM, AM): $V_{DDD} = V_{DDA1} = 5$ V; $T_{amb} = 25$ °C						
S/N	signal-to-noise ratio ADC	RMS value; not weighted; B = 0 to 29 kHz; maximum input	48	54	–	dB
		RMS value; not weighted; audio mode; B = 0 to 19 kHz; maximum input	52	58	–	dB
R_i	input resistance		200	400	–	kΩ
V_{FS}	full-scale input voltage	V_{DDA1} = 4.75 to 5.5 V	$1.05V_{DDA1}$	$1.1V_{DDA1}$	$1.15V_{DDA1}$	V
$V_{I(os)}$	DC offset voltage at minimum input voltage	with respect to V_{DACNL}	–	–	60	mV
V_{iADR}	input voltage level	R_{ext} = 5 kΩ	–0.3	–	+7.5	V
α	decimation filter attenuation		20	–	–	dB/Dec
f_{co}	pass-band cut-off frequency	at –3 dB	–	29	–	kHz
f_{sr}	sample rate after decimation	radio mode	–	38	76	kHz
		audio mode	–	38	76	kHz
Analog AC inputs: pins MPX, AM, TAPE and AUX						
$V_{i(con, rms)}$	maximum conversion input voltage level (RMS value)	THD < 1%	1.1	–	–	V
R_i	input resistance		48	60	72	kΩ
THD	total harmonic distortion	f_i = 1 kHz; V_i = 1 V (RMS)	–	–71	–61	dB
		f_i = 1 kHz; V_i = 1 V (RMS)	–	0.03	0.09	%
S/N_{ADC}	signal-to-noise ratio for ADC	not multiplexed; B = 19 kHz; V_i = 1 V (RMS)	81	85	–	dB
		multiplexed; unweighted; B = 19 kHz; V_i = 1 V (RMS)	72	76	–	dB
S/N_{AM}	signal-to-noise ratio for AM	B = 5 kHz; V_i = 200 mV (RMS); (M = 30%)	68	72	–	dB
$S/N_{FM(mon)}$	signal-to-noise-ratio for FM mono	V_i = 200 mV (RMS); (Δf = 22.5 kHz); B = 19 kHz; unweighted; (M = 30%)	69	72	–	dB
$S/N_{FM(st)}$	signal-to-noise-ratio for FM stereo	V_i = 200 mV (RMS); (Δf = 22.5 kHz); B = 19 kHz; unweighted; (M = 30%)	60	63	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N_{TAPE}	signal-to-noise-ratio for TAPE (+10 kHz RC)	B = 19 kHz; V_i = 1 V (RMS); unweighted	70	74	–	dB
S/N_{AUX}	signal-to-noise-ratio for AUX	B = 19 kHz; V_i = 1 V (RMS); unweighted	72	76	–	dB
α19	carrier and harmonic suppression at the output with and without modulation (for 19 kHz including notch)	pilot signal f_i = 19 kHz	–	81	–	dB
		no modulation	–	98	–	dB
α38	carrier and harmonic suppression at the output with and without modulation	subcarrier; f_i = 38 kHz	–	83	–	dB
		no modulation	–	91	–	dB
α57	carrier and harmonic suppression at the output with and without modulation	subcarrier; f_i = 57 kHz	–	83	–	dB
		no modulation	–	96	–	dB
α76	carrier and harmonic suppression at the output with and without modulation	subcarrier; f_i = 76 kHz	–	84	–	dB
		no modulation	–	94	–	dB
$IM_{\alpha 10}$	intermodulation	f_{mod} = 10 kHz; f_{spur} = 1 kHz; note 1	77	–	–	dB
$IM_{\alpha 3}$	intermodulation	f_{mod} = 13 kHz; f_{spur} = 1 kHz; note 1	76	–	–	dB
α57(VF)	traffic radio suppression	f_i = 57 kHz; note 2	–	110	–	dB
α67	subsidiary communication authority (SCA)	f_i = 67 kHz; note 3	–	110	–	dB
α114	adjacent channel interference	f_i = 114 kHz; note 4	–	110	–	dB
α190	adjacent channel interference	f_i = 190 kHz; note 4	–	110	–	dB
$V_{pilot(rms)}$	pilot threshold voltage at pin 42	stereo ON	–	35.6	–	mV
		stereo OFF	–	35.5	–	mV
HYS	hysteresis level of pilot voltage		–	0	–	dB
f_i	input frequency range MPX	–3 dB; ADC via bitstream test output	0	–	55	kHz
α_{cs}	FM stereo channel separation	f_i = 1 kHz	40	45	–	dB
		f_i = 10 kHz	25	30	–	dB
f_{resFM}	audio frequency response FM	at –3 dB via DSP at DAC output	16	–	–	kHz
$\lvert\Delta G_v\rvert$	channel unbalance left/right TAPE, AUX, FM and AM		–	–	0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{cs}	channel separation TAPE and AUX	f_i = 1 kHz	40	45	–	dB
		f_i = 10 kHz	25	30	–	dB
		f_i = 1 kHz, software compensated	–	50	–	dB
f_{res}	frequency response TAPE and AUX	at –3 dB	18	–	–	kHz
α_{ct}	crosstalk between inputs	f_i = 1 kHz	65	–	–	dB
		f_i = 15 kHz	50	–	–	dB
PSRR	power supply ripple rejection for MPX and RDS ADCs	output via I^2S-bus; ADC input shorted; f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); $C_{VrefMPX}$ = 22 µF; $C_{VrefRDS}$ = 22 µF; C_{VDACPM} = 10 µF	35	45	–	dB
	power supply ripple rejection for ADC level	output via DAC; ADC input shorted; f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); $C_{VrefRDS}$ = 22 µF	29	39	–	dB
Analog AC inputs: RDS						
$V_{i(rms)}$	input voltage level (RMS value)	THD < 1%	1.1	–	–	V
R_i	input resistance RDS ADC		48	60	72	kΩ
α_{pilot}	pilot attenuation RDS		50	–	–	dB
α	nearby selectivity RDS	neighbouring channel at 200 kHz distance	61	–	–	dB
α_{mux}	multiplex attenuation RDS	mono	70	–	–	dB
		stereo	40	–	–	dB
Δf_{osc}	allowable frequency deviation 57 kHz RDS	maximum crystal deviation of 100 ppm	–	–	6	Hz
Analog outputs: $V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V; T_{amb} = 25 °C						
PSRR	power supply ripple rejection DACs	input via I^2S-bus; f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); C_{Vref} = 22 µF	35	42	–	dB
$\Delta V_{o(DAC)}$	maximum deviation in output level (plus or minus) of the 4 DAC current outputs	with respect to the average of the 4 outputs; tolerance R_o < 0.1%; full-scale output	–	–	0.38	dB
α_{ct}	crosstalk between all outputs in the audio band	two outputs digital silence other two maximum volume; f_{audio} = 10 kHz	–	–	–60	dB
G_O	DC open loop gain of operational amplifiers		–	85	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_o	AC output impedance of operational amplifiers	$R_L > 5$ kΩ; note 5	–	1.5	–	Ω
f_{ug}	unity gain frequency operational amplifiers	open loop	–	4.5	–	MHz
$I_{o(sc)}$	short-circuit current output	output short-circuited to ground	–	10	25	mA
RES	DAC resolution		–	18	–	bits
(THD + N)/S	DAC total harmonic distortion plus noise-to-signal ratio of DAC and operational amplifiers	f_i = 1 kHz; V_o = 2.8 V (p-p) (full-scale)	–	–70	–60	dB
		f_i = 1 kHz; at –60 dB; A-weighted	–	–38	–28	dBA
DR	dynamic range	$V_{ref(o)}$ = 4.46 V (p-p); f_i = 1 kHz; at –60 dB; A-weighted	92	102	–	dBA
DS	digital silence	$V_{ref(o)}$ = 4.46 V (p-p); f_i = 20 Hz to 17 kHz; A-weighted	–	–110	–100	dBA
	digital silence noise level at output	RMS value; B = 20 kHz, A-weighted	–	5	15	μV
IM	intermodulation distortion/comparator	f_i = 60 Hz and 7 kHz; ratio 4 : 1	–	–70	–55	dB
$f_{s(max)}$	maximum sample frequency	f_{xtal} = 36.9 MHz	48	–	–	kHz
B	bandwidth of DAC	$f_s = f_s$ – 3 dB	–	$\frac{1}{2}f_s$	–	kHz
C_L	allowed load capacitance on DAC voltage outputs		–	–	2.5	nF
R_L	allowed load resistor on DAC voltage outputs		2	–	–	kΩ
Crystal oscillator at: V_{DDX} = 5 V; T_{amb} = 25 °C						
f_{xtal}	crystal frequency		–	36.860	–	MHz
α_f	spurious frequency attenuation		20	–	–	dB
I_{64}	output current pin 64		–	–	1	mA
G_m	transconductance	at start-up	4	8	–	mS
V_{xtal}	voltage across crystal		–	500	–	mV
C_L	load capacitance	note 6	–	10	–	pF
R_{xtal}	allowed resistance loss of crystal	C_p = 5 pF; C_{x1} = 10 pF; C_{x2} = 10 pF	–	20	100	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing at: V_{DDD} = V_{DDA} = V_{DDA1} = V_{DDX} = 5 V; T_{amb} = 25 °C						
f_{xtal}	crystal frequency		–	36.860	–	MHz
$\delta f_{xtal}/f_{xtal}$	frequency adjustment tolerance		–30	–	+30	ppm
$\delta f_{xtal}/\Delta T$	drift over temperature range		–30	–	+30	ppm
$f_{i(max)}$	maximum input frequency of I^2C-bus clock		100	–	–	kHz
I^2S-bus inputs and outputs (see Fig.18)						
t_r	rise time	V_{DDD} = 4.75 V; T_{amb} = 85 °C	–	–	4.75 + 0.28C_L	ns
		V_{DDD} = 5.5 V; T_{amb} = –40 °C	1.302 + 0.101C_L	–	–	ns
t_f	fall time	V_{DDD} = 4.75 V; T_{amb} = 85 °C	–	–	6.44 + 0.36C_L	ns
		V_{DDD} = 5.5 V; T_{amb} = –40 °C	0.971 + 0.115C_L	–	–	ns
t_{HC}	clock output HIGH time		112	–	–	ns
t_{LC}	clock output LOW time		112	–	–	ns
t_{dWS}	Word Select delay time		0	–	–	ns
t_h	data hold time		0	–	–	ns
t_s	data set-up time		25	–	–	ns
t_d	data delay time		0	–	5	ns
t_a	data out access time		–	–	5 + 0.5C_L	ns
RDS; (see Figs.14 and 15**)**						
f_{clk}	nominal clock frequency	RDS-clock	–	1187.5	–	Hz
t_s	clock set-up time		100	–	–	µs
T_{cy}	periodic time		–	842	–	µs
t_{HC}	clock HIGH time		220	–	640	µs
t_{LC}	clock LOW time		220	–	640	µs
t_h	data hold time		100	–	–	µs
t_w	wait time		1	–	–	µs
t_{pb}	periodic time		2	–	–	µs
t_{HC}	clock HIGH time		1	–	–	µs
t_{LC}	clock LOW time		1	–	–	µs
Other						
f_{EXCLK}	input frequency on pin 40		–	–	22	MHz

Notes to the AC characteristics

1. Intermodulation suppression (BFC: Beat Frequency Components).
   a) $\alpha 2 = V_{o(signal)}$ (at 1 kHz)/$V_{o(spurious)}$ (at 1 kHz); $f_s = (2 \times 10\ kHz) - 19\ kHz$.
   b) $\alpha 3 = V_{o(signal)}$ (at 1 kHz)/$V_{o(spurious)}$ (at 1 kHz); $f_s = (3 \times 13\ kHz) - 38\ kHz$.
   c) Measured with 91% mono signal; f_{mod} = 10 or 13 kHz; 9% pilot signal.
2. Traffic radio (VF) suppression.
   a) $\alpha 57(VF) = V_{o(signal)}$ (at 1 kHz)/$V_{o(spurious)}$ (at 1 kHz $\pm$23 Hz).
   b) Measured with 91% stereo signal; f_{mod} = 1 kHz; 9% pilot signal.
   c) 5% traffic subcarrier (f = 57 kHz; f_{mod} = 23 Hz AM, m = 0.6).
3. SCA (Subsidiary Communication Authorization).
   a) $\alpha 67 = V_{o(signal)}$ (at 1 kHz)/$V_{o(spurious)}$ (at 9 kHz); $f_s = (2 \times 38\ kHz) - 67\ kHz$.
   b) Measured with 81% mono signal; f_{mod} = 1 kHz; 9% pilot signal.
   c) 10% SCA subcarrier (f_s = 67 kHz, unmodulated).
4. ACI (Adjacent Channel Interference).
   a) $\alpha 114 = V_{o(signal)}$ (at 1 kHz)/$V_{o(spurious)}$ (at 4 kHz); $f_s = 110\ kHz - (3 \times 38\ kHz)$.
   b) $\alpha 190 = V_{o(signal)}$ (at 1 kHz)/$V_{o(spurious)}$ (at 4 kHz); $f_s = 186\ kHz - (5 \times 38\ kHz)$.
   c) Measured with 90% mono signal; f_{mod} = 1 kHz; 9% pilot signal; 1% spurious signal (f_s = 110 kHz or 186 kHz, unmodulated).
5. R_L is the AC impedance of the external circuitry at 1 kHz connected to the audio outputs in the application. There is also no DC current flowing through R_L.
6. The load capacitance is the sum of the series connection of C $\times$ 1 and C $\times$ 2 (see Fig.11) and the parasitic parallel capacitor of the crystal C_p.

15 I²C-BUS CONTROL AND COMMANDS

15.1 Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to V_{DDD} via a pull-up resistor when connected to the output stages of a microcontroller. Data transfer can only be initiated when the bus is not busy.

15.2 Bit transfer

One data bit is transferred during each clock pulse.
The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.
The maximum clock frequency is 100 kHz (see Fig.16).

15.3 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Fig.17).

15.4 Data transfer

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’.

The device that controls the message is the ‘master’ and the devices that are controlled by the master are the ‘slaves’ (see Fig.18).

15.5 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge-related clock pulse.
A slave receiver that is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Set-up and hold times must be taken into account. A master receiver must signal an end-of-data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH, to enable the master to generate a STOP condition (see Fig.19).

15.6 I²C-bus format

15.6.1 ADDRESSING

Before any data is transmitted on the I²C-bus, the device that should respond is addressed first. The addressing is always done with the first byte transmitted after the START procedure.

15.6.2 SLAVE ADDRESS (A0 PIN)

The CDSP acts as a slave receiver or slave transmitter. Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bi-directional line. The CDSP slave address is shown in Table 6.

Table 6 Slave address

MSB							**LSB**
0	0	1	1	1	0	A0	R/$\overline{W}$

The sub-address bit A0 corresponds to the hardware address pin A0, which allows the device to have 1 of 2 different addresses. The A0 input is also used in test mode as a serial input of the test control block.

15.6.3 CDSP WRITE CYCLES

The I²C-bus configuration for a WRITE cycle is illustrated in Fig.22. The WRITE cycle is used to write in the IAC register, the input selector control register and to initialize or update coefficient values in XRAM or YRAM. The data is transferred from the I²C-bus register to the DSP register once every DSP cycle.

The I²C-bus interface circuitry in the SAA7707H requires that the LOW period of the SCL line following the acknowledge bit is at least $1/f_s$ (in seconds); where f_s is the audio sampling frequency (in Hertz). This requirement must be met for a single write operation and an auto-incremental operation, but only applies to the acknowledge bit following each DATA-L (see Figs 20 and 21).

The data length is 2 or 3 bytes, depending on the accessed memory. If the Y-memory is addressed the data length is 2 bytes, If the X-memory is addressed the length is 3 bytes. The slave receiver detects the address and adjusts the byte length accordingly.

15.6.4 CDSP READ CYCLES

The I²C-bus configuration for a READ cycle is illustrated in Fig.23. The READ cycle is used to read data values from XRAM or YRAM. The data is transferred from the DSP register to the I²C-bus register at execution of the MPI instruction in the DSP program. Therefore, an MPI instruction should be added at least once every DSP cycle.

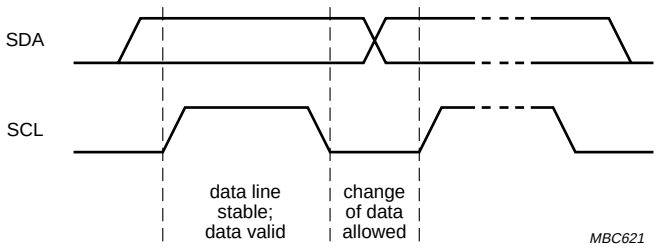


Fig.16 Bit transfer on the I²C-bus.

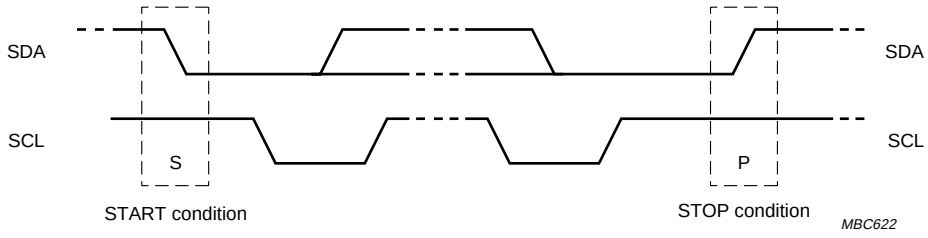


Fig.17 START and STOP conditions.

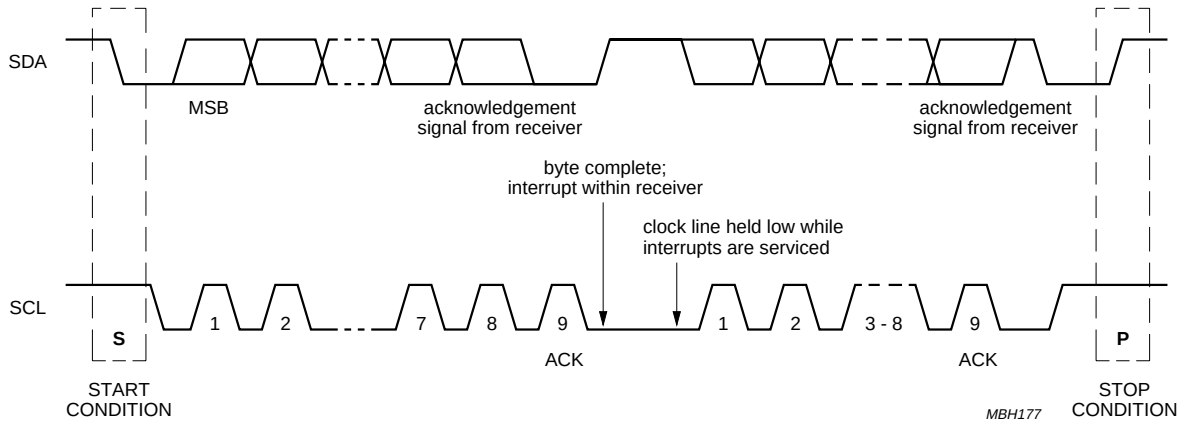


Fig.18 Data transfer on the I²C-bus.

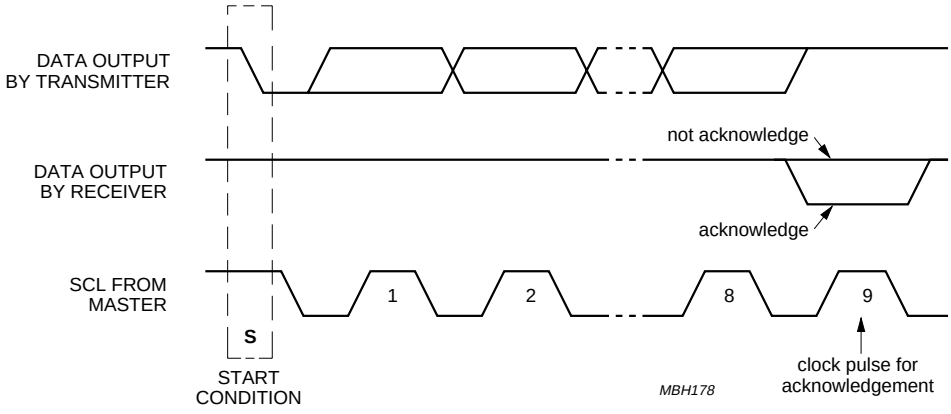


Fig.19 Acknowledge on the I²C-bus.

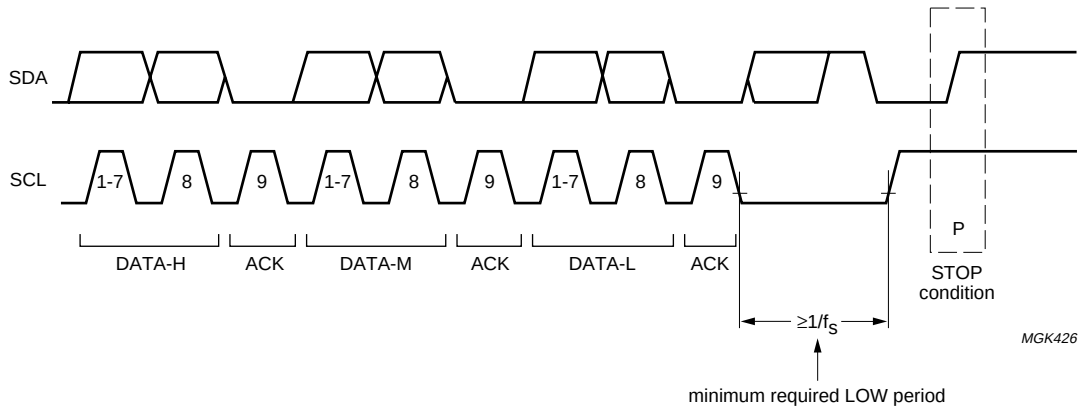


Fig.20 Minimum required SCL LOW period; single write.

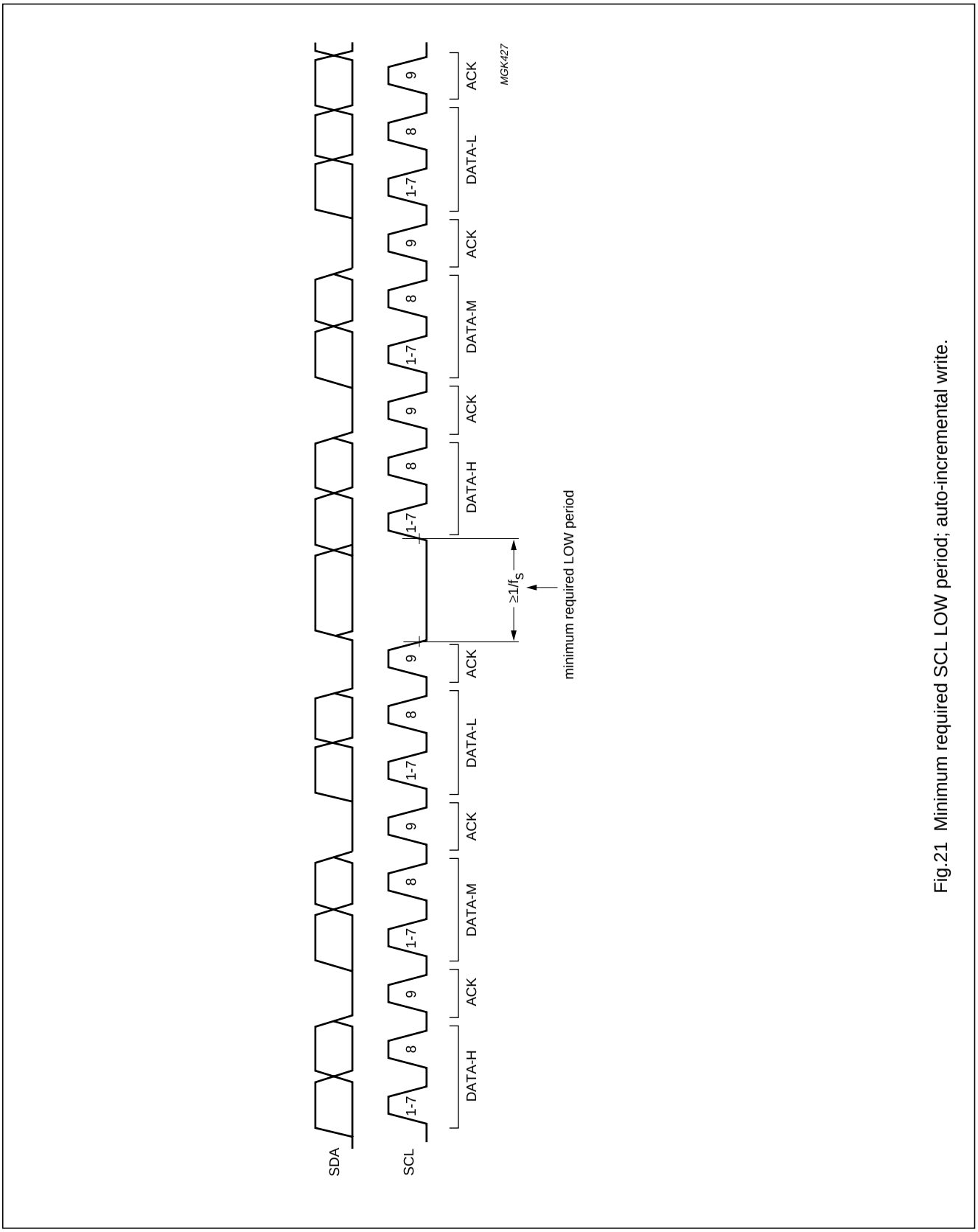


Fig.21 Minimum required SCL LOW period; auto-incremental write.

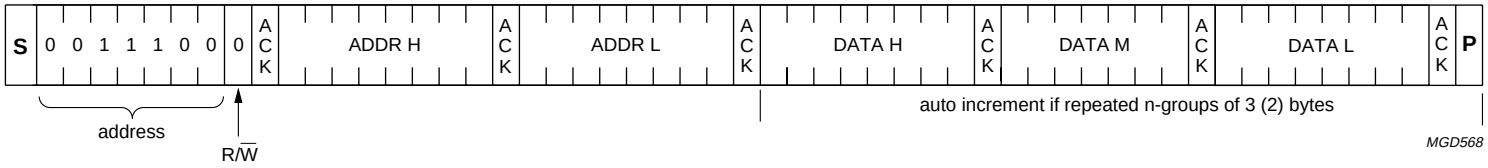


Fig.22 Master transmitter writes to CDSP registers.

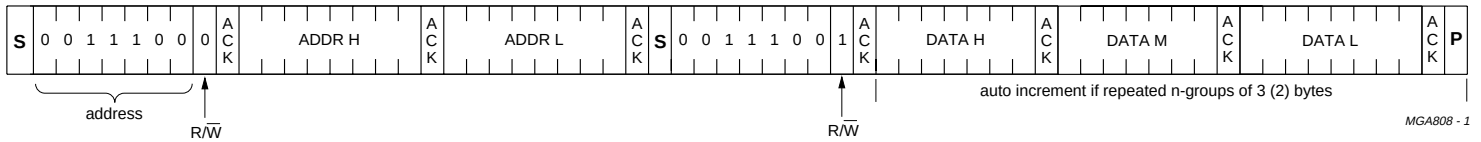


Fig.23 Master transmitter reads from CDSP registers.

16 SOFTWARE DESCRIPTION

A detailed description of the software feature, complete with operating instructions, is provided in the application manual.

17 APPLICATION INFORMATION

The application diagram illustrated in Figs. 24 and 25 must be considered as one of the examples of a (limited) application of the SAA7707H. For example, in the application shown, the I^2S-bus inputs of the DCC and CD are not used.

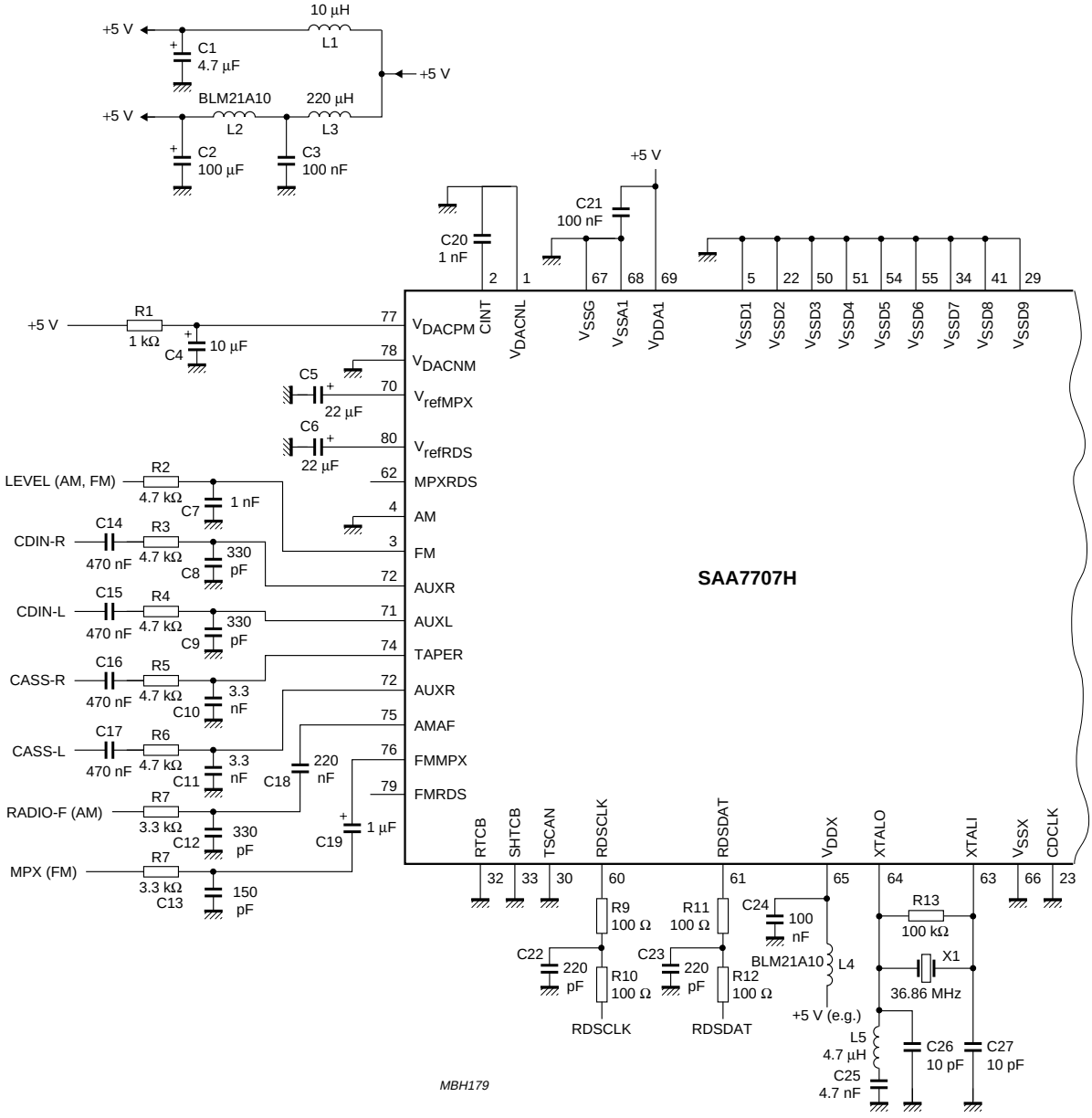


Fig.24 Application diagram (continued in Fig.25).

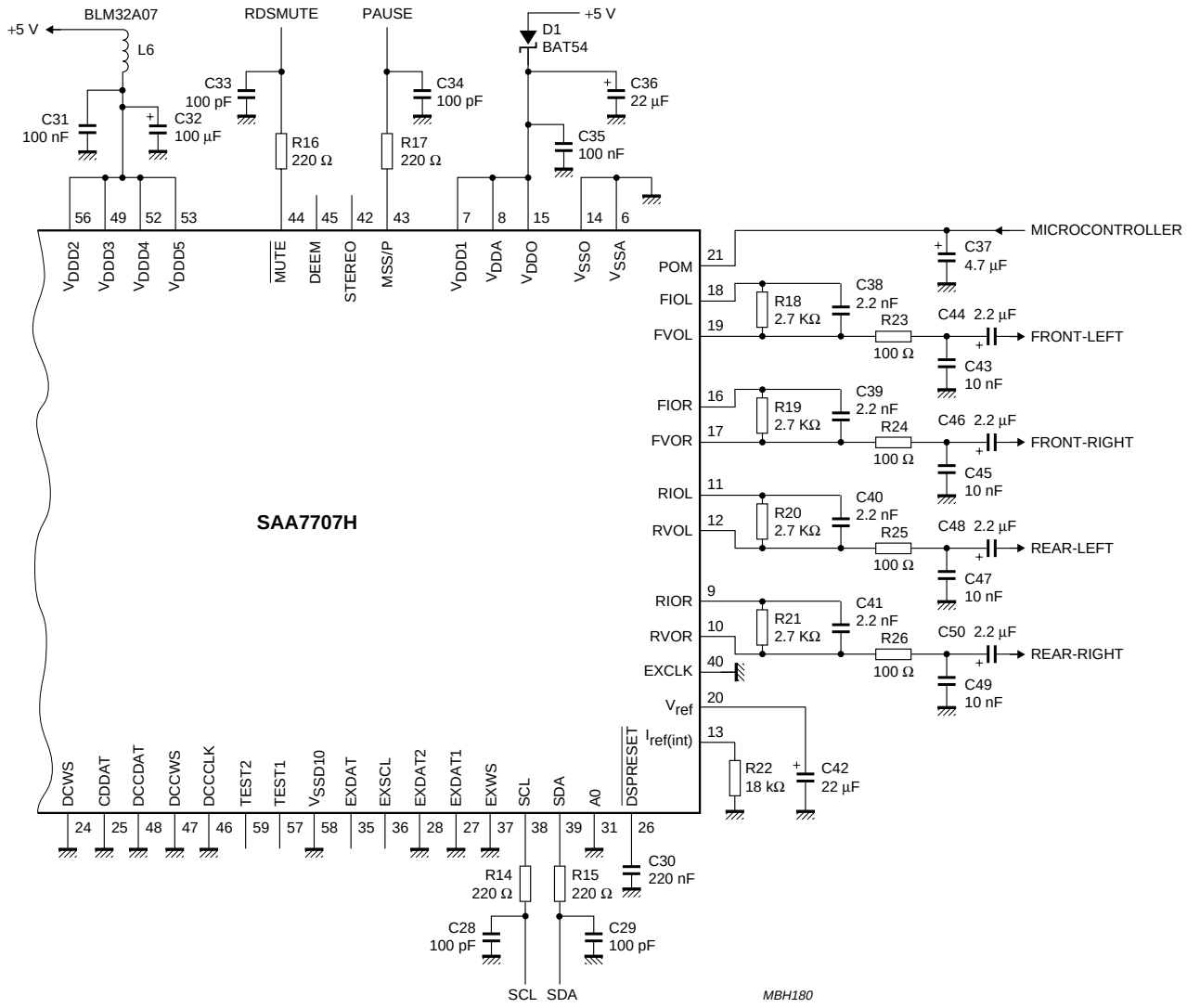
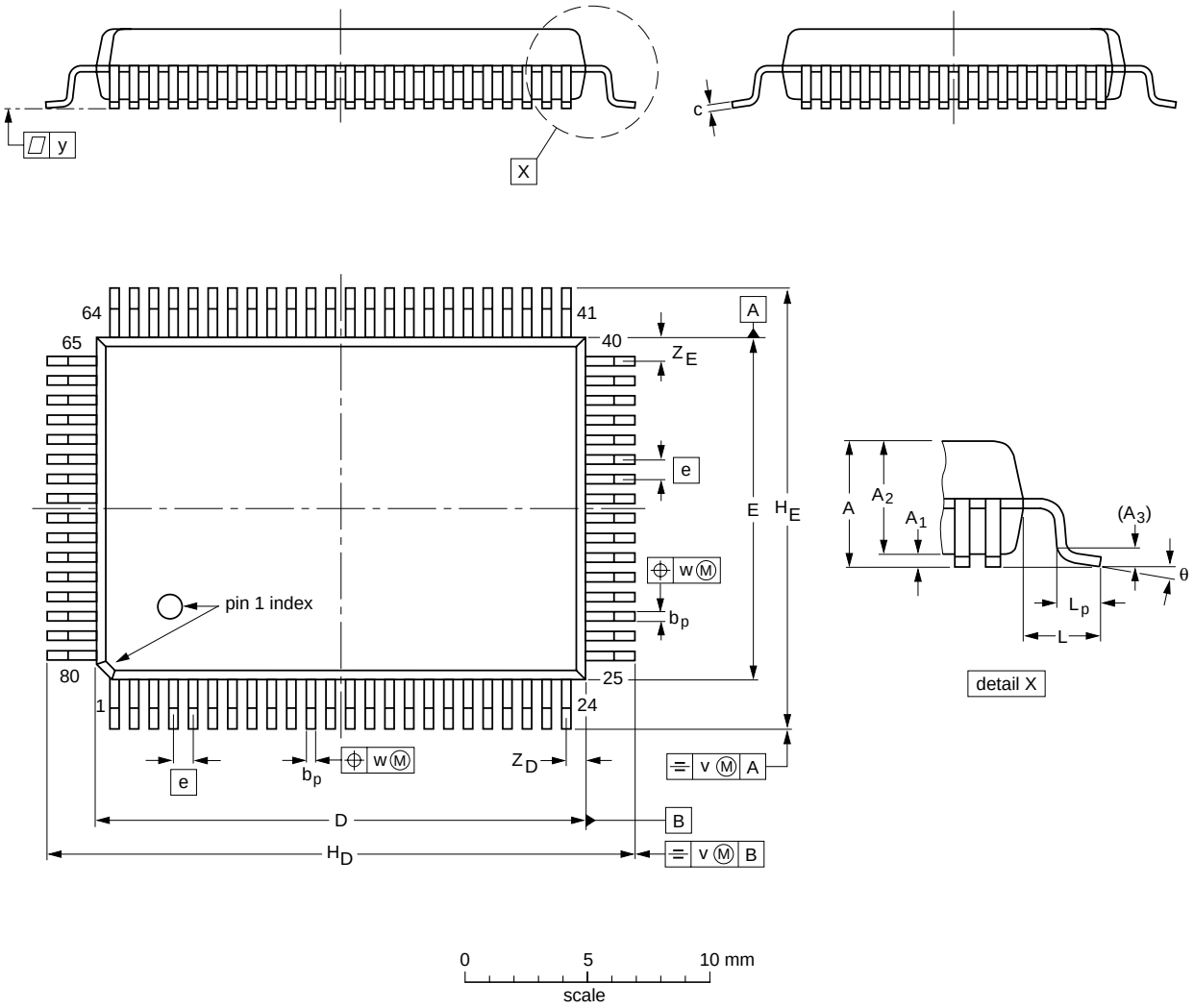


Fig.25 Application diagram (continued from Fig.24).

18 PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2						~~95-02-04~~ 97-08-01

19 SOLDERING

19.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

19.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

19.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

20 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

21 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

22 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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