PRELIMINARY

MOSTEK

3870 MICROCOMPUTER COMPONENTS

Serial Control Unit SCU20

FEATURES

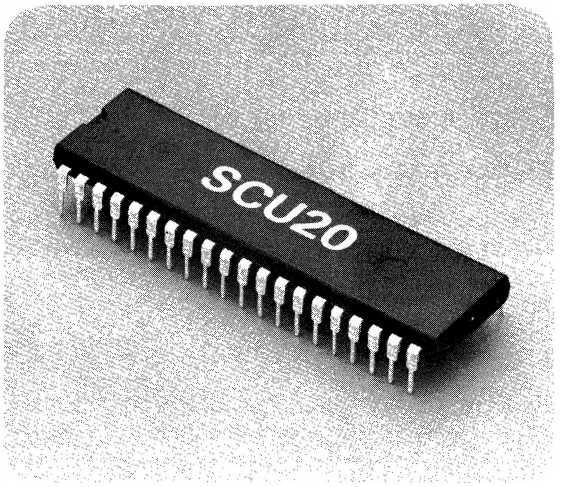
- Provides programmable remote I/O functions, real time operational capabilities, and standardized network communications on a 40 pin chip.
- Performs preprogrammed functions on command, including:
  - Byte input and output
  - Bit input and output
  - Set, clear, and toggle selected pins
  - Data access from real time functions
- Performs real time preprogrammed functions, including:
  - Data log on external interrupt, timer, or host control, up to 63 bytes of data
  - Five Event Counters driven from external interrupt, timer or host control
- Up to 24 programmable I/O pins
- Allows user to network up to 255 SCUs on a single communications channel
- Asynchronous serial data transmission
- Selectable Baud rate (300, 1200, 2400, or 9600 Baud)
- Secure, Error resistant data link protocol
- Requires single +5 volt supply
- Low power (275mW typ)

INTRODUCTION

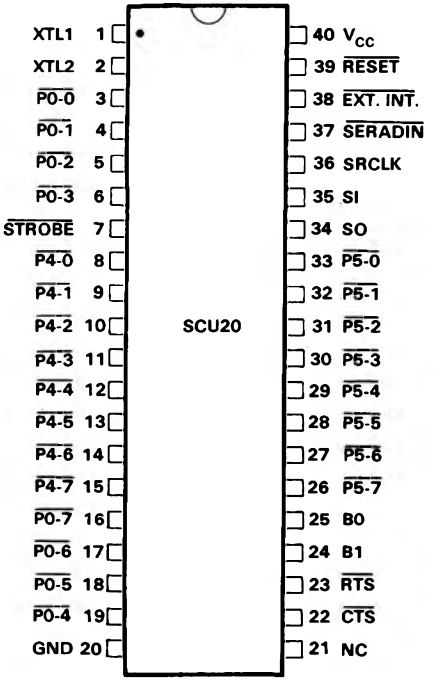
The SCU20 serial control unit is a preprogrammed MK3873 single chip microcomputer. It is a general purpose remote control/data acquisition unit, with 38 preprogrammed functions available to the user.

Communications with the SCU20 take place over an asynchronous half duplex communications channel at 300, 1200, 2400, or 9600 Baud. The communications protocol is efficient and error resistant, and yet easy to implement on the host system.

SCU20
Figure 1



SCU20 PINOUT
Figure 2



The SCU20 can be used for both monitoring and control systems where remote intelligence is required. It can be configured to provide many different input/output and data acquisition functions through its 24 I/O pins. Such intelligent functions as Data Log and Event Counters allow many different applications that will not burden the host system with constant update requirements.

FUNCTIONAL PIN DESCRIPTION

The SCU20 is housed in a plastic 40 pin dual in-line package.

Figure 2 shows the location of each pin on the SCU20. The following describes the function of each pin.

SCU20 PINOUT DEFINITION

XTL1, XTL2 - Time base inputs for 3.6864 MHz crystal.

$\overline{P0\text{-}0}$ - $\overline{P0\text{-}7}$ - SCU20 port 0 (Bidirectional, active low). SCU20 address input or general purpose data port (see SCU20 Address section).

$\overline{STROBE}$ - Data available strobe for port 4 (output active low).

$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ - SCU20 port 4 (Bidirectional, active low). General purpose data port.

$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ - SCU20 port 5 (Bidirectional, active low). General purpose data port.

SRCLK - Clock signal generated by internal Baud rate generator.

SI - Serial input. Receives serial asynchronous data from the host.

SO - Serial output. Transmits serial asynchronous data to the host.

$\overline{RTS}$ - Request to send (output, active low).

$\overline{CTS}$ - Clear to send (input, active low).

$\overline{RESET}$ - External reset (input, active low).

$\overline{EXT.\ INT.}$ - External interrupt (input, active low).

$\overline{SERADIN}$ - Serial address input/address mode (input, active low. See SCU20 Address section).

B0, B1 - Baud rate select.

V_{CC} - Power supply, 5 volts.

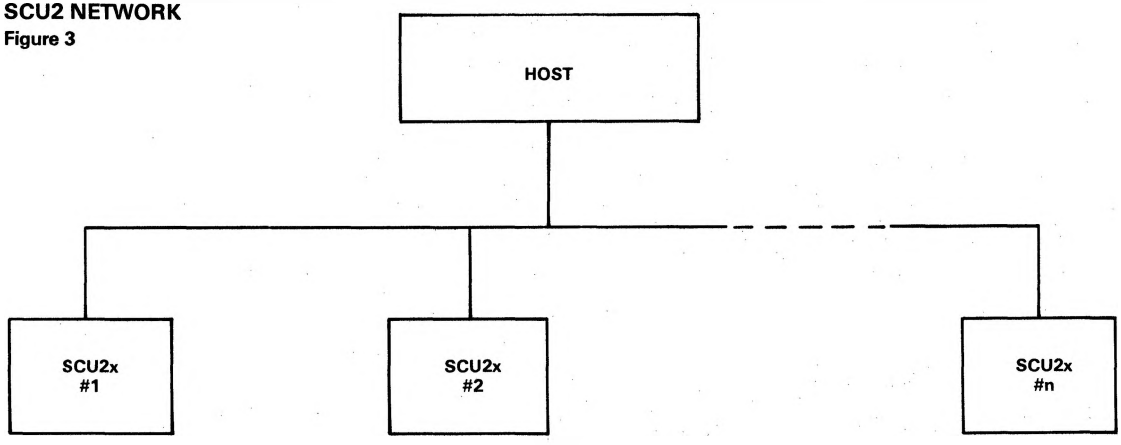
GND - Power supply ground.

SCU2 NETWORK

The SCU2 Network is a serial linked network of devices in the SCU2 family. All communications are via a common serial link using the SCU2 family communications protocol. In this way, a distributed control facility may be easily implemented from standard parts, and controlled by the host computer via the serial link.

Figure 3 illustrates the SCU2 Network.

SCU2 NETWORK
Figure 3



Each SCU2x in the network has an individual address to which it will respond. All SCU2x devices in the network are slave processors to the host, and are unable to initiate communications except in response to the host.

When the system is initialized, all SCU2x devices are in the listen mode, and are performing no functions. The host will issue an inquiry command to each device. Once all devices have been queried, the host will issue commands to each device to set up the particular operational parameters required of it. When this has been done, the host may then use the devices to control equipment, measure values, etc., by issuing commands and receiving responses.

Unless issuing a response, the SCU2x is always in the listen mode. If a command has been sent to an SCU2x, a response is expected within a specific time period. If none is forthcoming, it means that the command transmitted was not successfully received by the device. In this case, the host must take steps either to notify the operator or to retransmit the command.

If a system error occurs in the host, it may suspend operation of the entire network by transmitting the network reset command which causes all devices to be reset. This is the only command that does not require a specific SCU2x address as part of the command. It uses the system reset address which is recognized by each device.

SCU20 ADDRESS

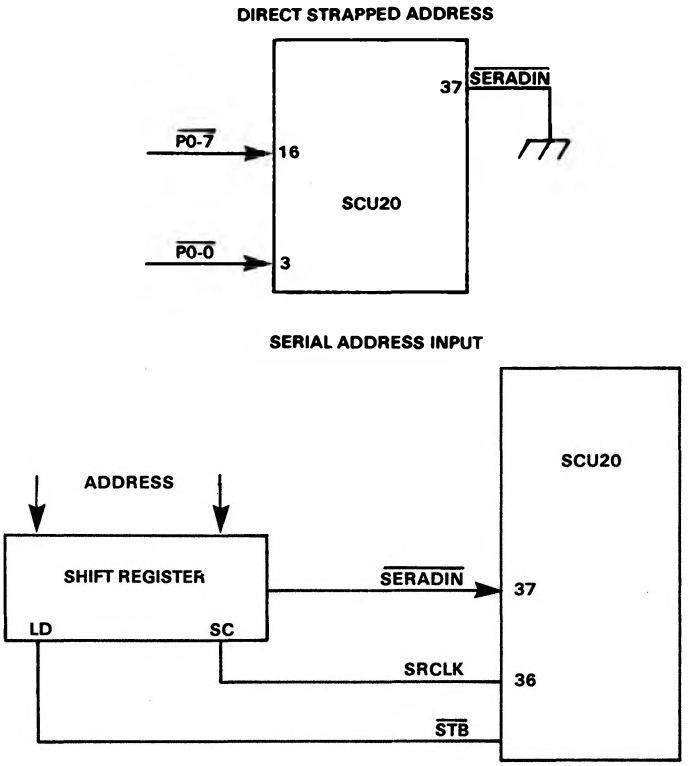
The address to which the SCU20 responds may be established in one of two ways.

The first mode is the Direct Strapped Address mode, and is enabled by tying the $\overline{\text{SERADIN}}$ pin directly to ground. In this mode, the SCU20 address is strapped at port 0. Because of this, port 0 is not available as a general purpose I/O port.

The second mode is the Serial Address Input mode. The $\overline{\text{SERADIN}}$ pin is used to input the address as a serial 8-bit stream from a shift register. SRCLK is used as a shift clock for this operation. The $\overline{\text{STROBE}}$ signal is used at initialization time to cause the address to be loaded into the shift register before shifting begins. In the Serial Address mode, port 0 becomes available for use as a general purpose data I/O port.

Figure 4 illustrates both methods of establishing the SCU20 address.

SCU20 ADDRESS ESTABLISHMENT
Figure 4



SCU20 COMMUNICATIONS

The SCU20 communicates with the host computer over a half duplex asynchronous serial link. The communications protocol is simple, yet error resistant.

The general form of the communication message is as follows:

HDR	ADDR	CMD	DATA	DATA	• • • •	LRC

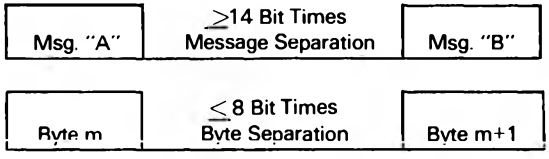
HDR - Message header. Hex '01' indicates a command message from the host; Hex '02' indicates a response from the SCU20.

ADDR - SCU20 Address. Indicates which SCU20 the message is for, or originates from.

CMD - Command. Indicates the function to be performed.

DATA - Any data that may be required by the particular command.

LRC - Linear Redundancy Check.



Messages are to be transmitted in block mode, with a message separation of at least 14 bit times. Interbyte separations should be no more than 8 bit times within a message.

A message from the host to the SCU20 will generate a response if there is no transmission error. If any transmission error is detected, no response will be made.

Possible transmission errors are LRC errors, parity errors, interbyte separation errors, or intermessage separation errors.

BAUD RATE SELECTION

The serial Baud rate is selected by a strapped option on the SCU20. Those options are listed below:

BAUD RATE	B0 (Pin 25)	B1 (Pin 24)
300	Low	Low
1200	Low	High
2400	High	Low
9600	High	High

MODEM SIGNALS

$\overline{RTS}$ and $\overline{CTS}$ are provided to facilitate handshaking with modems. Just prior to responding to a valid command, $\overline{RTS}$ will go to logic 1, indicating that the SCU20 is ready to send data back to the host. $\overline{CTS}$ is an input to the SCU20 that is tested after $\overline{RTS}$ goes active to determine if the SCU20 may begin transmitting data.

PARALLEL I/O PORTS

The SCU20 has a minimum of 2 parallel I/O ports and a maximum of 3 available for general use, depending on the address selection mode chosen. For each of these ports, there exist 2 registers that control and modify the I/O to and from the ports. These are the Data Direction Register (DDR) and the Mask Register(MR).

The Data Direction Register defines the usage of each pin in the port. If a bit is set to 0, then the corresponding pin is used as input. If a bit is set to 1, then the corresponding pin is used as an output. When a port is read, all bits are sampled for input whether or not they are marked for input. When a port is written to, however, only those pins declared as output will be modified.

The Mask Register provides a data mask that may be applied to the input data before transmission to the master. The mask is established once and may be used repeatedly before being changed by establishing a new mask value. If a pin is to be available upon read, the corresponding bit in the mask register is set to 1, while a pin that is to be masked out will have its mask bit set to 0.

SCU20 PREPROGRAMMED FUNCTIONS

The SCU20 has a variety of preprogrammed functions available to the user. Each of these functions addresses a different general area of application such that the SCU20 is truly a general purpose device.

PORT COMMANDS

There are several commands which allow the host to manipulate the 8-bit general purpose I/O ports. The host may load data into any one or all of the ports, may read any or all of the ports with or without a mask, may read with a new mask, or may read using the last defined mask. When data is loaded, the resulting port state is returned in the response message.

LOGIC COMMANDS

In addition to performing data I/O with the ports, the host may perform logical operations with the ports and data from the host. These commands allow the host to AND, OR, or Exclusive OR (XOR) data with any or all of the ports, and output the result to the ports. The resultant output is returned in the command response message.

BIT COMMANDS

These commands allow the host to SET, CLEAR, TEST, or TOGGLE bits in the ports by specifying bit number (0 - 24). Any pin that is declared as an input will not be changed.

EVENT COUNTERS

There are 5 Event Counters defined in SCU20. They are 16 bit up counters, and are driven by the timer, the external interrupt, or by host command. They may be used as simple event counters, or may be used in conjunction with the Data Log, and Pulse functions.

DATA LOG

The Data Log function allows the user to command the SCU20 to log data from the ports specified in the command, and store the data in the on-board RAM. Up to 63 bytes of data may be accumulated in the log, and may be captured on external interrupt, timer, or host command through use of an Event Counter.

Data from the Log is transmitted back to the host in a single read command burst.

CONTROL COMMANDS

There are several commands to control the SCU20 as well as the entire SCU2 network. These commands provide the host with the ability to query each individual SCU2x on the network for its type, the last message it sent, and for detailed error codes. In addition, there are commands that allow the host to reset an individual device, or to cause the entire SCU2 network to reset with a single command.

ERROR PROCESSING

The SCU20 does not provide a "negative acknowledge" response to command stream errors. Those errors are parity errors, LRC errors, unidentifiable commands, overrun, or violation of the separation specifications as described earlier.

In some cases, the SCU20 will provide error response to functional errors in commands that have been recognized. This response will be either a "NAK0" or a "NAK3" as specified for the command. "NAK0" is the hex value H'FB', and "NAK3" is the hex value H'FE'.

H'2'	ADDR	H'FB' or H'FE'	LRC

SCU20 COMMANDS

Figure 5 gives a complete list of the commands and functions available to the SCU20. For a full description of these commands and their use, refer to the SCU20 Operations Manual.

SCU20 COMMANDS
Figure 5

FUNCTION	COMMAND CODES	# DATA BYTES (CMD)	# DATA BYTES (RESP)	ERR COD RET
** PORT COMMANDS **				
Load Data Direction Registers	1E	3	0	-
Load Port (0, 4, 5)	00,01,02	1	1	-
Load All Ports	03	3	3	-
Read Port (0, 4, 5)	04,05,06	0	1	-
Read All Ports	07	0	3	-
Read Port Masked, Mask Provided	08,09,0A	1	1	-
Read All Ports, Masks Provided	0B	3	3	-
Read Port using Previous Mask	0C,0D,0E	0	1	-
Read All Ports using Previous Masks	0F	0	3	-

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -20°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin With Respect to Ground
(Except open drain pins and TEST) ..... -1.0 V to +7 V
Voltage on TEST with Respect to Ground ..... -1.0 V to + 9 V
Voltage on Open Drain Pins With Respect to Ground ..... -1.0 V to +13.5 V
Power Dissipation ..... 1.5 W
Power Dissipation by any one I/O pin[2] ..... 60 mW
Power Dissipation by all I/O pins[2] ..... 600 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING VOLTAGES AND TEMPERATURES

Operating Voltage V_{CC} ..... +5 V ± 10%
Operating Temperature T_A ..... 0° - 70°C

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	NOTES
XTL1 XTL2	t_o	Time Base Period, all clock modes	250	500	ns	4 MHz - 2 MHz 3.6864 required for
	$t_{ex(H)}$	External clock pulse width high	90	400	ns	standard baud
	$t_{ex(L)}$	External clock pulse width low	100	400	ns	frequencies
Φ	t_Φ	Internal Φ clock	$2t_O$			
$\overline{\text{STROBE}}$	$t_{I/O-s}$	output valid to $\overline{\text{STROBE}}$ delay	3tΦ -1000	3tΦ +250	ns	I/O load = 50 pF + 1 TTL load
	t_{sL}	$\overline{\text{STROBE}}$ low time	8tΦ -250	12tΦ +250	ns	$\overline{\text{STROBE}}$ load = 50 pF + 3TTL loads
$\overline{\text{RESET}}$	t_{RH}	$\overline{\text{RESET}}$ hold time, low	6tΦ +750		ns	
	t_{RPOC}	$\overline{\text{RESET}}$ hold time, low for power clear	power supply rise time +0.1		ms	
$\overline{\text{EXT INT}}$	t_{EH}	$\overline{\text{EXT INT}}$ hold time in active and inactive state	6tΦ +750		ns	To trigger interrupt

CAPACITANCE
T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O, $\overline{\text{RESET}}$, $\overline{\text{EXT INT}}$		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

AC CHARACTERISTICS FOR SERIAL I/O PINS
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	CONDITIONS
SRCLK	$t_{r(SRCLK)}$	Serial Clock Rise Time	60		ns	0.8 V - 2.0 V C_L = 100 pf
	$t_{f(SRCLK)}$	Serial Clock Fall Time	30		ns	2.4 V - 0.4 V C_L = 100 pf

DC CHARACTERISTICS
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	MIN	MAX	UNIT	DEVICE
I_{CC}	Average Power Supply Current		103	mA	SCU20 Outputs Open
P_D	Power Dissipation		485	mW	SCU20 Outputs Open

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	MIN	MAX	UNIT	CONDITIONS
V_{IHEX}	External Clock input high level	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	V	
I_{IHEX}	External Clock input high current		100	μA	$V_{IHEX} = V_{CC}$
I_{ILEX}	External Clock input low current		-100	μA	$V_{ILEX} = V_{SS}$
$V_{IHI/O}$	I/O input high level	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	open drain (1)
V_{IHR}	Input high level, $\overline{\text{RESET}}$	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	No pull-up
V_{IHEI}	Input high level, $\overline{\text{EXT INT}}$	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	No pull-up
V_{IL}	I/O ports, $\overline{\text{RESET}}$[1], $\overline{\text{EXT INT}}$[1] input low level	-.3	.8	V	(1)
I_{IL}	Input low current, I/O ports and $\overline{\text{EXT IN}}$		-1.6	mA	$V_{IN} = 0.4$ V
I_L	Input leakage current, $\overline{\text{RESET}}$ input		+10 -5	μA μA	$V_{IN} = 13.2$ V $V_{IN} = 0.0$V
I_{OH}	Output high current, I/O ports	-100		μA	$V_{OH} = 2.4$ V
		-30		μA	$V_{OH} = 3.9$ V
I_{OL}	Output low current, I/O ports	1.8		mA	$V_{OL} = 0.4$ V
I_{OHS}	$\overline{\text{STROBE}}$ Output High current	-300		μA	$V_{OL} = 2.4$ V
I_{OLS}	$\overline{\text{STROBE}}$ output low current	5.0		mA	$V_{OL} = 0.4$ V

DC CHARACTERISTICS FOR SERIAL PORT I/O PINS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 2)

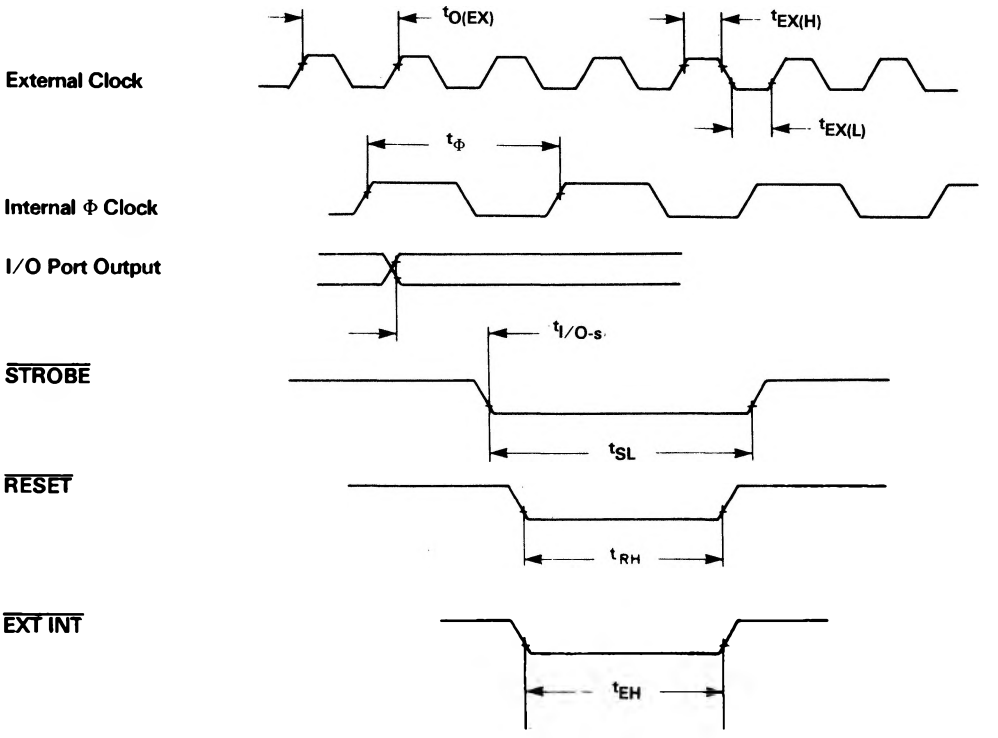
SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
V_{IHS}	Input High for SI	2.0	5.8	V	
V_{ILS}	Input Low level for SI	-.3	.8	V	
I_{ILS}	Input low current for SI		-1.6	mA	V_{IL} = 0.4 V
I_{OHSO}	Output High Current SO	-100 -30		μA μA	V_{OH} = 2.4 V V_{OL} = 3.9 V
I_{OLSO}	Output Low Current SO	1.8		mA	V_{OL} = 0.4 V
I_{OHSRC}	Output High Current, SRCLK	-300		μA	V_{OH} = 2.4 V
I_{OLSRC}	Output Low Current, SRCLK	5.0		mA	V_{OL} = 0.4 V

NOTES

1. RESET and EXT INT have internal Schmitt triggers giving minimum .2 V hysteresis.
2. Power dissipation for I/O pins is calculated by $\Sigma(V_{CC} - V_{IL})(\ I_{IL}\ ) + \Sigma(V_{CC} - V_{OH})(\ I_{OH}\ ) + \Sigma(V_{OL})(I_{OL})$

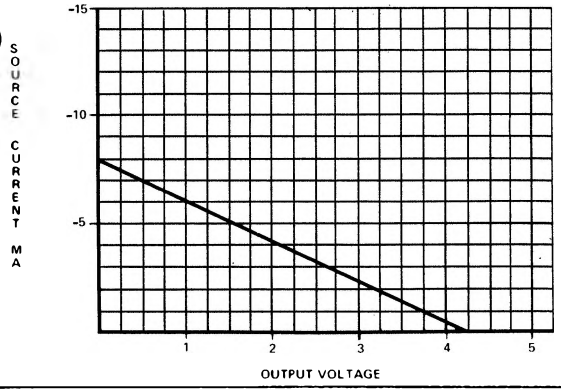
AC TIMING DIAGRAM

Figure 6

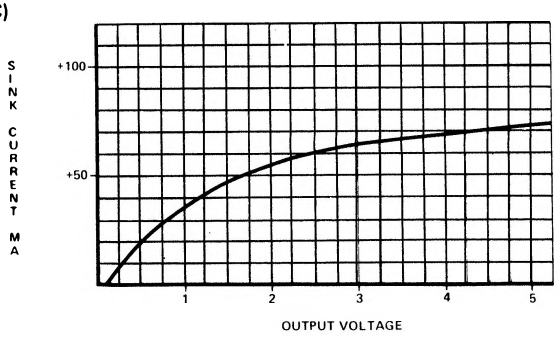


Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

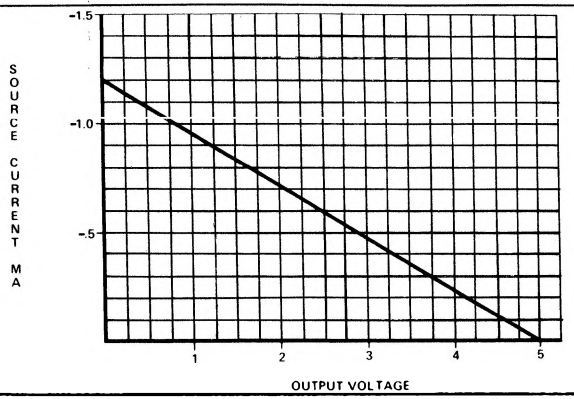
STROBE SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 7



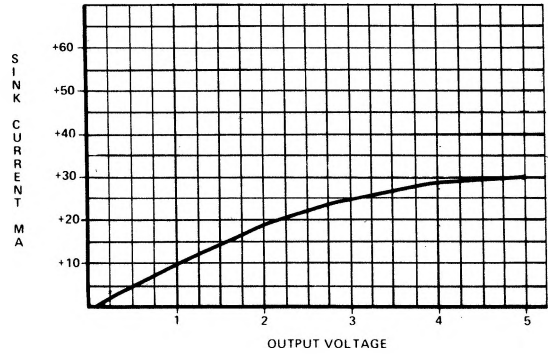
STROBE SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 8



STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 9

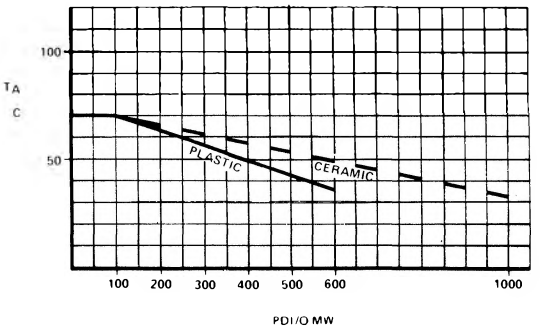


I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 10



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 11



ORDERING INFORMATION

An example of the device order number is shown below.

MK 95010 N - 1 0

Power Supply Tolerance	0 = 5 V ±10% 5 = 5 V ± 5%
Operating Temperature Range	0 = 0°C - +70°C 1 = -40°C - +85°C
Package Types	P = Ceramic N = Plastic
Customer/Code Specific Number	