Advanced Power MOSFET   SFP9630

FEATURES

■ Avalanche Rugged Technology
■ Rugged Gate Oxide Technology
■ Lower Input Capacitance
■ Improved Gate Charge
■ Extended Safe Operating Area
■ Lower Leakage Current : -10 μA (Max.) @ V_{DS} = -200V
■ Low $R_{DS(ON)}$: 0.581 Ω (Typ.)

BV_{DSS} = -200 V

$R_{DS(on)}$ = 0.8 Ω

I_D = -6.5 A

TO-220
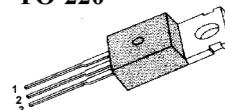
1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	-200	V
I_D	Continuous Drain Current (T_C=25°C)	-6.5	A
	Continuous Drain Current (T_C=100°C)	-4.0	
I_{DM}	Drain Current-Pulsed ①	-26	A
V_{GS}	Gate-to-Source Voltage	$\pm$30	V
E_{AS}	Single Pulsed Avalanche Energy ②	563	mJ
I_{AR}	Avalanche Current ①	-6.5	A
E_{AR}	Repetitive Avalanche Energy ①	7.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
P_D	Total Power Dissipation (T_C=25°C)	70	W
	Linear Derating Factor	0.56	W/^{o}C
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	^{o}C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8 " from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.79	^{o}C/W
$R_{\theta CS}$	Case-to-Sink	0.5	--	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

SAMSUNG
ELECTRONICS

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	-200	--	--	V	V_{GS}=0V,I_D=-250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	-0.17	--	V/^{o}C	I_D=-250μA *See Fig 7*
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	--	-4.0	V	V_{DS}=-5V,I_D=-250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	-100	nA	V_{GS}=-30V
	Gate-Source Leakage , Reverse	--	--	100		V_{GS}=30V
I_{DSS}	Drain-to-Source Leakage Current	--	--	-10	μA	V_{DS}=-200V
		--	--	-100		V_{DS}=-160V,T_C=125°C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.8	Ω	V_{GS}=-10V,I_D=-3.3A ④
g_{fs}	Forward Transconductance	--	4.2	--	$\mho$	V_{DS}=-40V,I_D=-3.3A ④
C_{iss}	Input Capacitance	--	740	965	pF	V_{GS}=0V,V_{DS}=-25V,f =1MHz *See Fig 5*
C_{oss}	Output Capacitance	--	125	185		
C_{rss}	Reverse Transfer Capacitance	--	49	75		
$t_{d(on)}$	Turn-On Delay Time	--	14	35	ns	V_{DD}=-100V,I_D=-6.5A, R_G=12Ω *See Fig 13* ④ ⑤
t_r	Rise Time	--	22	55		
$t_{d(off)}$	Turn-Off Delay Time	--	41	90		
t_f	Fall Time	--	17	45		
Q_g	Total Gate Charge	--	29	36	nC	V_{DS}=-160V,V_{GS}=-10V, I_D=-6.5A *See Fig 6 & Fig 12* ④ ⑤
Q_{gs}	Gate-Source Charge	--	5.8	--		
Q_{gd}	Gate-Drain(" Miller ") Charge	--	13.6	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	-6.5	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	-26		
V_{SD}	Diode Forward Voltage ④	--	--	-5.0	V	T_J=25°C,I_S=-6.5A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	160	--	ns	T_J=25°C,I_F=-6.5A
Q_{rr}	Reverse Recovery Charge	--	0.96	--	μC	di$_F$/dt=100A/μs ④

Notes ;
① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
② L=20mH, I_{AS}=-6.5A, V_{DD}=-50V, R_G=27Ω*, Starting T_J=25°C
③ I_{SD} ≤6.5A, di/dt≤400A/μs, V_{DD}≤BV_{DSS} , Starting T_J=25°C
④ Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%
⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

V_{GS}
Top :   - 15 V
     - 10 V
     -8.0 V
     -7.0 V
     -6.0 V
     -5.5 V
     -5.0 V
Bottom : - 4.5 V

@ Notes :
1. 250 μs Pulse Test
2. T_C = 25 °C

X-axis: $-V_{DS}$, Drain-Source Voltage [V]
Y-axis: $-I_D$, Drain Current [A]
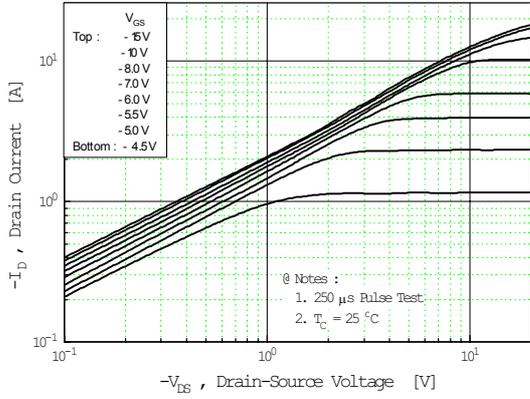
Fig 2. Transfer Characteristics

150 °C
25 °C
- 55 °C

@ Notes :
1. V_{GS} = 0 V
2. V_{DS} = −40 V
3. 250 μs Pulse Test

X-axis: $-V_{GS}$, Gate-Source Voltage [V]
Y-axis: $-I_D$, Drain Current [A]
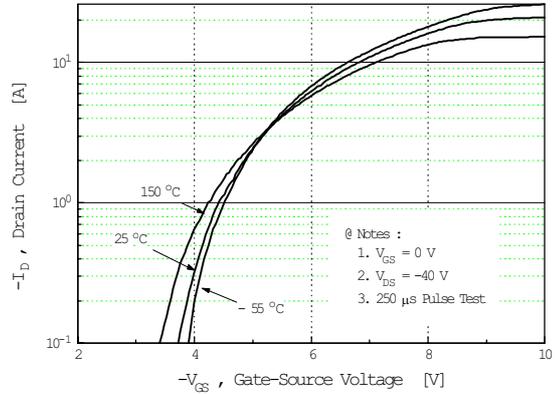
Fig 3. On-Resistance vs. Drain Current

V_{GS} = −10 V
V_{GS} = −20 V

@ Note : T_J = 25 °C

X-axis: $-I_D$, Drain Current [A]
Y-axis: $R_{DS(on)}$, [Ω] Drain-Source On-Resistance
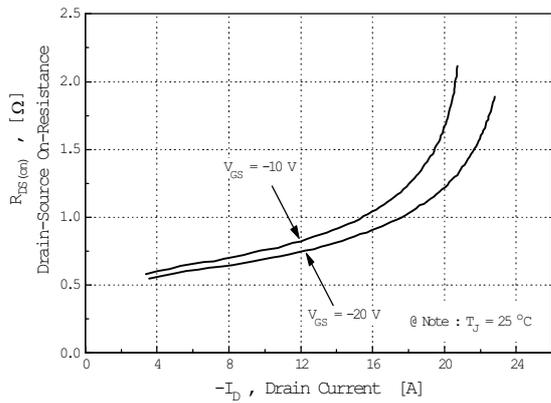
Fig 4. Source-Drain Diode Forward Voltage

150 °C
25 °C

@ Notes :
1. V_{GS} = 0 V
2. 250 μs Pulse Test

X-axis: $-V_{SD}$, Source-Drain Voltage [V]
Y-axis: $-I_{DR}$, Reverse Drain Current [A]
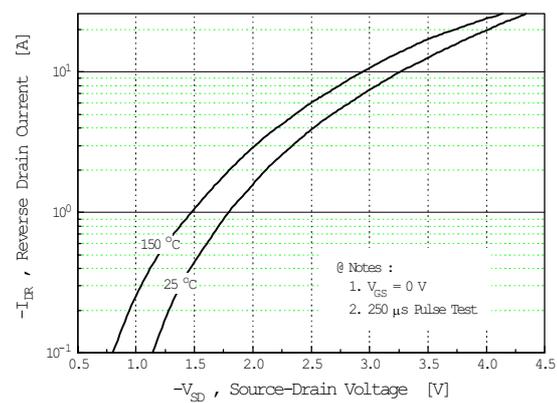
Fig 5. Capacitance vs. Drain-Source Voltage

$C_{iss} = C_{gs} + C_{gd}$ (C_{ds} = shorted)
$C_{oss} = C_{ds} + C_{gd}$
$C_{rss} = C_{gd}$

C_{iss}
C_{oss}
C_{rss}

@ Notes :
1. V_{GS} = 0 V
2. f = 1 MHz

X-axis: $-V_{DS}$, Drain-Source Voltage [V]
Y-axis: Capacitance [pF]
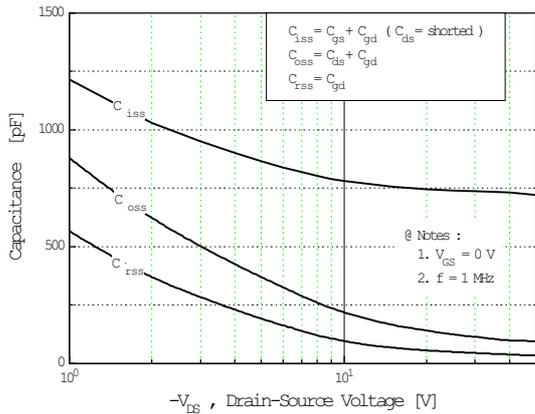
Fig 6. Gate Charge vs. Gate-Source Voltage

V_{DS} = −40 V
V_{DS} = −100 V
V_{DS} = −160 V

@ Notes : I_D =−6.5 A

X-axis: Q_G , Total Gate Charge [nC]
Y-axis: $-V_{GS}$, Gate-Source Voltage [V]
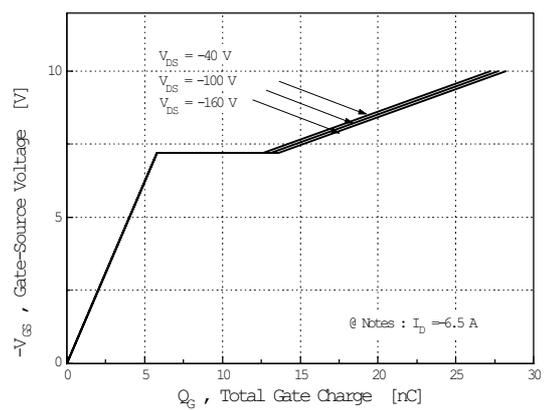
Fig 7. Breakdown Voltage vs. Temperature

Y-axis: $-BV_{DSS}$, (Normalized) Drain-Source Breakdown Voltage

X-axis: T_J , Junction Temperature [°C]

@ Notes :
1. V_{GS} = 0 V
2. I_D = −250 µA
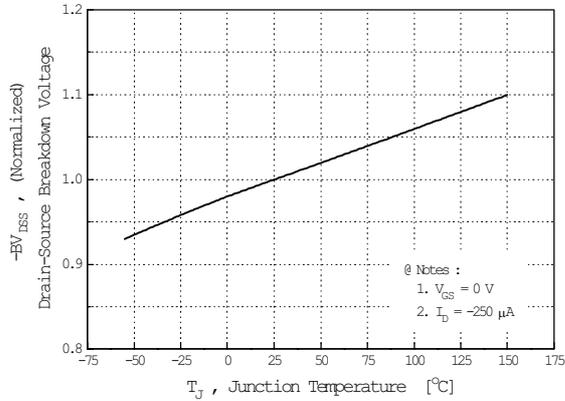
Fig 8. On-Resistance vs. Temperature

Y-axis: $R_{DS(on)}$, (Normalized) Drain-Source On-Resistance

X-axis: T_J , Junction Temperature [°C]

@ Notes :
1. V_{GS} = −10 V
2. I_D = −3.3 A
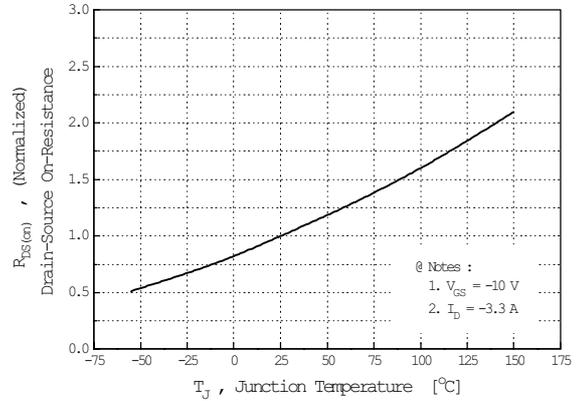
Fig 9. Max. Safe Operating Area

Y-axis: $-I_D$, Drain Current [A]

X-axis: $-V_{DS}$, Drain-Source Voltage [V]

Operation in This Area is Limited by $R_{DS(on)}$

0.1 ms
1 ms
10 ms
DC

@ Notes :
1. T_C = 25 °C
2. T_J = 150 °C
3. Single Pulse
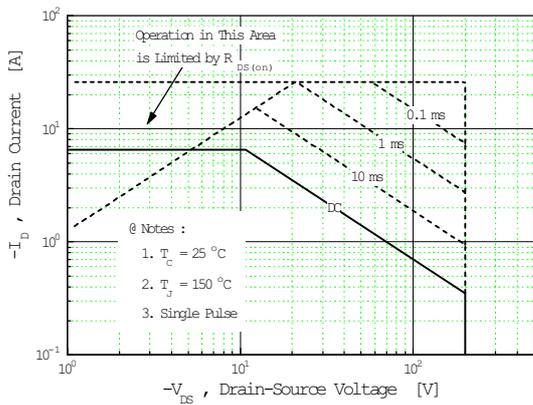
Fig 10. Max. Drain Current vs. Case Temperature

Y-axis: $-I_D$, Drain Current [A]

X-axis: T_C , Case Temperature [°C]

Fig 11. Thermal Response

Y-axis: $Z_{\theta JC}(t)$, Thermal Response

X-axis: t_1 , Square Wave Pulse Duration [sec]

D=0.5
0.2
0.1
0.05
0.02
0.01
single pulse

@ Notes :
1. $Z_{\theta JC}(t)$ = 1.79 °C/W Max.
2. Duty Factor, D=t_1/t_2
3. $T_{JM}-T_C=P_{DM}*Z_{\theta JC}(t)$

P_{DM}
t_1
t_2
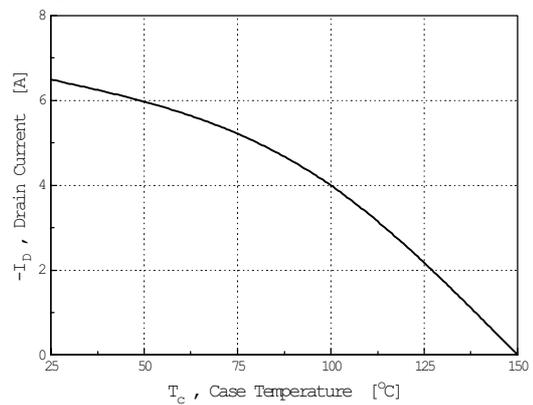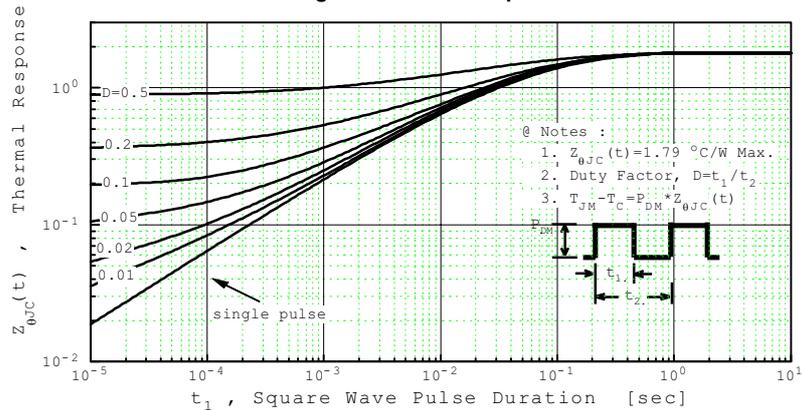
Fig 12. Gate Charge Test Circuit & Waveform

" Current Regulator "

Same Type as DUT

12V   200nF   50KΩ   300nF

V_{GS}

V_{DS}

DUT

-3mA

R_1 R_2

Current Sampling (I_G) Resistor   Current Sampling (I_D) Resistor

V_{GS}

-10V

Q_g

Q_{gs} Q_{gd}

Charge
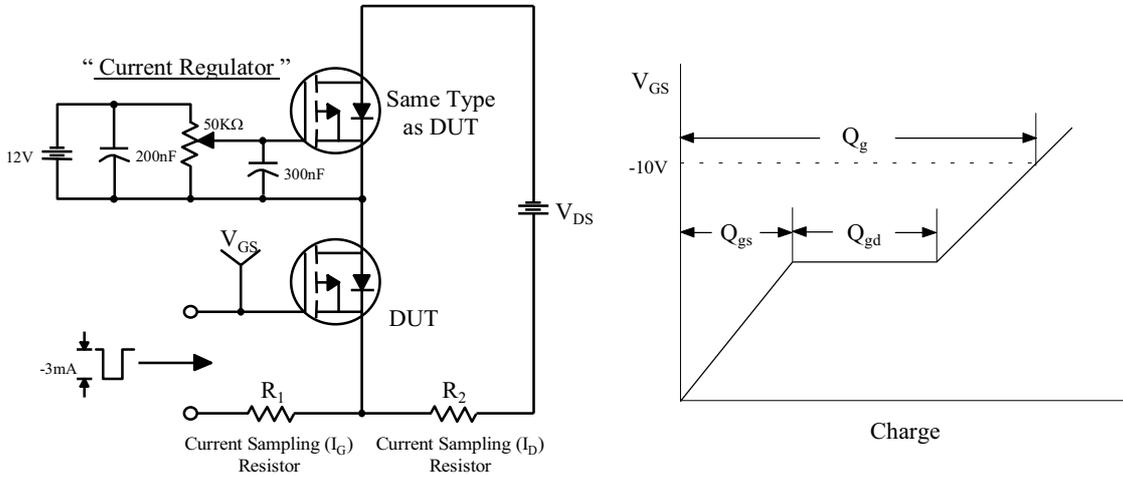
Fig 13. Resistive Switching Test Circuit & Waveforms

V_{out} R_L

V_{in} V_{DD}
(0.5 rated V_{DS})

R_G

DUT

-10V

t_{on} t_{off}

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

V_{in} 10%

V_{out} 90%
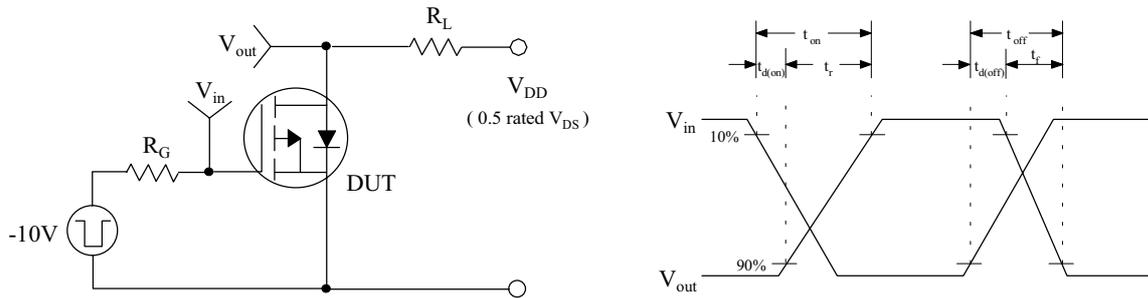
Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

L_L

V_{DS}

I_D

Vary t_p to obtain required peak I_D

R_G C V_{DD}

DUT

-10V

t_p

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} -- V_{DD}}$$

t_p Time

V_{DD} $V_{DS}(t)$

$I_D(t)$

I_{AS}

BV_{DSS}
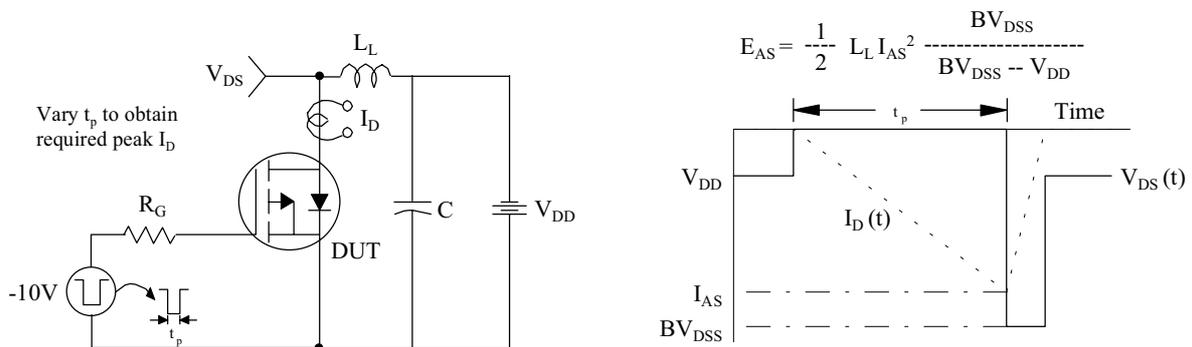
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

V_{DS}

DUT

I_S

L

Driver

V_{GS}

R_G

Compliment of DUT
(N-Channel)

V_{DD}

V_{GS}

• dv/dt controlled by "R_G"
• I_S controlled by Duty Factor "D"

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

Body Diode Reverse Current

I_{RM}

I_S
(DUT)

di/dt

I_{FM} , Body Diode Forward Current

V_f

V_{DS}
(DUT)

Body Diode
Forward Voltage Drop

V_{DD}

Body Diode Recovery dv/dt