

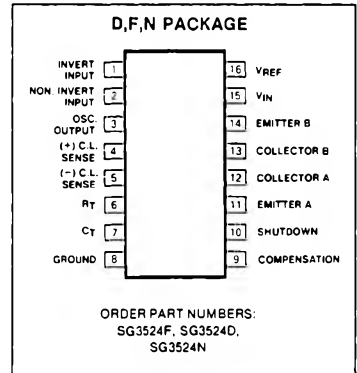
DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

FEATURES

- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Line and load regulation of 0.2%
- 1% maximum temperature variation
- Total supply current is less than 10mA
- Operation beyond 100kHz

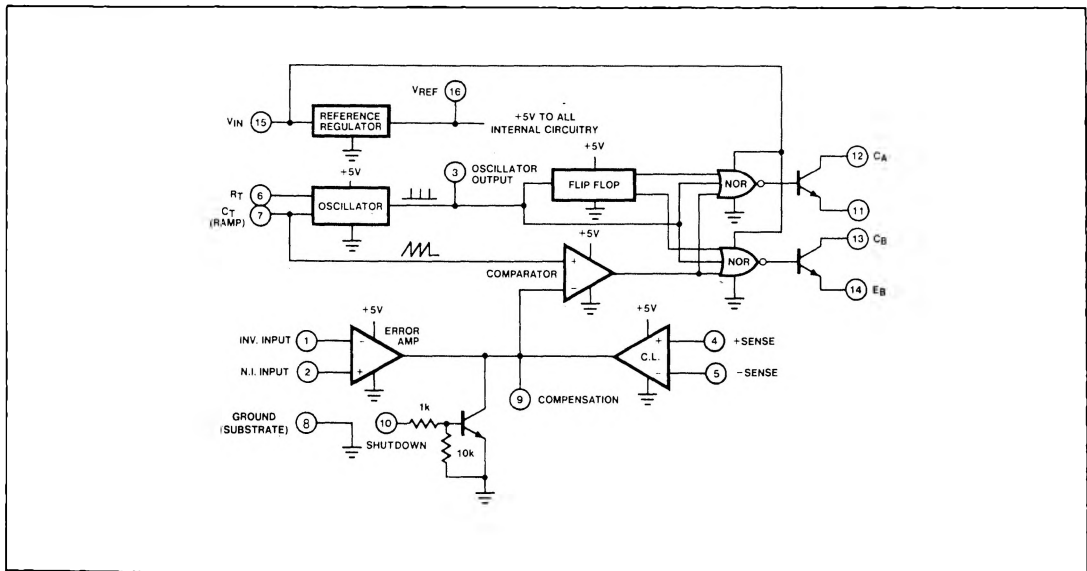
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW/°C
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C

BLOCK DIAGRAM



SMPS CONTROL CIRCUIT

SG3524

DC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{ON} = 20\text{V}$, and $f = 20\text{kHz}$ unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SG3524			UNIT
		Min	Typ	Max	
Reference Section					
Output voltage		4.6	5.0	5.4	V
Line regulation	$V_{IN} = 8$ to 40V		10	30	mV
Load regulation	$I_L = 0$ to 20mA		20	50	mV
Ripple rejection	$f = 120\text{Hz}$, $T_A = 25^\circ\text{C}$		66		dB
Short circuit current limit	$V_{REF} = 0$, $T_A = 25^\circ\text{C}$		100		mA
Temperature stability	Over operating temperature range		0.3	1	%
Long term stability	$T_A = 25^\circ\text{C}$		20		mV/kHr
Oscillator Section					
Maximum frequency	$C_T = .001$ mfd, $R_T = 2\text{k}\Omega$		300		kHz
Initial accuracy	R_T and C_T constant		5		%
Voltage stability	$V_{IN} = 8$ to 40V , $T_A = 25^\circ\text{C}$			1	%
Temperature stability	Over operating temperature range			2	%
Output amplitude	Pin 3, $T_A = 25^\circ\text{C}$		3.5		V_P
Output pulse width	$C_T = .01$ mfd, $T_A = 25^\circ\text{C}$		0.5		μs
Error Amplifier Section					
Input offset voltage	$V_{CM} = 2.5\text{V}$		2	10	mV
Input bias current	$V_{CM} = 2.5\text{V}$		2	10	μA
Open loop voltage gain		68	80		dB
Common mode voltage	$T_A = 25^\circ\text{C}$	1.8		3.4	V
Common mode rejection ratio	$T_A = 25^\circ\text{C}$		70		dB
Small signal bandwidth	$A_V = 0\text{dB}$, $T_A = 25^\circ\text{C}$		3		MHz
Output voltage	$T_A = 25^\circ\text{C}$	0.5		3.8	V
Comparator Section					
Duty cycle	% each output "ON"	0		45	%
Input threshold	Zero duty cycle		1		V
Input threshold	Maximum duty cycle		3.5		V
Input bias current			1		μA
Current Limiting Section					
Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, $T_A = 25^\circ\text{C}$	180	200	220	mV
Sense voltage T.C.			0.2		mV/ $^\circ\text{C}$
Common mode voltage		-1		+1	V
Output Section (each output)					
Collector-emitter voltage (breakdown)		40			V
Collector-leakage current	$V_{CE} = 40\text{V}$		0.1	50	μA
Saturation voltage	$I_C = 50\text{mA}$		1	2	V
Emitter output voltage	$V_{IN} = 20\text{V}$	17	18		V
Rise time	$R_C = 2\text{k}\Omega$, $T_A = 25^\circ\text{C}$		0.2		μs
Fall time	$R_C = 2\text{k}\Omega$, $T_A = 25^\circ\text{C}$		0.1		μs
Total standby current (excluding oscillator charging current, error and current limit dividers, and with outputs open)	$V_{IN} = 40\text{V}$		8	10	mA

THEORY OF OPERATION

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

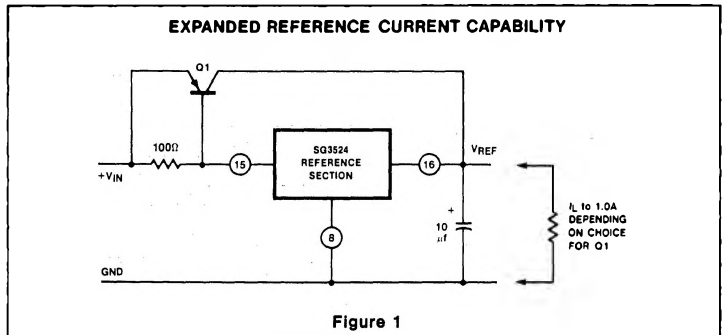
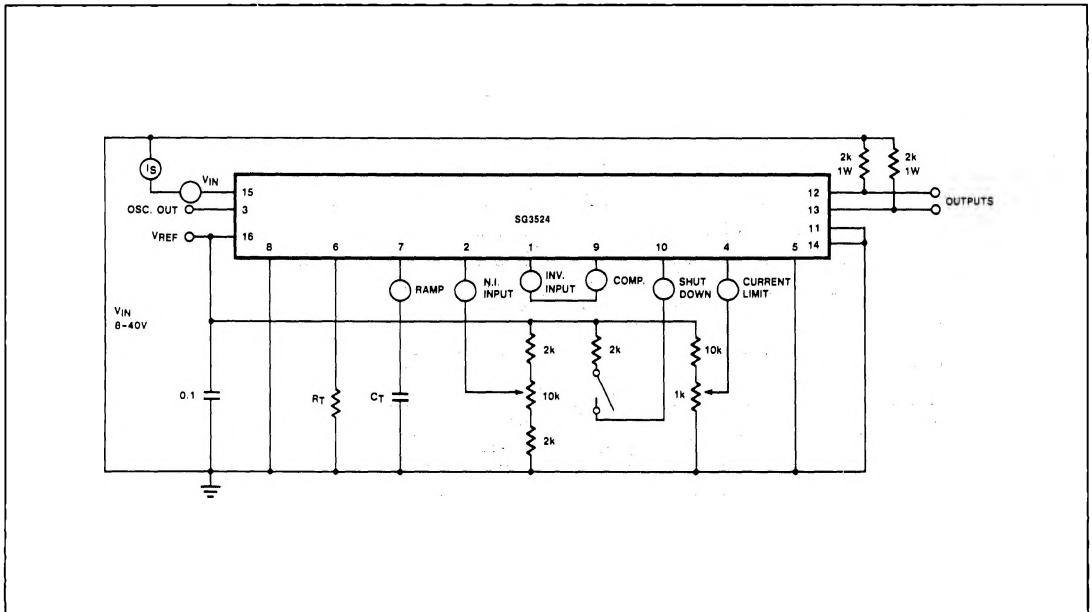


Figure 1

TEST CIRCUIT



OUTPUT STAGE DEAD TIME AS A FUNCTION OF THE TIMING CAPACITOR VALUE

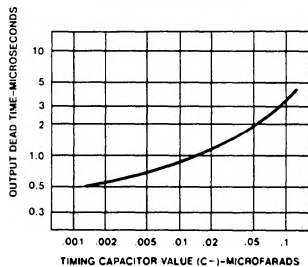


Figure 2

OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

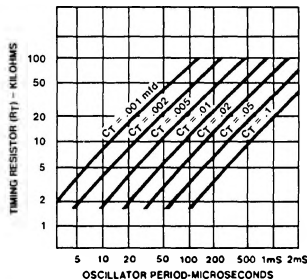


Figure 3

AMPLIFIES OPEN-LOOP GAIN AS A FUNCTION OF FREQUENCY AND LOADING ON PIN 9

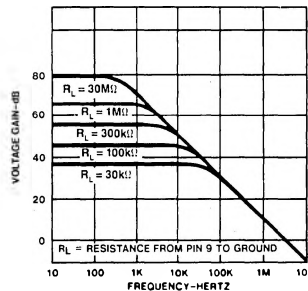


Figure 4

Oscillator

The oscillator in the SG3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The

charging current is equal to 3.6V ÷ R_T and should be kept within the range of approximately 30μA to 2mA, i.e., 1.8K < R_T < 100K.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (≈ 100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately t = R_TC_T where t is in microseconds when R_T = ohms and C_T = microfarads. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the

two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG3524 to an external clock, a pulse of ≈ +3 volts may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more SG3524s must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node (R_L ≈ 5MΩ). The gain is

$$A_v = g_m R_L = \frac{8 I_C R_L}{2kT} \approx .002 R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus .001 microfarad.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

Current Limiting

The current limiting circuitry of the SG3524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R₁:

$$\begin{aligned} \text{Threshold} &= V_{BE}(Q1) + I_1 R_2 - V_{BE}(Q2) \\ &= I_1 R_2 \approx 200\text{mV} \end{aligned}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R₁C₁ and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 11.) Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

***For additional information, consult the Applications Section.**

