FAIRCHILD SEMICONDUCTOR®

October 2008

SG6905
Green Mode PFC/Flyback-PWM Controller

Features

- Interleaved PFC/PWM Switching
- Green Mode PWM Operation
- Low Startup and Operating Current
- Innovative Switching-Charge Multiplier-Divider
- Average-Current-Mode Control for PFC
- PFC Over-Voltage and Under-Voltage Protections
- PFC Remote On/Off Control
- PFC and PWM Feedback Open-Loop Protection
- Cycle-by-Cycle Current Limiting for PFC/PWM
- Slope Compensation for PWM
- Constant Power Limit for PWM
- Power-On Sequence Control
- Brownout Protection
- Over-Temperature Protection

Applications

- Switching Power Suppliers with Active PFC
- High-Power Adaptors
- LCD TV Applications

Description

The highly integrated SG6905 is specially designed for power supplies consisting of boost PFC and flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections. It is available in 20-pin SOP package.

The proprietary interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6905 shuts off PFC to prevent extra-high voltage on output.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

During startup, the RDY (ready) is pulled low until the PFC output voltage reaches the setting level. This signal can be used to control the second power stage for proper power-on sequence.

In addition, SG6905 provides complete protection functions, such as brownout protection and RI pin open/short.

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status	Packing Method
SG6905SY	-40°C to +105°C	20-pin Small Outline Package (SOP)	Green	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

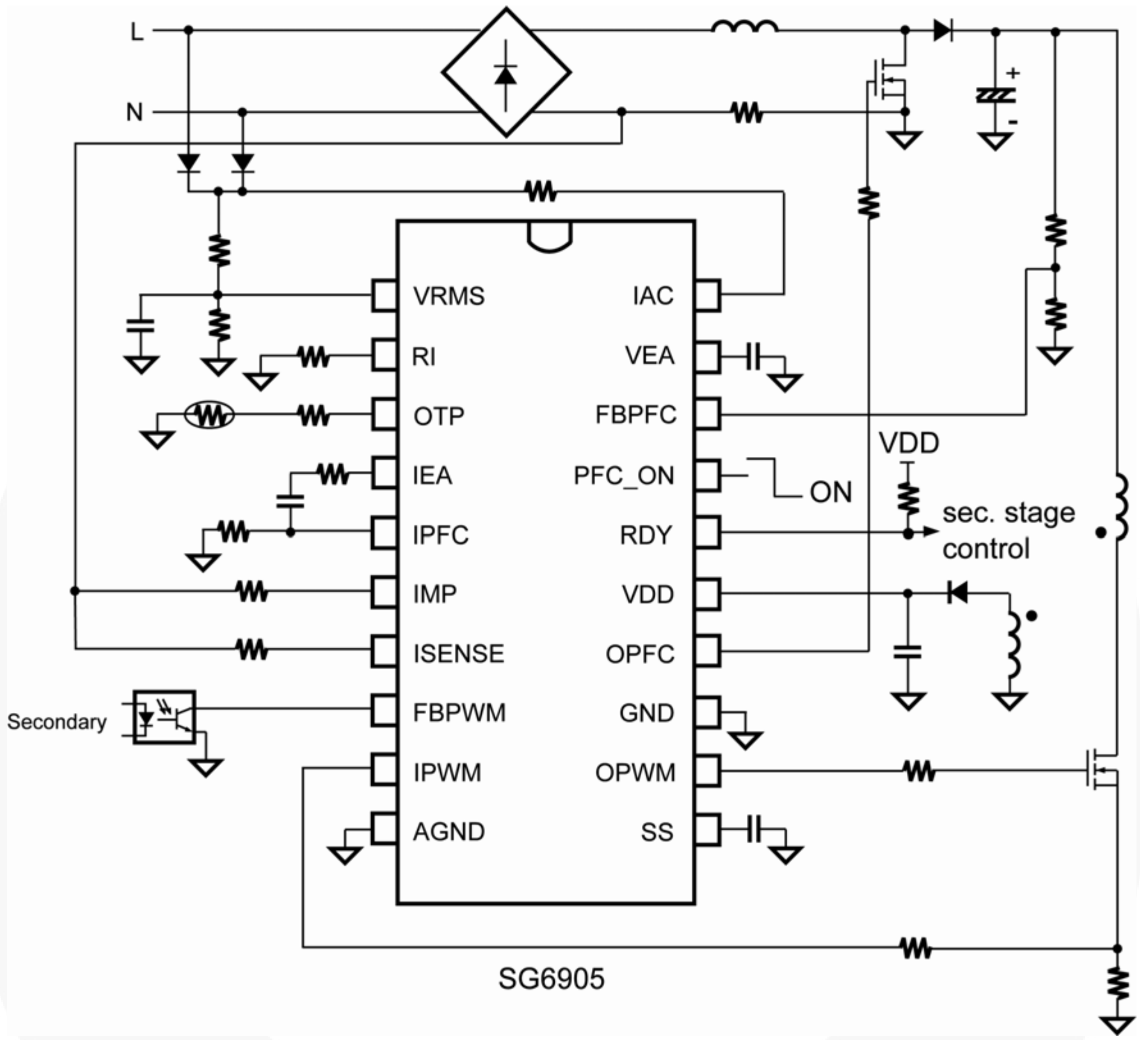


Figure 1. Typical Application

Block Diagram

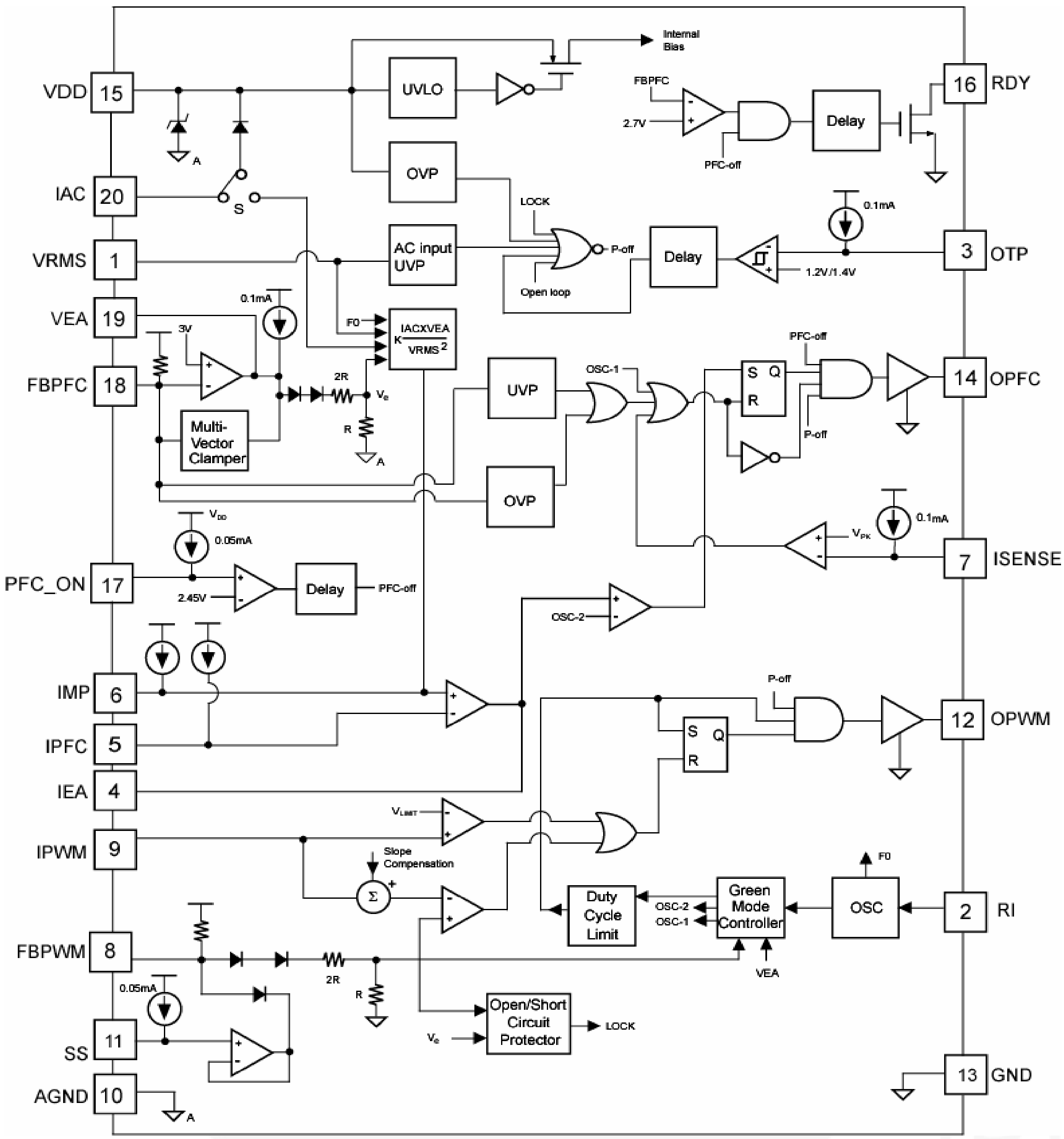
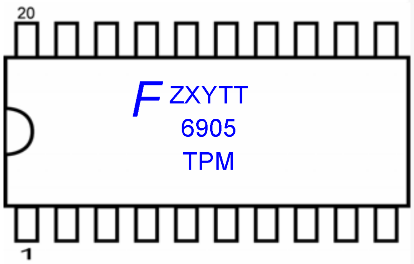


Figure 2. Function Block Diagram

Marking Information



F- Fairchild Logo
Z- Plant Code
X- Year Code
Y- Week Code
TT: Die-Run Code
T: Package Type (S=SOP)
P: Y: Green Package
M: Manufacture Flow Code

Figure 3. Marking Information

Pin Configuration

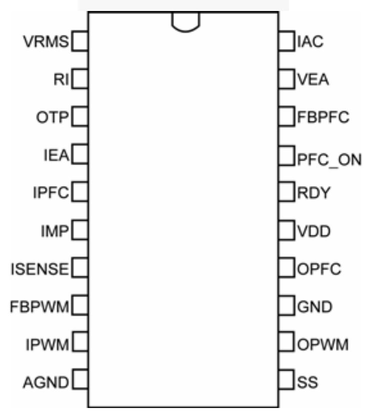


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	VRMS	**Line Voltage Detection**. The pin is used for PFC multiplier, brownout protection. For brownout protection, the controller is disabled after a delay time when the VRMS voltage drops below a threshold.
2	RI	**Reference Setting**. One resistor connected between RI and ground determines the switching frequency. The switching frequency is equal to [1560 / R_I]KHz, where R_I is in kΩ. For example, if R_I is equal to 24kΩ, then the switching frequency is 65KHz.
3	OTP	**Over-Temperature Protection**. This pin supplies an over-temperature-protection signal. A constant current is output from this pin. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6905 is disabled.
4	IEA	**Output for PFC Current Amplifier**. This is the output of the PFC current amplifier. The signal from this pin is compared with an internal saw-tooth and hence determines the pulse width for PFC gate drive.
5	IPFC	**Inverting Input for PFC Current Amplifier**. The inverting input of the PFC current amplifier. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
6	IMP	**Non-Inverting Input for PFC Current Amplifier**. The non-inverting input of the PFC current amplifier and also the output of multiplier. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
7	ISENSE	**Peak Current Limit Setting for PFC**.
8	FBPWM	**PWM Feedback Input**. The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a 6.5kΩ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
9	IPWM	**PWM Current Sense**. The current-sense input for the flyback PWM. Via a current-sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
10	AGND	**Ground.** Signal ground.
11	SS	**PWM Soft-Start**. During startup, the SS pin charges an external capacitor with a 50µA (R_I=24kΩ) constant current source. The voltage on FBPWM is clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin is quickly discharged.
12	OPWM	**PWM Gate Drive**. The totem-pole output drive for the flyback PWM MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
13	GND	**Ground.** Power ground.
14	OPFC	**PFC Gate Drive.** The totem-pole output drive for the PFC MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
15	VDD	**Supply**. The power-supply pin.
16	RDY	**Ready-Signal Output**. This pin outputs a ready signal to control the power-on sequence. Once the SG6905 is turned on and the FBPFC (PFC feedback input) voltage is higher than 2.7V, the pin locks to HIGH impedance. Disabling the SG6905 resets this pin to LOW.
17	PFC_ON	**Remote On/Off**. The PFC stage disables whenever the voltage at this pin exceeds 2.45V.
18	FBPFC	**Voltage Feedback Input for PFC**. The feedback input for PFC voltage loop. The inverting input of PFC error-amp. This pin is connected to the PFC output through a divider network.
19	VEA	**Error-Amp Output for PFC Voltage Feedback Loop**. The error-amp output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and hence improves the power factor.
20	IAC	**Input AC Current**. Before startup, this input is used to provide startup current for V_{DD}. For normal operation, this input is used to provide current reference for the multiplier.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltage, are given with respect to GND pin. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		25	V
I_{AC}	Input AC Current		2	mA
V_{HIGH}	OPWM, OPFC, IAC Pin	-0.3	25.0	V
V_{LOW}	Others Pin	-0.3	7.0	V
P_D	Power Dissipation At T_A < 50°C		800	mW
T_J	Operating Junction Temperature	-40	+105	°C
θ_{JC}	Thermal Resistance (Junction-to-Case)		23.64	°C/W
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature (Wave soldering, or IR 10 seconds)		+260	°C
ESD	Human Body Model, JESD22-A114		3.5	KV
	Charged Device Model, JESD22-C101		1250	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	-40		+105	°C

Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{DD-OP}	Continuous Operation Voltage				20	V
V_{DD-ON}	Turn-On Threshold Voltage		15	16	17	V
V_{DD-OFF}	Turn-Off Threshold Voltage		9	10	11	V
I_{DD-ST}	Startup Current	V_{DD}=V_{DD-ON} – 0.16V		10	25	µA
I_{DD-OP}	Operating Supply Current	V_{DD}=15V; OFC, OPWM open		6	10	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection Level		23.5	24.5	25.5	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce	R_I=24kΩ	8		25	µs
RI Section						
V_{RI}	RI Voltage		1.17	1.20	1.23	V
RI	RI Pin Resistance Range		15.6		47.0	kΩ
RI_{OPEN}	RI Pin Open Protection If R_I > RI_{open}, SG6905 turns OFF	R_I=24kΩ			200	kΩ
RI_{SHORT}	RI Pin Short Protection If R_I < RI_{short}, SG6905 turns OFF	R_I=24kΩ	2			kΩ
VRM Section						
$V_{RMS-UVP-1}$	RMS AC-Voltage Under-Voltage Protection Threshold (with T_{UVP} Delay)		0.75	0.80	0.85	V
$V_{RMS-UVP-2}$	Recovery Level on VRMS		$V_{RMS-UVP-1}$+0.17V	$V_{RMS-UVP-1}$+0.19V	$V_{RMS-UVP-1}$+0.21V	V
t_{UVP}	Under-Voltage-Protection Delay Time (No Delay for Startup)	R_I=24kΩ	150	195	240	ms
t_{D-PWM}	UVP Occurs, the Interval from PFC Off to PWM Off	R_I=24kΩ	$t_{UVP-Min}$+9		$t_{UVP-Min}$+14	ms

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Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PFC Stage						
Voltage Error Amplifier Section						
V_{REF}	Reference Voltage		2.95	3.00	3.05	V
Av	Open-Loop Gain			60		db
OVP_{FBPFC}	PFC Over-Voltage-Protection on FBPFC		V_{REF}+ 0.15	V_{REF}+ 0.25	V_{REF}+ 0.30	V
ΔOVP_{PFC}	PFC Feedback-Voltage-Protection Hysteresis		60	90	120	mV
$t_{OVP-PFC}$	Debounce Time of PFC OVP		40	70	120	µs
UVP_{FBPFC}	PFC Feedback Under Voltage Protection		0.35	0.40	0.45	V
$t_{UVP-PFC}$	Debounce Time of PFC UVP		40	70	120	µs
GM	Trans-Conductor		35	50	65	mho
$I_{FBPFC-L}$	Maximum Source Current		28	34		µA
$I_{FBPFC-H}$	Maximum Sink Current		28	34		µA
V_{FBHIGH}	FB Open Voltage		6.0	6.3	6.6	V
Current Error Amplifier Section						
V_{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
A_I	Open-Loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common-Mode Rejection Ratio	V_{CM}=0 to +1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	R_I=24kΩ (I_{MR}=20+I_{RI}*0.8)	50		70	µA
I_L	Maximum Source Current		3			mA
I_H	Maximum Sink Current		0.15	0.25	0.30	mA
Peak Current Limit Section						
I_P	Constant Current Output	R_I=24KΩ	90	100	110	µA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{SENSE} < V_{PK})	V_{RMS}=1.05V	0.15	0.20	0.25	V
		V_{RMS}=3V	0.35	0.40	0.45	V
t_{PD-PFC}	Propagation Delay				200	ns
$t_{LEB-PFC}$	Leading-Edge Blanking Time		70	120	170	ns

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Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PFC Stage						
Multiplier Section						
I_{AC}	Input AC Current	Multiplier Range	0		360	μA
I_{MO-max}	Maximum Multiplier Current Output	R_I=24kΩ	230	250		μA
I_{MO-1}	Multiplier Current Output (Low-Line, High-Power)	V_{RMS}=1.05V; I_{AC}=90μA; V_{EA}=5V; R_I=24kΩ	200	250	280	μA
I_{MO-2}	Multiplier Current Output (High-Line, High-Power)	V_{RMS}=3V; I_{AC}=264μA; V_{EA}=5V; R_I=24kΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V
PFC Oscillator Section						
f_{OSC}	PFC Frequency	R_I=24kΩ	62	65	68	KHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11 to 20V			2	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-20 to 85°C			2	%
PFC Output Driver Section						
V_Z	Output-Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PFC}	Output-Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
V_{OH-PFC}	Output-Voltage High		8			V
t_{PFC}	The interval of OPFC Lags behind OPWM at Startup	V_{DD}=13V; I_O=100mA	8.0	11.0	13.5	ms
t_{R-PFC}	Rising Time	V_{DD}=15V; C_L=5nF; O/P=2V to 9V	40	70	120	ns
t_{F-PFC}	Falling Time	V_{DD}=15V; C_L=5nF; O/P=9V to 2V	40	60	110	ns
DCY_{MAX}	Maximum Duty Cycle		93		98	%
PFC On/Off Section						
$I_{ON/OFF}$	Constant Current Output for PFC_ON Pin	R_I=24kΩ	44	50	56	μA
V_{OFF}	Turn-Off Threshold Voltage		2.00	2.45	2.90	V
t_{PFC_ON}	Debounce Time of PFC_On/Off	R_I=24kΩ	40	70	120	μs

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Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM Stage						
FBPWM Section						
$A_{v\text{-}PWM}$	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB}	Input Impedance		4	5	7	kΩ
I_{FB}	Maximum Source Current		0.8	1.2	1.5	mA
$FB_{OPEN\text{-}LOOP}$	PWM Open-Loop Protection Voltage		4.2	4.5	4.8	V
$t_{OPEN\text{-}PWM}$	PWM Open-Loop Protection Delay Time	R_I=24kΩ	45	56	70	ms
$t_{OPEN\text{-}PWM\text{-}DLY}$	PWM Off to Turn On Delay Time		450	600	750	ms
S_G	Green-Mode Modulation Slope	PFC_ON > VOFF	80	100	120	Hz/V
$V_{FB\text{-}N}$	Frequency Reduction Threshold on FBPWM	PFC_ON > VOFF	1.8	2.0	2.2	V
$V_{FB\text{-}G}$	Voltage on FBPWM at f_S = 20KHz	PFC_ON > VOFF	1.35	1.60	1.75	V
$V_{OZ\text{-}NG}$	Voltage of FBPWM < V_{OZ} Gate Turn Off	PFC_ON < VOFF		0.6		V
PWM-Current Sense Section						
$t_{PD\text{-}PWM}$	Propagation Delay to Output	V_{DD}=15V OPWM ≤ 9V	50		120	ns
V_{LIMIT}	Peak Current Limit Threshold Voltage1		0.85	0.90	0.95	V
$t_{LEB\text{-}PWM}$	Leading-Edge Blanking Time		170	250	350	ns
ΔV_{SLOPE}	Slope Compensation $\Delta V_S = DV_{SLOPE}$ x (T_{on}/T) ΔV_S: Compensation Voltage Added to Current Sense		0.30	0.33	0.36	V
PWM Oscillator Section						
f_{OSC}	PWM Frequency	R_I=24kΩ	62	65	68	V
$f_{OSC\text{-}MIN}$	Minimum Frequency	R_I=24kΩ; FBPWM=V_G; PFC_ON > VOFF	19.0	21.0	23.5	V
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11 to 20V			2	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-20 to 85°C			2	%
PWM Output Driver Section						
$V_{Z\text{-}PWM}$	Output-Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
$V_{OL\text{-}PWM}$	Output-Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
$V_{OH\text{-}PWM}$	Output-Voltage High	V_{DD}=13V; I_O=100mA	8			V
$t_{r\text{-}pwm}$	Rising Time	V_{DD}=15V; C_L=5nF; O/P=2V to 9V	30	60	120	ns
$t_{f\text{-}pwm}$	Falling Time	V_{DD}=15V; C_L=5nF; O/P=9V to 2V	30	50	110	ns
DCY_{MAXPWM}	Maximum Duty Cycle		73	78	83	%

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Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
RDY Section						
$V_{FB\text{-}RDY\text{-}HIGH}$	RDY is a High Impedance at the Voltage of FBPFC>$V_{FB\text{-}RDY\text{-}HIGH}$ and PFC_ON Low		2.6	2.7	2.8	V
$I_{FB\text{-}RDY\text{-}HIGH}$	The Leakage Current of RDY is a High Impedance at the Voltage of FBPFC	FBPFC=2V			10	µA
V_{OL}	Output-Voltage Low for RDY is Failed	I_{SINK}=1mA			0.5	V
OTP Section						
I_{OTP}	OTP Pin Output Current	R_I=24kΩ	90	100	110	µA
$V_{OTP\text{-}ON}$	Recovery Level on OTP		1.35	1.40	1.45	V
$V_{OTP\text{-}OFF}$	OTP Threshold Voltage		1.15	1.20	1.25	V
t_{otp}	OTP Debounce Time	R_I=24kΩ	8		25	µs
Soft-Start Section						
I_{SS}	Constant Current Output for Soft-Start	RT=24kΩ	44	50	56	µA
R_D	Discharge R_{DSon}	FBPWM=$FB_{OPEN\text{-}LOOP}$		470		Ω

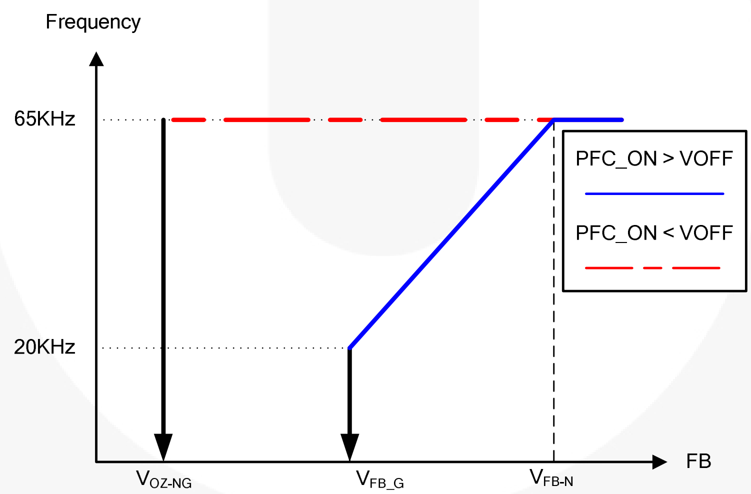

Figure 5. PWM Frequency

Function Protection Table

Item	PWM GATE	PFC GATE	RDY Pin
PFC_ON exceed V_{OFF}	No change	OFF	Short to ground
OTP	OFF	OFF	Short to ground
Brownout	OFF	OFF	Short to ground
OVP(PFC)	No change	OFF	Open drain
UVP(PFC)	No change	OFF	Short to ground
IMP open	No change	OFF	Short to ground
PWM open loop	OFF	OFF	Short to ground
SS Pin pull low(=0V)	OFF	OFF	Short to ground
RI Pin open	OFF	OFF	Short to ground

Note:

1. The PFC stage is disabled, whenever the voltage at PFC_ON pin exceeds V_{OFF}.
2. The RDY Pin is reset, whenever the voltage at PFC_ON pin exceeds V_{OFF} or UVP_{FBPFC}, OVP_{FBPFC}, V_{IMP}, $V_{RMS-UVP}$ occur, IC V_{DD} reaches V_{DD-MIN}.

Green Mode Function

Item	PWM	PFC
PFC_ON	×	×
PFC_OFF	O	×

Typical Performance Characteristics

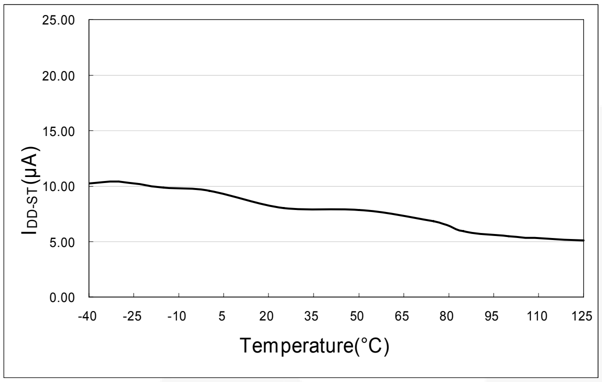

Figure 6. I_{DD-ST} vs. T_A

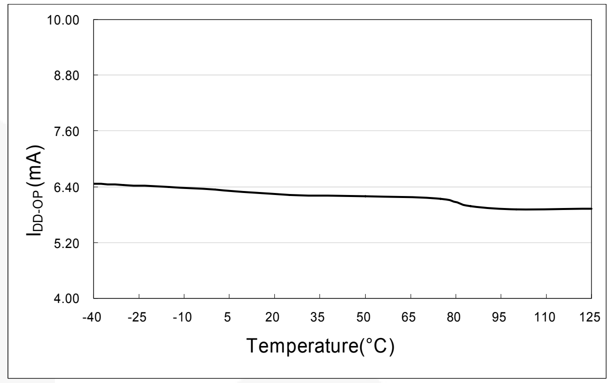

Figure 7. I_{DD-OP} vs. T_A

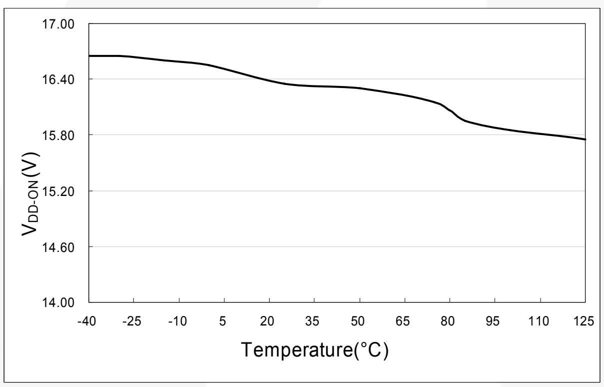

Figure 8. V_{DD-ON} vs. T_A

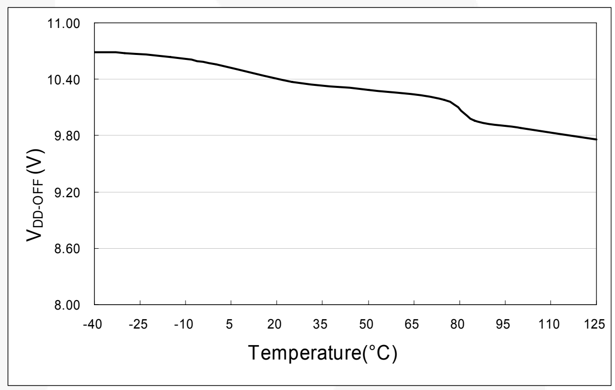

Figure 9. V_{DD-OFF} vs. T_A

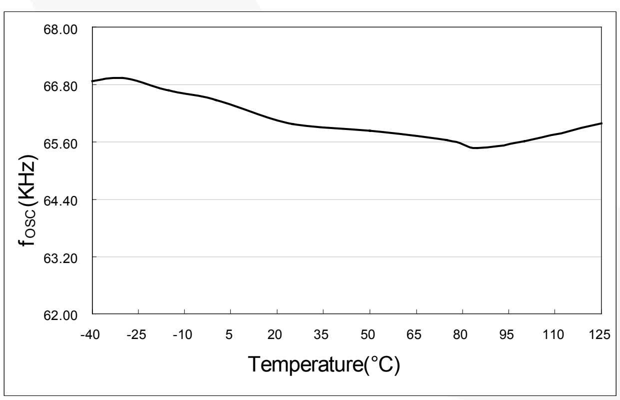

Figure 10. f_{OSC} vs. T_A

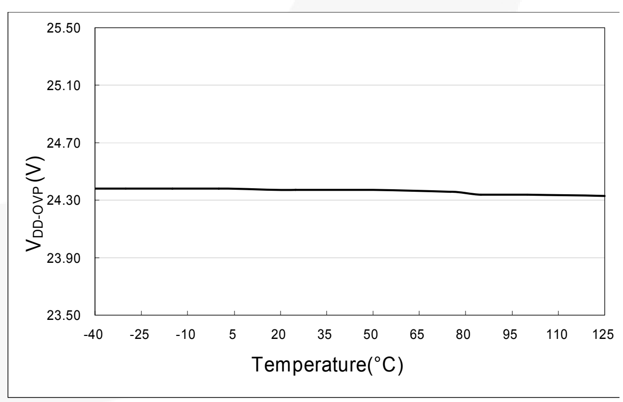

Figure 11. V_{DD-OVP} vs. T_A

Typical Performance Characteristics (Continued)

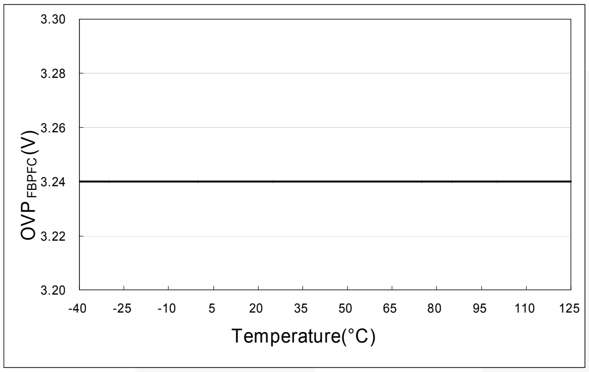

Figure 12. OVP_{FBPFC} vs. T_A

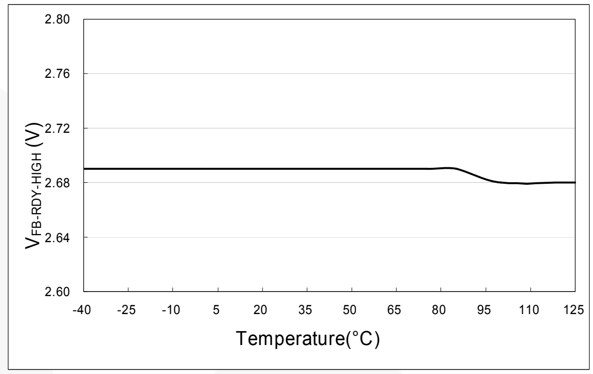

Figure 13. $V_{FB\text{-}RDY\text{-}HIGH}$ vs. T_A

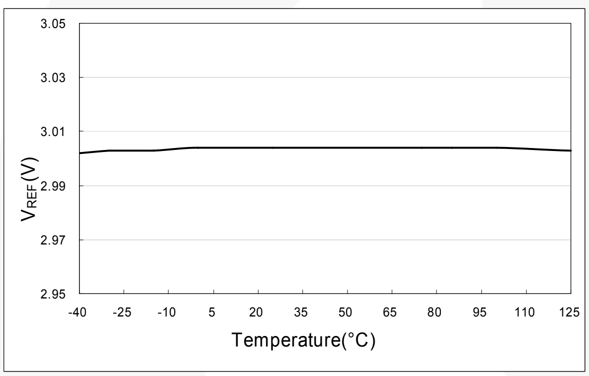

Figure 14. V_{REF} vs.. T_A

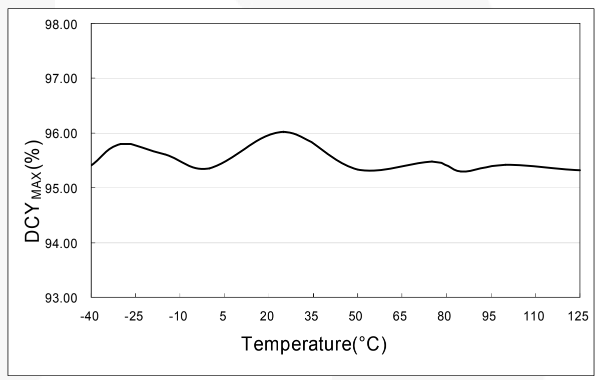

Figure 15. DCY_{MAX} vs. T_A

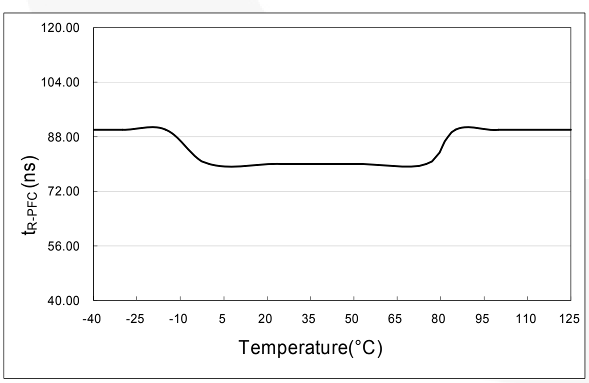

Figure 16. $t_{R\text{-}PFC}$ vs. T_A

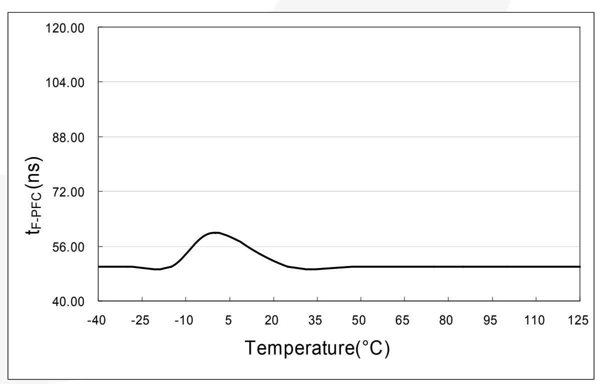

Figure 17. $t_{F\text{-}PFC}$ vs. T_A

Typical Performance Characteristics (Continued)

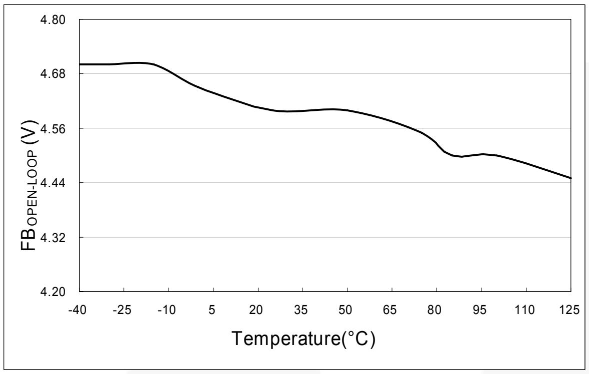

Figure 18. $FB_{OPEN-LOOP}$ vs. T_A

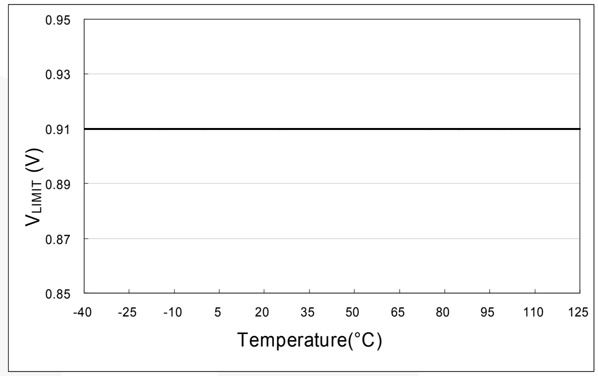

Figure 19. V_{LIMIT} vs. T_A

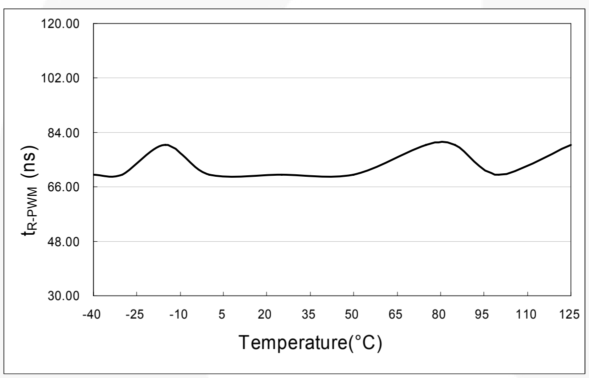

Figure 20. t_{R-PWM} vs. T_A

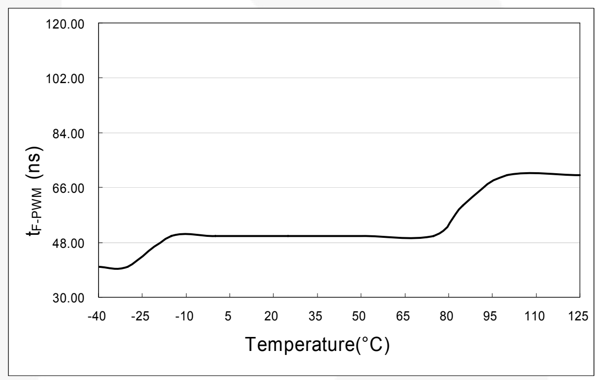

Figure 21. t_{F-PWM} vs. T_A

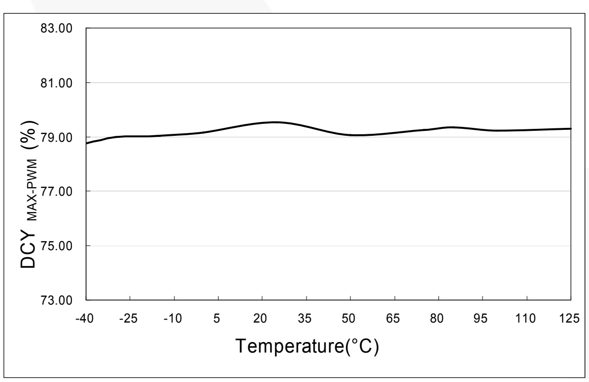

Figure 22. $DCY_{MAX-PWM}$ vs. T_A

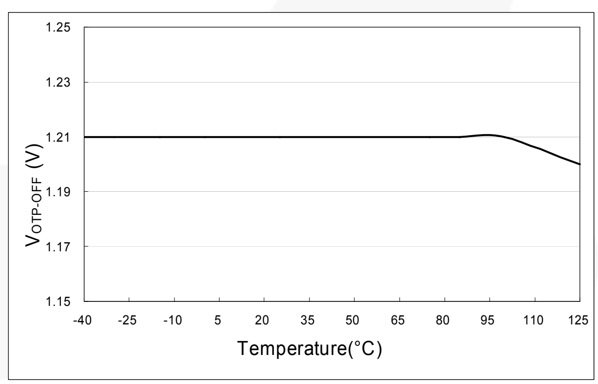

Figure 23. $V_{OTP-OFF}$ vs. T_A

Functional Description

The highly integrated SG6905 is specially designed for power supplies consisting of boost PFC and flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections. It is available in a 20-pin SOP package.

The proprietary interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption.

For the PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6905 shuts off PFC to prevent extra-high voltage on output.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

During startup, the RDY pin is pulled low until the PFC output voltage reaches the setting levels. This signal can be used to control the second power stage for proper power-on sequence.

In addition, SG6905 provides complete protection functions, such as brownout protection and RI pin open/short.

PFC ON/OFF Control and RDY Signal for Power-ON Sequence Control

A PFC on/off control function is built in to control the power on and power off of the PFC controller. Once the voltage on this pin is pulled below 2.45V, the OPFC is enabled. Once the OPFC is enabled, the output voltage of the PFC converter gradually increases to the regulated voltage. To provide a proper power-on-sequence control, a RDY pin is pulled high after the PFC voltage reaches 90% (FBPFC>$V_{FB\text{-}RDY\text{-}HIGH}$) of its regulated voltage.

Startup

Figure 24 shows the startup circuit of the SG6905. A resistor R_{AC} is utilized to charge the V_{DD} capacitor through S1. The turn-on and turn-off threshold of SG6905 are fixed internally at 16V/10V. During startup, the hold-up capacitor must be charged to 16V through the startup resistor so that SG6905 is enabled. The hold-up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer flyback converter. V_{DD} must not drop below 10V during this startup process. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply V_{DD} during startup. Since SG6905 consumes less than 25μA startup current, the value of R_{AC} can be large to reduce power consumption. One 10μF capacitor should hold enough energy for successful startup. After startup, S1 switches so that the current I_{AC} is the input for the PFC multiplier. This helps reduce circuit complexity and power consumption.

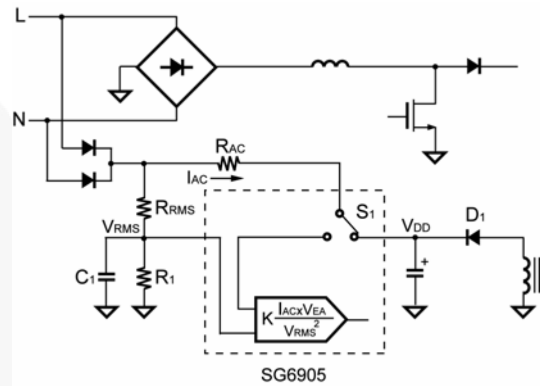

Figure 24. Startup Circuit of the SG6905

Switching Frequency and Current Sources

The switching frequency of SG6905 can be programmed by the resistor R_I connected between the RI and GND pins. The relationship is:

$$f_{OSC} = \frac{1560}{R_I\ (k\Omega)}(KHz) \qquad (1)$$

For example, a 24kΩ resistor R_I results in a 65KHz switching frequency. Accordingly, a constant current I_T flows through R_I.

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \qquad (2)$$

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 25 shows a resistive divider with low-pass filtering for line-voltage detection on the VRMS pin. The V_{RMS} voltage is used for the PFC multiplier and brownout protection.

For brownout protection, the SG6905 is disabled with 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier, please refer to below section for more details.

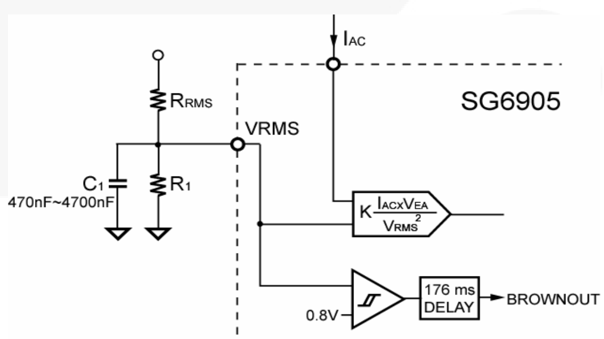

Figure 25. Line Voltage Detection Circuit

Interleave Switching

The SG6905 uses interleaved switching to synchronize the PFC and flyback stages. This reduces switching noise and spreads the EMI emissions. Figure 26 shows that an off-time t_{OFF} is inserted between the turn-off of the PFC gate drive and the turn-on of the PWM.

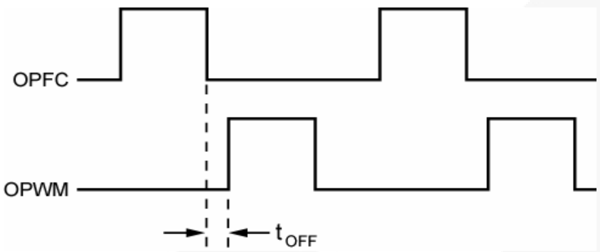

Figure 26. Line-Voltage Detection Circuit

PFC Operation

The purpose of a boost active Power Factor Corrector (PFC) is to shape the input current of a power supply. The input-current waveform and phase follows that of the input voltage. Using SG6905, average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching charge multiplier/divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 27 shows the total control loop for the average-current-mode control circuit of SG6905.

The current source output from the switching charge multiplier/divider can be expressed as:

$$I_{MO} = K \bullet \frac{I_{AC} \bullet V_{EA}}{V_{RMS}{}^2}(\mu A) \qquad (3)$$

Refer to Figure 27, the current output from IMP pin, I_{MP}, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical fixed current sources. They are used to pull HIGH the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground. The constant current sources I_{MR1} and I_{MR2} are typically 60µA.

Through the differential amplification of the signal across R_S, better noise immunity is achieved. The output of IEA is compared with an internal sawtooth and hence the pulse width for PFC is determined. Through the average current-mode control loop, the input current I_S is proportional to I_{MO}.

$$I_{MO} \bullet R_2 = I_S \bullet R_S \qquad (4)$$

There are different concerns in determining the value of the sense resistor R_S The value of R_S should be small to reduce power consumption, but it should be large enough to maintain the resolution. A current transformer (CT) may be used to improve the efficiency of high power converters.

There are two major concerns when compensating the voltage-loop error amplifier (V_{EAO}): stability and transient response. Optimizing interaction between stability and transient response requires that the error amplifier's open-loop crossover frequency be half that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency). The gain vs. input voltage of the SG6905's voltage error amplifier (V_{EAO}) has a specially shaped non-linearity, so that under steady-state operating conditions the transconductance of the error amplifier is at a local minimum. Rapid perturbation in line or load conditions causes the input to the voltage error amplifier (V_{FB}) to deviate from its 3V (nominal) value. If this happens, the transconductance of the voltage error amplifier increases significantly. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with conventional linear gain characteristics.

The voltage loop gain(s) is given by:

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} \bullet \frac{\Delta V_{FB}}{\Delta V_{OUT}} \bullet \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$
$$\approx \frac{P_{IN} \bullet 3}{V^2_{OUTDC} \bullet \Delta V_{EAO} \bullet S \bullet C_{DC}} \bullet GM_V \bullet Z_C \qquad (5)$$

where:

Z_C: Compensation network for the voltage loop.

GM_V: Transconductance of VEAO.

P_{IN}: Average PFC input power.

V_{2OUTDC}: PFC boost output voltage (typical designed value is 380V).

C_{DC}: PFC boost output capacitor.

The average total input power can be expressed as:

$$P_{IN} = V_{IN}(rms) \times I_{IN}(rms)$$
$$\propto V_{RMS} \times I_{MO} \propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}{}^2} \qquad (6)$$
$$\propto V_{RMS} \times \frac{\frac{V_{IN}}{R_{AC}} \times V_{EA}}{V_{RMS}{}^2} = \sqrt{2} \times \frac{V_{EA}}{R_{AC}}$$

From equation 6, V_{EA}, the output of the voltage error amplifier, actually controls the total input power and hence the power delivered to the load.

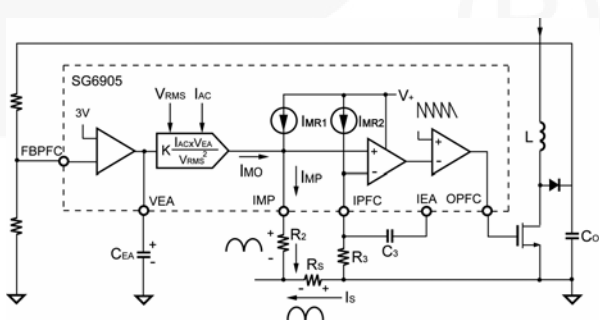

Figure 27. Average Current Mode Control Loop

Cycle-by-Cycle Current Limiting

SG6905 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 28 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on ISENSE pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and VRMS is also shown in Figure 28.

The amplitude of the constant current I_P is determined by the internal current reference according to the following equation:

$$I_{SENSE\_peak} = \frac{(I_P \bullet R_P) - 0.2V}{R_S} \quad (7)$$

therefore the peak current of the I_{SENSE} is given by (V_{RMS}<1.05V)

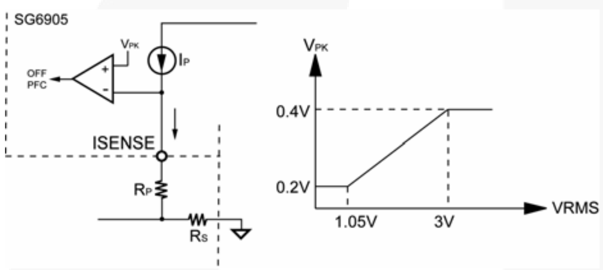

Figure 28. V_{RMS} Controlled Current Limiting

Flyback PWM and Slope Compensation

As shown in Figure 29, peak-current-mode control is utilized for flyback PWM. The SG6905 inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous-current-mode operation.

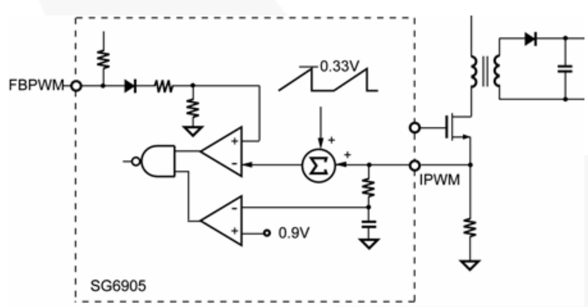

Figure 29. Peak Current Control Loop

When the IPWM voltage across the sense resistor reaches the threshold voltage (0.9V), the OPWM is turned off after a small propagation delay t_{PD-PWM}.

To improve stability or prevent sub-harmonic oscillation, a synchronized positive-going ramp is inserted at every switching cycle.

Limited Power Control

When the output power supply is shorted or over loaded, the FBPWM voltage increases. If the FBPWM voltage is higher than a designed threshold, $FB_{OPEN-LOOP}$ (4.5V), for longer than $t_{OPEN-PWM}$ (56ms), the OPWM is turned off. As OPWM is turned off, the supply voltage V_{DD} begins decreasing.

When V_{DD} is lower than the turn-off threshold, V_{DD-OFF} (10V), SG6905 is totally shut down. Due to the startup resistor, V_{DD} is charged up to the turn-on threshold voltage, V_{DD-ON} (16V), until SG6905 is enabled again. If the overloading condition still exists, the protection takes place repeatedly. This prevents the power supply from being overheated under overloading conditions.

Over-Temperature Protection (OTP)

SG6905 provides an OTP pin for over-temperature protection. A constant current is output from this pin. If R_I is equal to 24kΩ, the magnitude of the constant current is 100μA. An external NTC thermistor must be connected from this pin to ground as shown in Figure 30. When the OTP voltage drops below $V_{OTP-OFF}$ (1.2V), SG6905 is disabled, and does not recover until OTP voltage exceeds V_{OTP-ON} (1.4V).

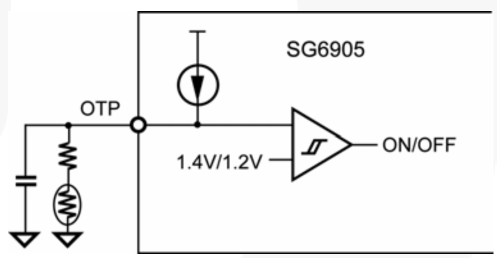

Figure 30. OTP Function

Soft-Start

During startup of the PWM stage, the SS pin charges an external capacitor with a constant current source. The voltage on FBPWM is clamped by SS voltage during startup. In the event of a protected condition occurring and/or PWM being disabled, the SS pin is quickly discharged.

Gate Drivers

The SG6905 output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode in order to protect the external power MOSFET.

Physical Dimensions

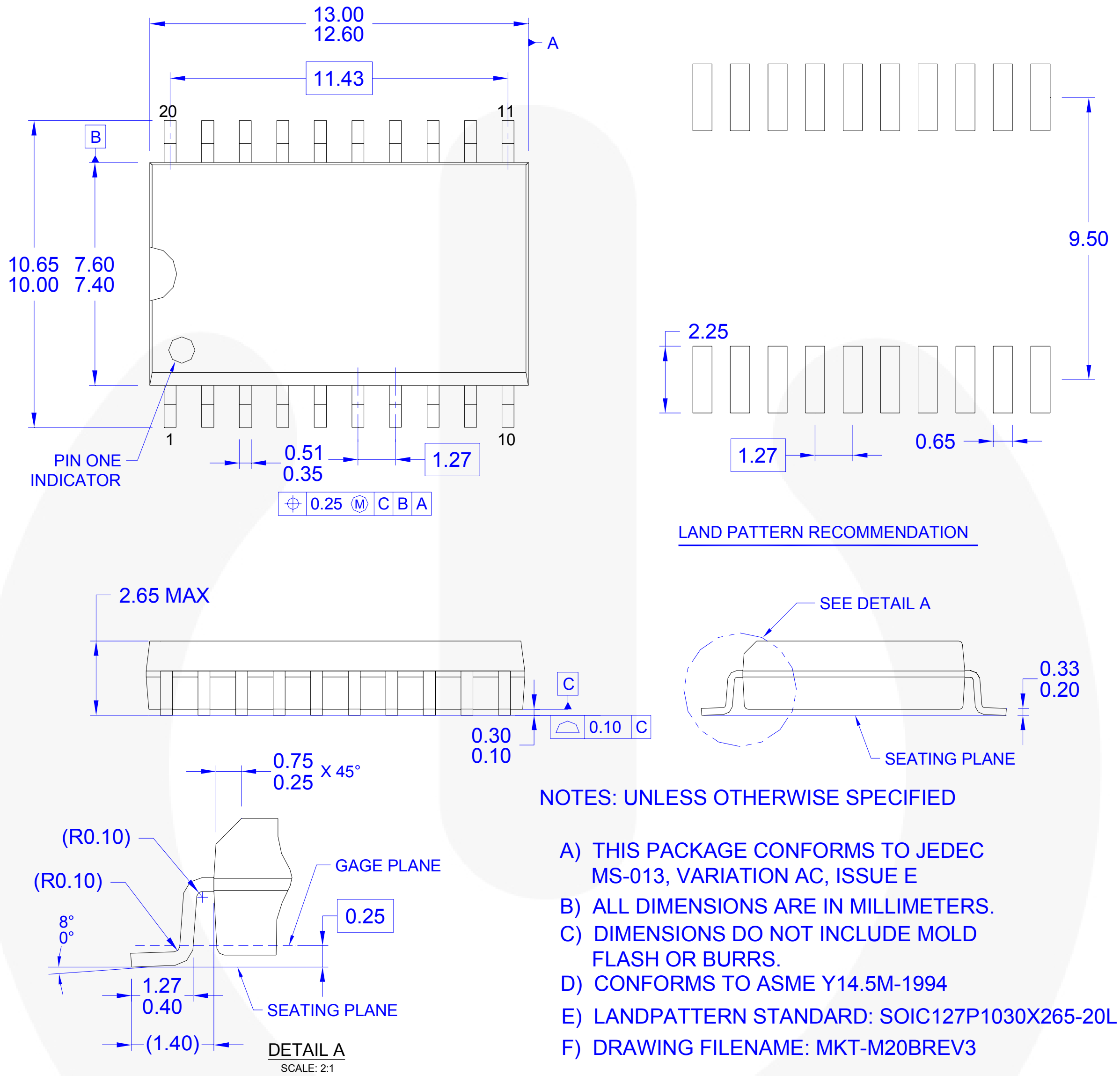

Figure 31. 20-Pin Small Outline Package (SOP)

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