SiI150 / SiI150A
PanelLink® Digital Transmitter

Silicon Image

March 1999

General Description

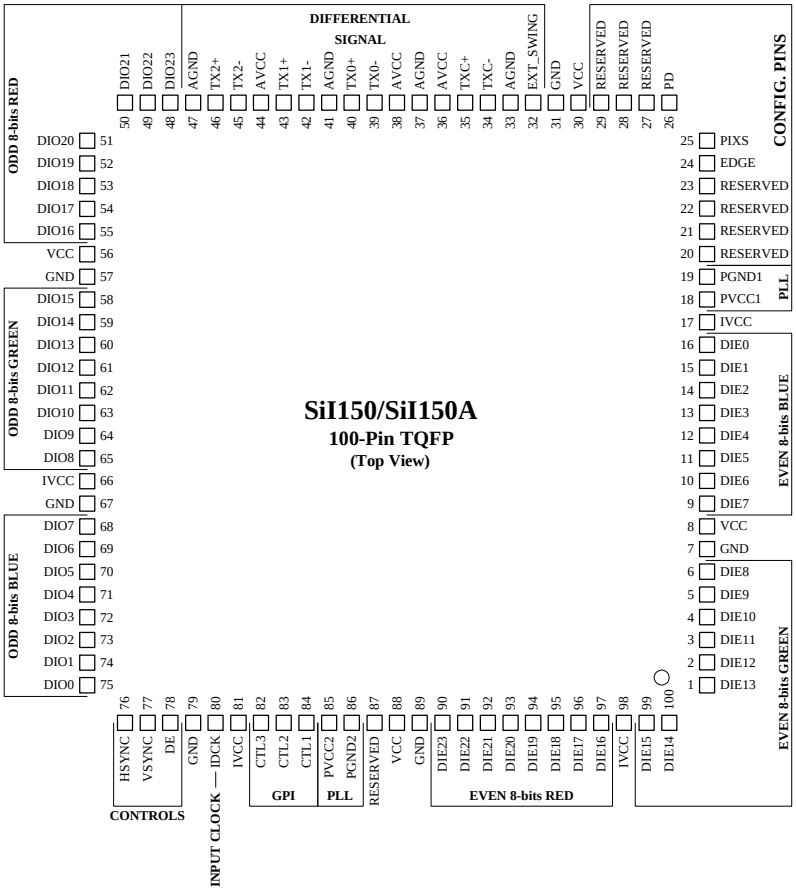
As the universal transmitter, SiI150/SiI150A uses PanelLink Digital technology to support displays ranging from VGA to SXGA (25-112 MHz). The SiI150/SiI150A transmitter supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode, and also features an inter-pair skew tolerance up to 1 full input clock cycle. An advanced on-chip jitter filter is also added to extend tolerance to VGA clock jitter. Since all PanelLink products are designed on scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed digital design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

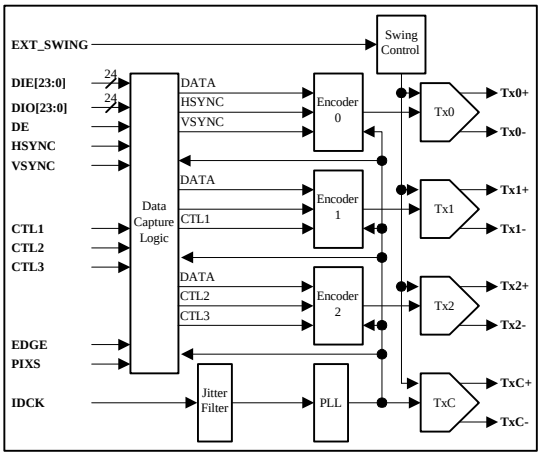
Features

- Scaleable Bandwidth: 25-112 MHz (VGA to SXGA)
- Low Power: 3.3V core operation & power-down mode
- High Skew Tolerance: 1 full input clock cycle (9ns at 108 MHz)
- Flexible panel interface: single or dual pixel in at up to 24-bits
- Sync Detect: for Plug & Display “Hot Plugging”
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

SiI150/SiI150A Pin Diagram



Functional Block Diagram



PanelLink™ DIGITAL

SiI 151
PanelLink® Digital Receiver

July 1999

General Description

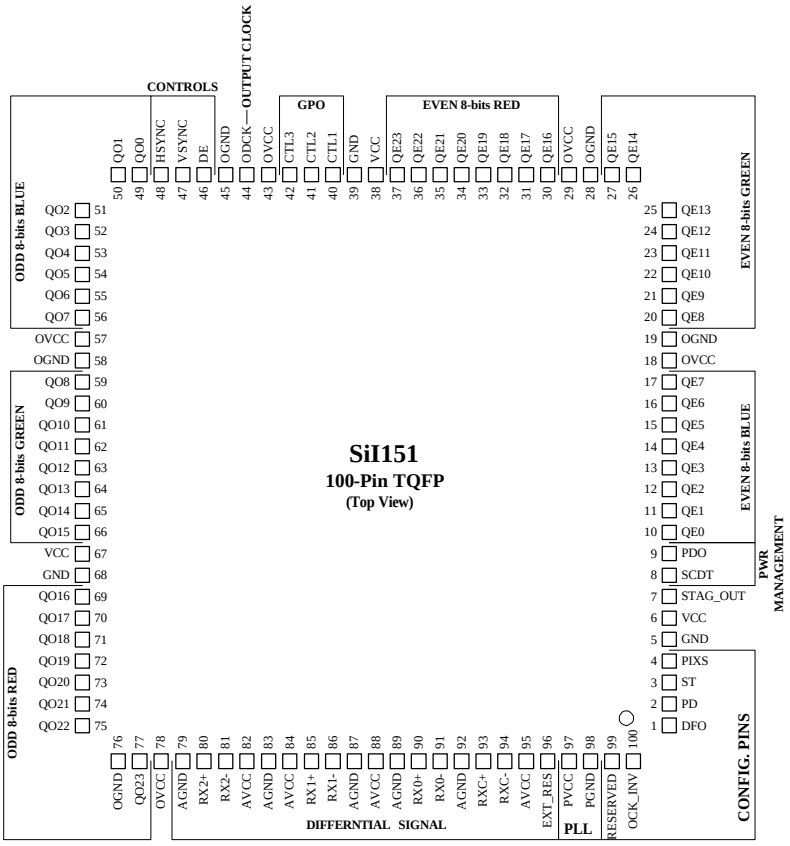
The SiI151 uses PanelLink Digital technology to support displays ranging from VGA to SXGA (25-112 MHz) which is ideal for desktop and specialty applications. The SiI151 receiver supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode, and also features an inter-pair skew tolerance up to 1 full input clock cycle. In addition, the receiver data output is time staggered to reduce ground bounce which affects EMI. Since all PanelLink products are designed on scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed digital design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features

- Scaleable Bandwidth: 25-112 MHz (VGA to SXGA)
- Low Power: 3.3V core operation & power-down mode
- High Skew Tolerance: 1 full input clock cycle (9ns at 108 MHz)
- Time staggered data output for reduced ground bounce
- Sync Detect: for Plug & Display "Hot Plugging"
  Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

SiI151 Pin Diagram



Functional Block Diagram