404-986

GEC PLESSEY
SEMICONDUCTORS

Farnell
COMPONENTS

SL6440
HIGH LEVEL MIXER

The SL6440 is a double balanced mixer intended for use in radio systems up to 150MHz. A special feature of the circuit allows external selection of the DC operating conditions by means of a resistor connected between pin 11 (bias) and Vcc. When biased for a supply current of 50mA the SL6440 offers a 3rd order intermodulation intercept point of typically +30dBm, a value previously unobtainable with integrated circuits. This makes the device suitable for many applications where diode ring mixers had previously been used and offers the advantages of a voltage gain, low local oscillator drive requirement and superior isolation.

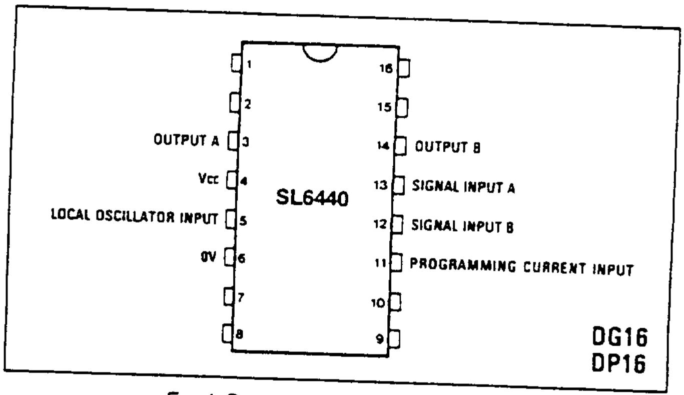

Fig.1 Pin connections - top view

FEATURES

- +30dBm Input Intercept Point
- +15dBm Compression Point (1dB)
- Programmable Performance
- Full Military Temperature Range (SL6440A)

APPLICATIONS

- Mixers in Radio Transceivers
- Phase Comparators
- Modulators

ORDERING INFORMATION

SL6440 A DG
SL6440 C DP

ABSOLUTE MAXIMUM RATINGS

Supply voltage and output pins	15V
Maximum power dissipation	1200mW
(Derate above 25°C 8mW/°C)	
Storage temperature range	-65°C to -150°C
Programming current into pin 11	50mA

THERMAL CHARACTERISTICS

Thermal resistance: θ_{JA}	125°C/W
θ_{JC}	40°C/W
Time constant, Junction-Ambient	1 9 mins
Maximum chip temperature	150°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC1} = 12V, V_{CC2} = 10V, I_P = 25mA, T_{amb} = -55°C to +125°C (SL6440A), -30°C to +85°C (SL6440C)
Local oscillator input level = 0dBm; Test circuit Fig.2.

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
Signal frequency 3dB point	100	150		MHz	
Oscillator frequency 3dB point	100	150		MHz	
3rd order input intercept point		+30		dBm	
Third order intermodulation distortion		-60		dB	Two 0dBm input Signals
Second order intermodulation distortion		-75		dB	
1dB compression point		15		dBm	Vcc1 = 15V Vcc2 = 12V; Vcc1 = 12V Vcc2 = 10V
Noise figure		11		dB	Fig.8 test circuit
Conversion gain		-1		dB	50Ω load Fig 2
Carrier leak to signal input	-40			dB	Test circuit Fig 8
Level of carrier at IF output		-25		dBm	See applications information
Supply current		7		mA	I_P = 0
Supply current (total from Vcc1 & Vcc2)		60		mA	
Local oscillator input	100	250	500	mV rms	I_P = 35mA
Local oscillator input impedance		1 5		kΩ	
Signal input impedance		500		Ω	Single ended
		1000		Ω	Differential

NOTE Supply current in Pin 3 is equal to that in Pin 14 and is equal to I. See over V 11 3V. 2 1V

CIRCUIT DESCRIPTION

The SL6440 is a high level mixer designed to have a linear RF performance. The linearity can be programmed using the I_p pin (11).

The output pins are open collector outputs so that the conversion gain and output loads can be chosen for the specific application.

Since the outputs are open collectors they should be returned to a supply Vcc1 through a load.

The choice of Vcc1 is important since it must be ensured that the voltage on pins 3 and 14 is not low enough to saturate the output transistors and so limit the signal swing unnecessarily. If the voltage on pins 3 and 14 is always greater than Vcc2 the outputs will not saturate. The output frequency response will reduce as the output transistors near saturation.

Minimum Vcc1 = (I_p x RL) + Vs + Vcc2
where I_p = programmed current
RL = DC load resistance
Vs = max signal swing at output
if the signal swing is not known:
minimum Vcc1 = 2 (I_p x RL) + Vcc2

In this case the signal will be limiting at the input before the output saturates.

The device has a separate supply (Vcc2) for the oscillator buffer (pin 4)

The current (I_p) programmed into pin 11 can be supplied via a resistor from Vcc1 or from a current source

The conversion gain is equal to

$$GdB = 20 \text{ Log } \frac{RL\ I_p}{56\ 61\ I_p - 0\ 0785} \text{ for single-ended output}$$

$$GdB = 20 \text{ Log } \frac{2\ RL\ I_p}{56\ 61\ I_p - 0\ 0785} \text{ for differential output}$$

Device dissipation is calculated using the formula

mW diss = 2 I_p Vo + V_p I_p - Vcc2 Diss
where Vo = voltage on pin 3 or pin 14
V_p = voltage on pin 11
I_p = programming current (mA)
Vcc2 Diss = dissipation obtained from graph (Fig 6)

As an example Fig. 7 shows typical dissipations assuming Vcc1 and Vo are equal. This may not be the case in practice and the device dissipation will have to be calculated for any particular application.

Fig 5 shows the intermodulation performance against I_p. The curves are independent of Vcc1 and Vcc2 but if Vcc1 becomes too low the output signal swing cannot be accommodated, and if Vcc2 becomes too low the circuit will not provide enough drive to sink the programmed current Examples are shown of performance at various supply voltages

The current in pin 14 is equal to the current in pin 3 which is equal to the current in pin 11

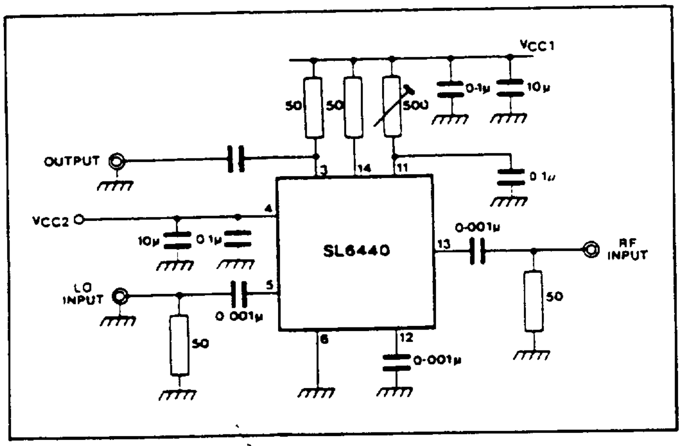

Fig.2 Typical application and test circuit

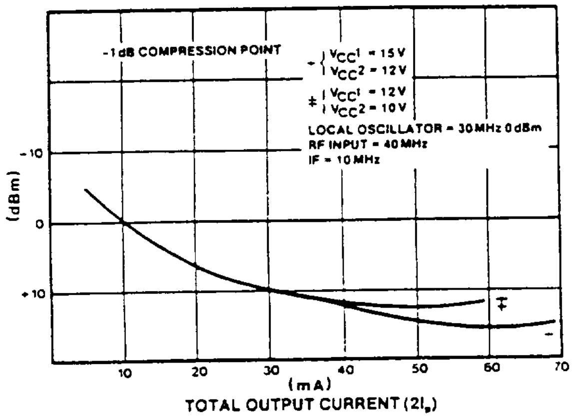

Fig 3 Compression point v total output current

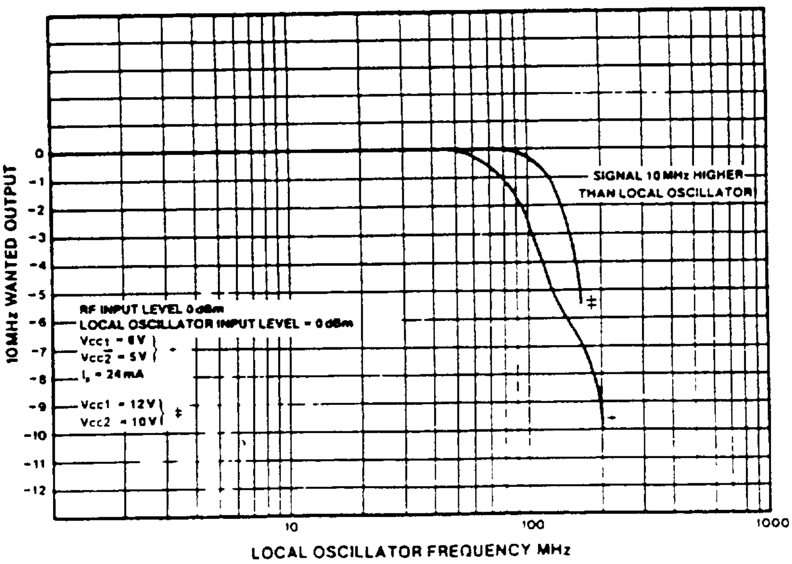

Fig 4 Frequency response at constant output IF

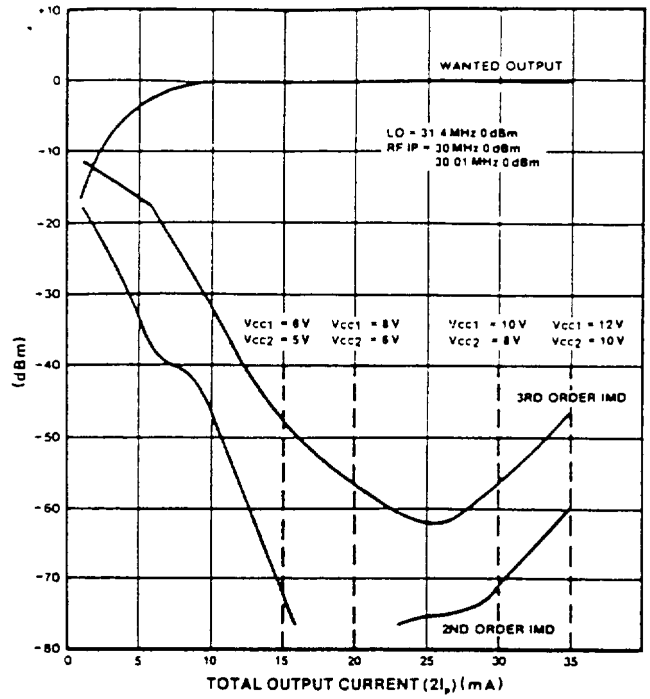

Fig 5 Intermodulation v programming current

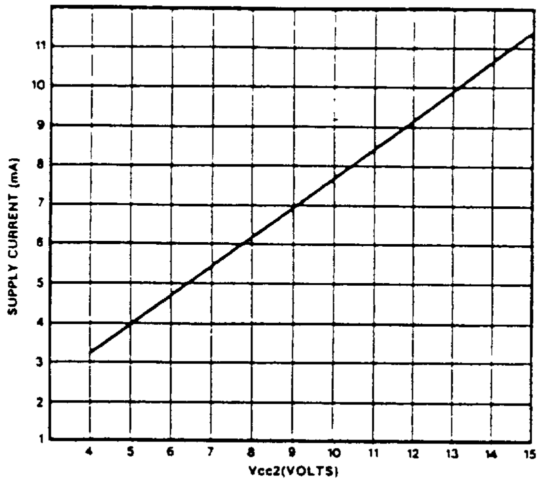

Fig.6 Supply current v Vcc2 (I_P = 0)

APPLICATIONS

The SL6440 can be used with differential or single-ended inputs and outputs. A balanced input will give better carrier leak. The high input impedance allows step-up transformers to be used if desired, whilst high output impedance allows a choice of output impedance and conversion gain.

Fig 2 shows the simplest application circuit. The input and output are single-ended and I_P is supplied from Vcc1 via a resistor. Increasing RL will increase the conversion gain, care being taken to choose a suitable value for Vcc1.

Fig 8 shows an application with balanced input, for improved carrier leak, and balanced output for increased conversion gain. A lower Vcc1 giving lower device dissipation can be used with this arrangement.

DESIGN PROCEDURE

1. Decide on input configuration using local oscillator data. If using transformer on input, decide on ratio from noise considerations.
2. Decide on output configuration and value of conversion gain required.
3. Decide on value of I_P and Vcc2 using intermodulation and compression point graphs.
4. Using values of conversion gain, Vcc2, load and I_P already chosen, decide on value of Vcc1.
5. Calculate device dissipation and decide whether heatsink is required from maximum operating temperature considerations.

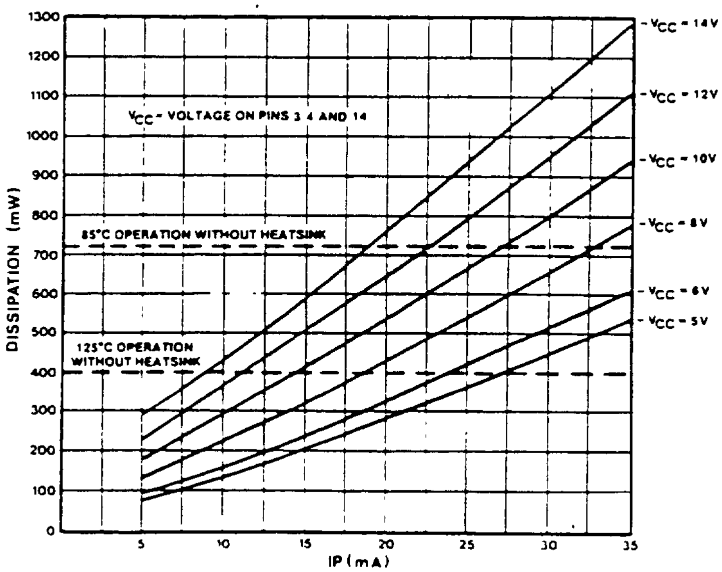

Fig 7 Device dissipation v I_P

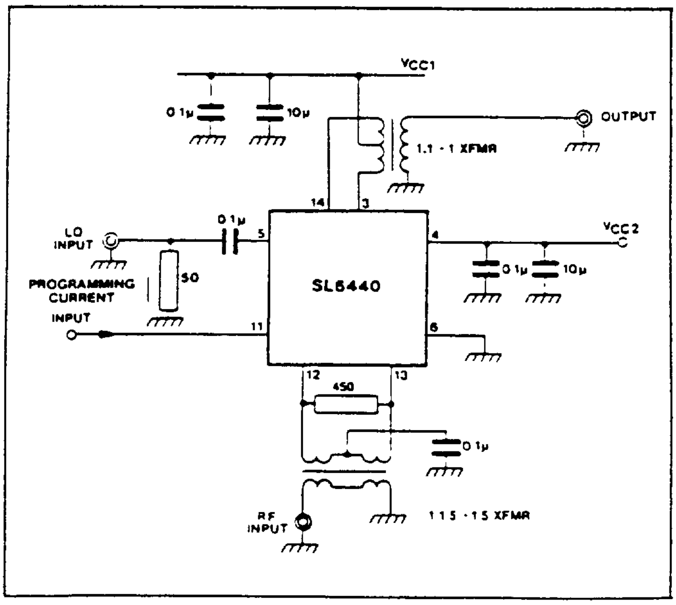

Fig 8 Typical application circuit for highest performance