

OVERVIEW

The SM5841C is a digital filter for digital audio, fabricated in Molybdenum-gate CMOS. The SM5841C features 8-times oversampling, digital deemphasis, soft muting and a noise shaper. It can operate from a standard 5V supply or a low-voltage 3.2V supply. The SM5841C is available in 22-pin SOPs.

FEATURES

- Filter configuration
 - 2-channel, 8-times oversampling (interpolation) filter
 - 3-stage interpolation (69-tap + 13-tap + 9-tap)
 - 44.1kHz IIR deemphasis filter for accurate gain and phase response
 - Overflow limiter
 - Crystal oscillation circuit built-in
- Filter characteristics (fs = sampling frequency)
 - 0.20 ± 0.03dB passband (0 to 0.4535fs) ripple
 - 53dB (min) stopband attenuation (0.5465fs to 7.4535fs)
 - Linear phase (zero group delay)
- Input/output
 - 16-bit serial data input (2s-complement, MSB-first)
 - 16-, 18- or 20-bit serial data output (2s-complement, MSB-first)
 - TTL-compatible
- 384fs system clock
- Supply voltage
 - 5V normal-voltage operation
 - 3.2V low-voltage operation
- Package: 22-pin SOP
- Molybdenum-gate CMOS process
- Filter functions
 - 1st-order noise shaper (ON/OFF selectable for 18-bit output)
 - Soft muting
 - Digital deemphasis (for 44.1kHz)

APPLICATIONS

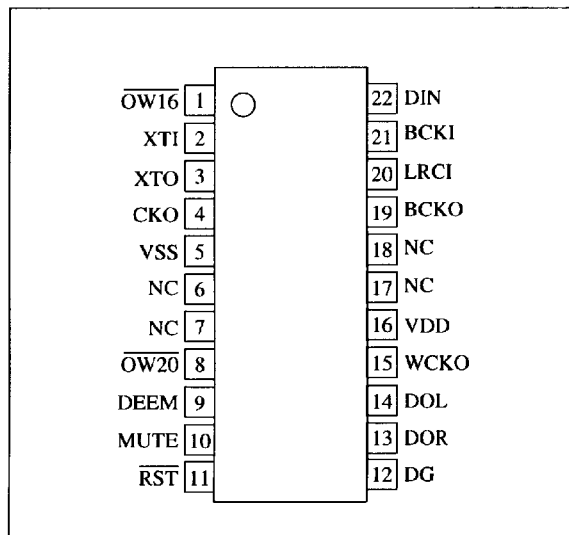
- CD playback systems
- PCM playback systems

ORDERING INFORMATION

Device	Package
SM5841CS	22-pin SOP

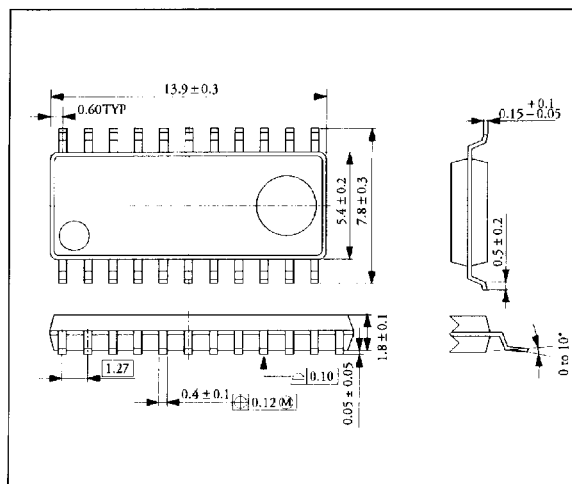
PINOUT

(Top view)

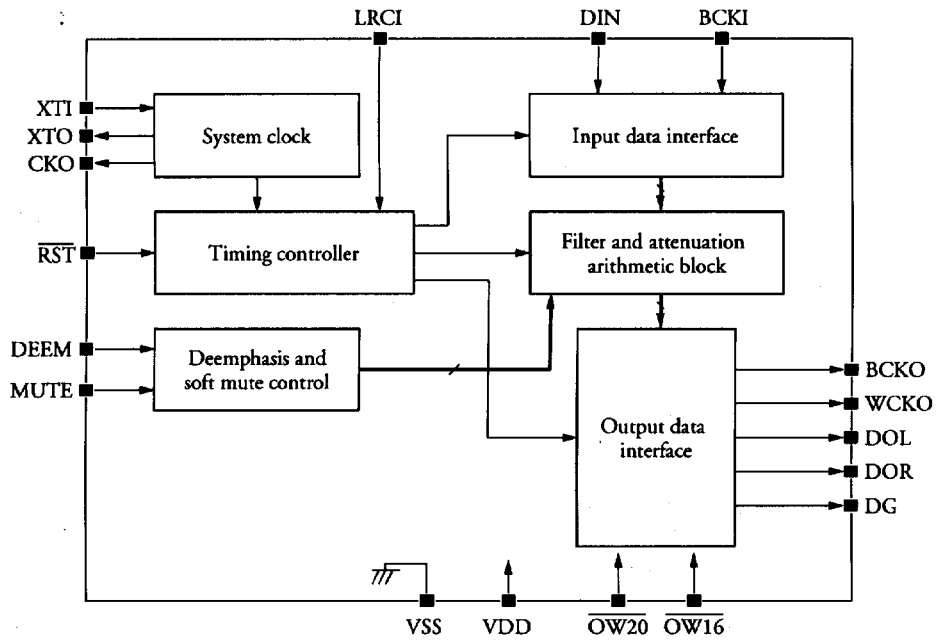


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	IO ¹	Description		
1	OW16	Ip	Output word length select 1		
			OW16	OW20	Output word length (Noise shaper ON/OFF)
			LOW	LOW	18 bits (OFF)
			LOW	HIGH	16 bits (ON)
			HIGH	LOW	20 bits (ON)
HIGH	HIGH	18 bits (ON)			
2	XTI	I	Oscillator input connection		
3	XTO	O	Oscillator output connection		
4	CKO	O	Oscillator output clock (same frequency as XTI)		
5	VSS	-	Ground		
6	NC	-	No connection		
7	NC	-	No connection		
8	OW20	Ip	Output word length select 2		
			OW16	OW20	Output word length (Noise shaper ON/OFF)
			LOW	LOW	18 bits (OFF)
			LOW	HIGH	16 bits (ON)
			HIGH	LOW	20 bits (ON)
HIGH	HIGH	18 bits (ON)			
9	DEEM	Ip	Deemphasis signal input. Deemphasis is OFF when LOW, and ON when HIGH.		
10	MUTE	Ip	Mute signal input. Soft muting is OFF when LOW, and ON when HIGH.		
11	RST	Ip	System reset		
12	DG	O	De-glitched output		
13	DOR	O	Right-channel data output		
14	DOL	O	Left-channel data output		
15	WCKO	O	Output word clock		
16	VDD	-	5 V supply		
17	NC	-	No connection		
18	NC	-	No connection		
19	BCKO	O	Output bit clock		
20	LRCI	Ip	Input data sample rate (fs) clock		
21	BCKI	Ip	Input bit clock		
22	DIN	Ip	Data input		

1. I = input, Ip = Input with pull-up resistor, O = output

SPECIFICATIONS

Absolute Maximum Ratings

 $V_{SS} = 0 \text{ V}$

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to 7.0	V
Input voltage range	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Power dissipation	P_D	250	mW
Storage temperature range	T_{stg}	-40 to 125	deg. C
Soldering temperature	T_{sld}	255	deg. C
Soldering time	t_{sid}	10	s

Recommended Operating Conditions

 $V_{SS} = 0 \text{ V}$

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	3.2 to 5.5	V
Operating temperature range	T_{opr}	-20 to 80	deg. C

DC Electrical Characteristics

Normal-voltage mode

 $V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = -20 \text{ to } 80 \text{ deg. C}$ unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	$V_{DD} = 5.0 \text{ V}$, $f_{sys} = 384fs = 19.3 \text{ MHz}$, no load	-	-	40	mA
XTI HIGH-level input voltage	V_{IH1}		$0.7V_{DD}$	-	-	V
XTI LOW-level input voltage	V_{IL1}		-	-	$0.3V_{DD}$	V
HIGH-level input voltage	V_{IH2}	See note 1.	2.4	-	-	V
LOW-level input voltage	V_{IL2}		-	-	0.5	V
HIGH-level output voltage	V_{OH}	$I_{OH} = -0.4 \text{ mA}$. See note 2.	2.5	-	-	V
LOW-level output voltage	V_{OL}	$I_{OL} = 1.6 \text{ mA}$. See note 2.	-	-	0.4	V
XTI HIGH-level input leakage current	I_{LH1}	$V_{IN} = V_{DD}$	-	10	20	μA
XTI LOW-level input leakage current	I_{LL1}	$V_{IN} = 0 \text{ V}$	-	10	20	μA
HIGH-level input leakage current	I_{LH2}	$V_{IN} = V_{DD}$. See note 1.	-	-	1.0	μA
LOW-level input current	I_{IL}	$V_{IN} = 0 \text{ V}$. See note 1.	-	10	20	μA

Notes

1. Pins LRCI, DIN, BCKI, MUTE, DEEM, $\overline{OW16}$, $\overline{OW20}$ and \overline{RST}
2. Pins CKO, DOL, DOR, BCKO, WCKO and DG

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Low-voltage mode

$V_{DD} = 3.2$ to 4.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 70 deg. C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	$V_{DD} = 3.4$ V, $f_{sys} = 384fs = 18.5$ MHz, no load	-	-	20	mA
XTI HIGH-level input voltage	V_{IH1}		$0.7V_{DD}$	-	-	V
XTI LOW-level input voltage	V_{IL1}		-	-	$0.3V_{DD}$	V
HIGH-level input voltage	V_{IH2}	See note 1.	2.4	-	-	V
LOW-level input voltage	V_{IL2}		-	-	0.5	V
HIGH-level output voltage	V_{OH}	$I_{OH} = -0.2$ mA. See note 2.	2.5	-	-	V
LOW-level output voltage	V_{OL}	$I_{OL} = 0.8$ mA. See note 2.	-	-	0.4	V
XTI HIGH-level input leakage current	I_{LH1}	$V_{IN} = V_{DD}$	-	-	12	μ A
XTI LOW-level input leakage current	I_{LL1}	$V_{IN} = 0$ V	-	-	12	μ A
HIGH-level input leakage current	I_{LH2}	$V_{IN} = V_{DD}$. See note 1.	-	-	1.0	μ A
LOW-level input current	I_{IL}	$V_{IN} = 0$ V. See note 1.	-	-	12	μ A

Notes

1. Pins LRCI, DIN, BCKI, MUTE, DEEM, $\overline{OW16}$, $\overline{OW20}$ and \overline{RST}
2. Pins CKO, DOL, DOR, BCKO, WCKO and DG

AC Electrical Characteristics

$V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 80 deg. C for normal-voltage operation.

$V_{DD} = 3.2$ to 4.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 70 deg. C for low-voltage operation.

Typical values are measured at $f_s = 44.1$ kHz.

System clock

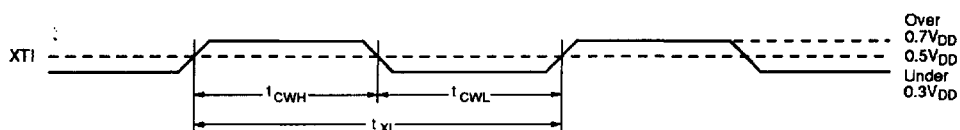
Crystal oscillator operation

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{MAX}	4.0	16.9	19.3	MHz

External clock input operation

Parameter	Symbol	Rating			Unit
		min	typ	max	
XTI HIGH-level clock pulsewidth	t_{CWH}	21.7	29.5	125	ns
XTI LOW-level clock pulsewidth	t_{CWL}	21.7	29.5	125	ns
XTI clock pulse time	t_{XI}	51.7	59.0	250	ns

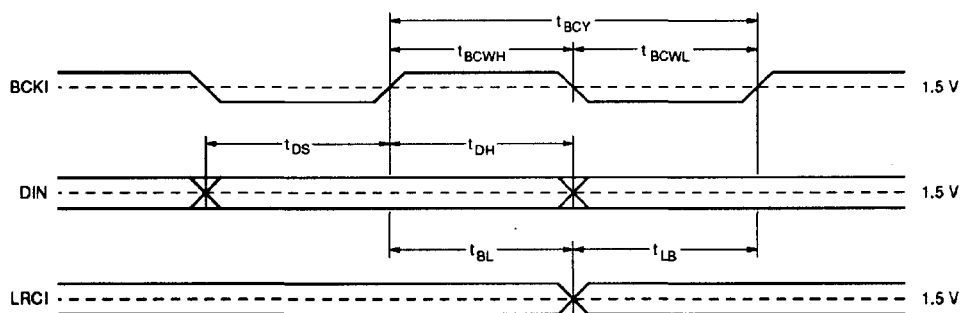
System clock timing waveform



Serial input timing (BCKI, DIN, LRCI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	-	-	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	-	-	ns
BCKI pulse period	t_{BCY}	100	-	-	ns
DIN setup time	t_{DS}	50	-	-	ns
DIN hold time	t_{DH}	50	-	-	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	-	-	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	-	-	ns

BCKI, DIN and LRCI Input timing waveform



Reset timing

$V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 80 deg. C

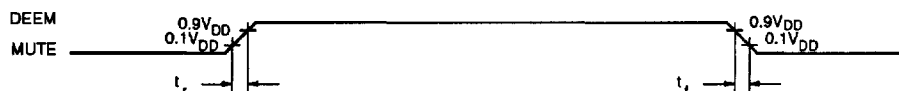
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RST LOW-level pulsewidth	t_{RST}	At power-on	1	-	-	μ s
		At other times	50	-	-	ns

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Control input timing (DEEM, MUTE)

Parameter	Symbol	Rating			Unit
		min	typ	max	
DEEM and MUTE rise time	t_r	–	–	100	ns
DEEM and MUTE fall time	t_f	–	–	100	ns

Control input timing waveform



Output timing

Normal-voltage mode

$V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator input to output delay	t_{XTO}	XTI falling edge to XTO rising edge	3	–	20	ns
Oscillator input to clock output delay	t_{CKO}	XTI falling edge to CKO falling edge	7	–	30	ns
Oscillator input to bit clock output delay (CKSL = HIGH)	t_{bH}	XTI falling edge to BCKO rising edge	10	–	60	ns
	t_{bL}	XTI falling edge to BCKO falling edge	10	–	60	ns
Oscillator input to bit clock output delay (CKSL = LOW)	t_{bH}	XTI rising edge to BCKO rising edge	10	–	60	ns
	t_{bL}	XTI falling edge to BCKO falling edge	10	–	60	ns
Bit clock output to data output and word clock output delay	t_{bdH1}	BCKO falling edge to rising-edge output	0	–	20	ns
	t_{bdL1}	BCKO falling edge to falling-edge output	0	–	20	ns
Bit clock output to de-glitched output delay	t_{bdH2}	BCKO rising edge to rising-edge output	0	–	20	ns
	t_{bdL2}	BCKO rising edge to falling-edge output	0	–	20	ns

Note

All measurements with 15 pF load

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Low-voltage mode

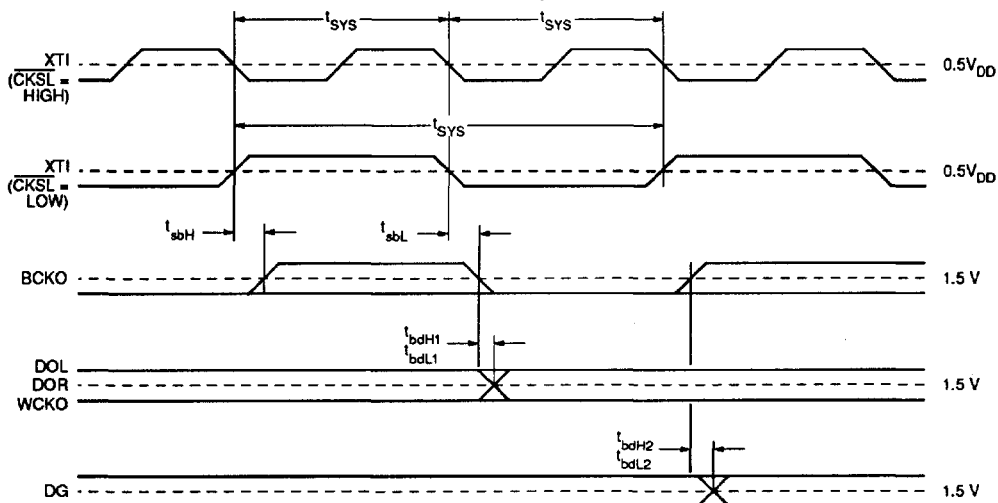
$V_{DD} = 3.2$ to 4.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator input to output delay	t_{XTO}	XTI falling edge to XTO rising edge	3	-	30	ns
Oscillator input to clock output delay	t_{CKO}	XTI falling edge to CKO falling edge	7	-	45	ns
Oscillator input to bit clock output delay (CKSL = HIGH)	t_{sbH}	XTI falling edge to BCKO rising edge	10	-	100	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	-	100	ns
Oscillator input to bit clock output delay (CKSL = LOW)	t_{sbH}	XTI rising edge to BCKO rising edge	10	-	100	ns
	t_{sbL}	XTI falling edge to BCKO falling edge	10	-	100	ns
Bit clock output to data output and word clock output delay	t_{bdH1}	BCKO falling edge to rising-edge output	0	-	30	ns
	t_{bdL1}	BCKO falling edge to falling-edge output	0	-	30	ns
Bit clock output to de-glitched output delay	t_{bdH2}	BCKO rising edge to rising-edge output	0	-	30	ns
	t_{bdL2}	BCKO rising edge to falling-edge output	0	-	30	ns

Note

All measurements with 15 pF load

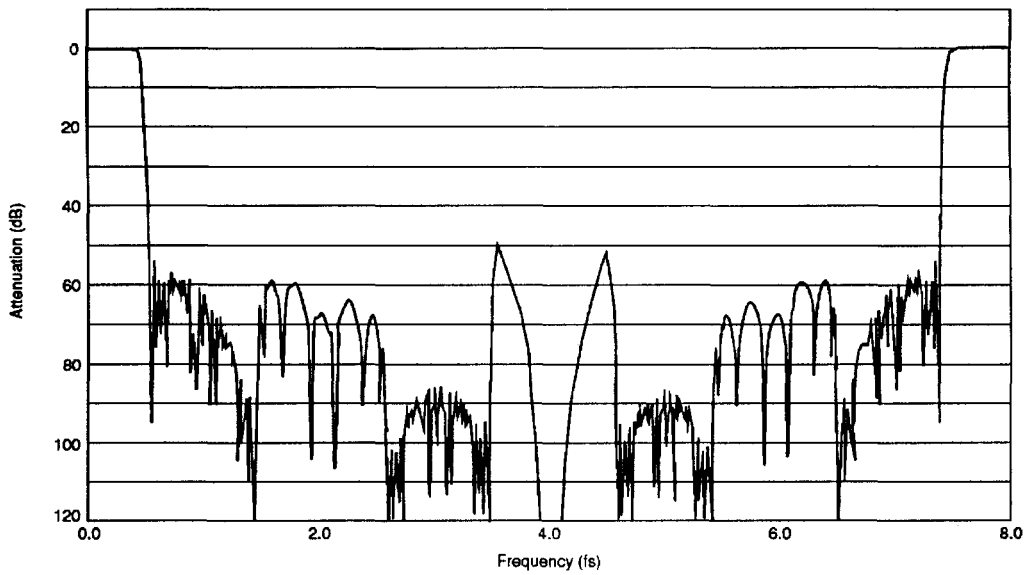
Output timing waveform



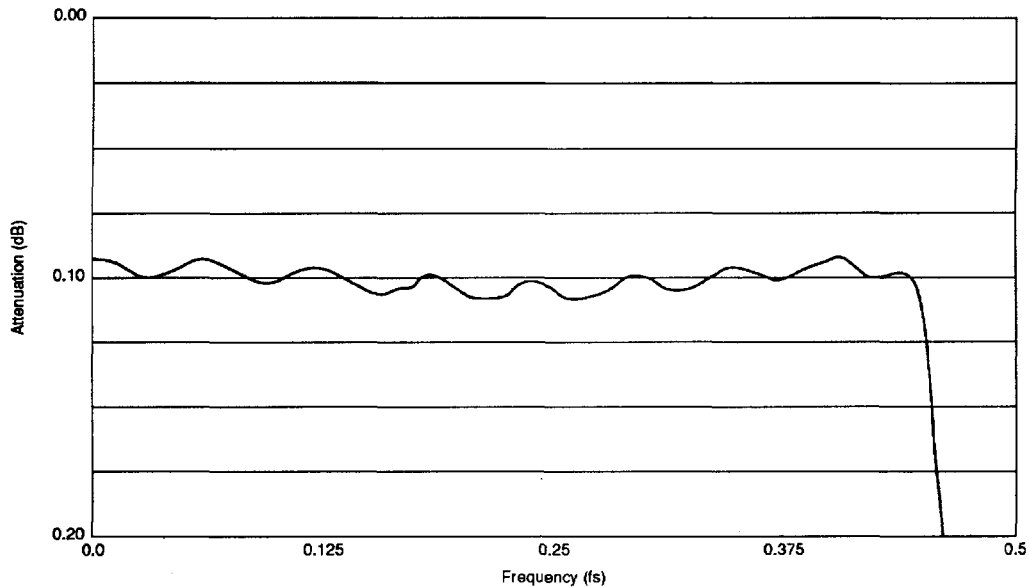
Filter Characteristics

Parameter	Frequency		Rating (dB)		
	f	@fs = 44.1 kHz	min	typ	max
Passband attenuation	0 to 0.4535fs	0 to 20 kHz	-	0.20	-
Passband ripple			-0.03	-	0.03
Stopband attenuation	0.5465fs to 3.4535fs	21.4 to 152 kHz	53	-	-
	3.4535fs to 4.5465fs	152 to 201 kHz	50	-	-
	4.5465fs to 7.4535fs	201 to 328 kHz	53	-	-

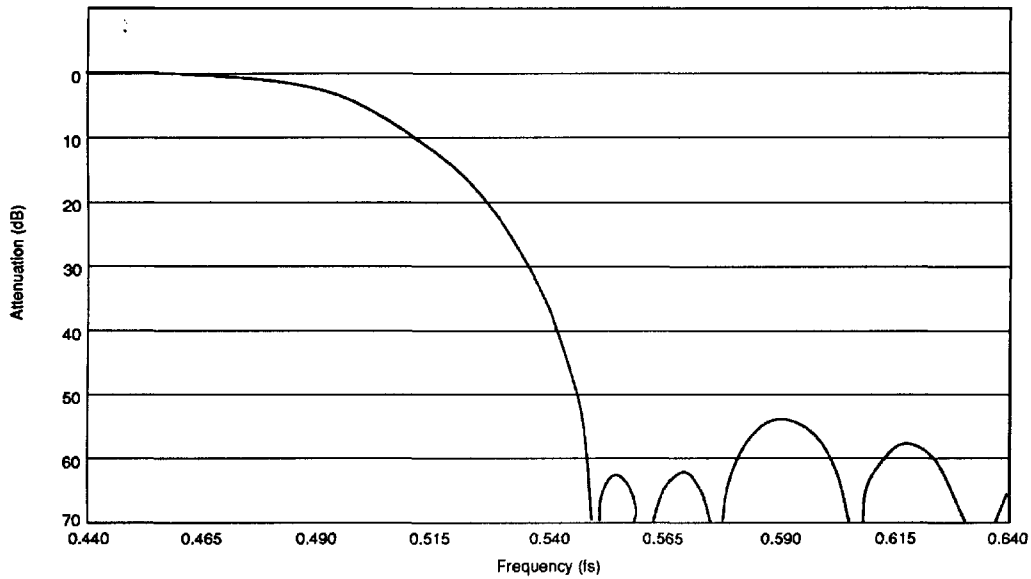
8fs filter frequency characteristic (Deemphasis OFF)



8fs filter passband characteristic (Deemphasis OFF)



8fs filter band-transition characteristic (Deemphasis OFF)



Deemphasis filter

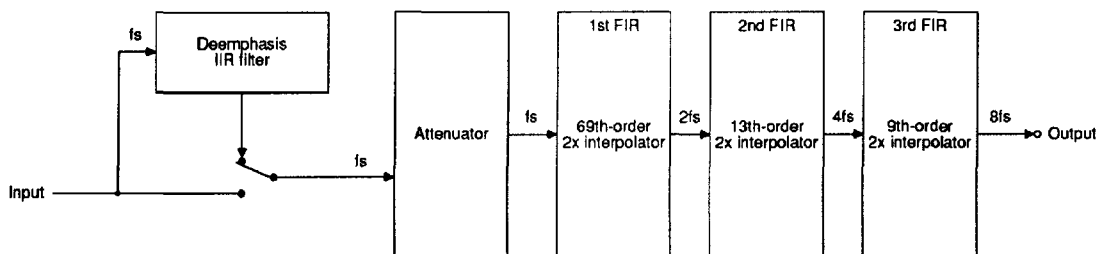
Parameter		Rating at fs = 44.1 kHz
Passband bandwidth (kHz)		0 to 20.0
Deviation from ideal characteristics	Attenuation (dB)	-0.05 to 0.15
	Phase, θ ($^\circ$)	-1 to 1.5

Note

These are the maximum deviations from a 1 kHz input signal with 0 dB attenuation and 0° phase ideal characteristic.

FUNCTIONAL DESCRIPTION

SM5841C Arithmetic Block



Oversampling (Interpolation)

The SM5841C performs oversampling using a three-stage FIR interpolation filter. Each filter stage interpolates the signal by a factor of two, giving an overall interpolation factor of eight. Sampling noise components are attenuated by the interpolation filter to greater than 53 dB in the 0.5465fs to 7.4535fs stopband.

Digital Deemphasis

The deemphasis filter is in cascade with the oversampling filters. It is implemented using an IIR filter, and reproduces the deemphasis gain and phase characteristics more faithfully than conventional analog deemphasis filters. Deemphasis is enabled when DEEM is HIGH, and disabled when DEEM is LOW.

Soft Mute

The oversampled output can be muted using a built-in digital attenuator controlled by the MUTE pin. Muting is ON when MUTE is HIGH, and OFF when MUTE is LOW.

When MUTE is HIGH, the maximum attenuation coefficient (DATT) 127 is loaded into the temporary-storage register and the attenuation slowly changes to ∞ dB in unit steps.

When MUTE is LOW, the maximum attenuation coefficient (DATT) 0 is loaded into the temporary-storage register and the attenuation slowly changes to 0 dB in unit steps.

Both the left and right channels are attenuated simultaneously by an amount

$$\text{Attenuation} = 20 \times \log_{10} (1 - \text{DATT}/127) \text{ dB}$$

where DATT is the contents of the attenuation register. When DATT = 127, the attenuation is infinite (mute function).

If MUTE changes level before the maximum/minimum level is reached, the gain ramps in the direction of the latest set level.

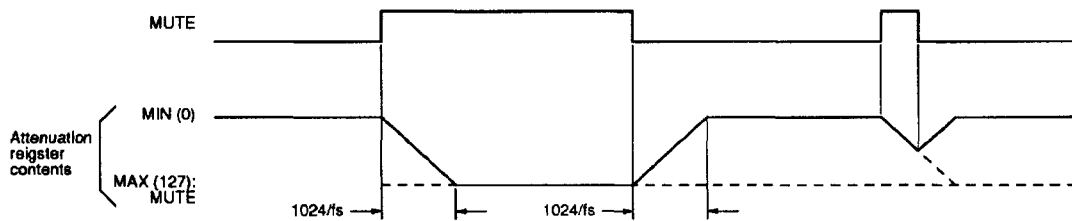


Figure 1. Attenuation level changes

The time taken to increase the attenuation from 0 (DATT = 1) to ∞ dB (DATT = 127) is approximately 1024/fs, which is approximately 23.2 ms at $f_s = 44.1$ kHz.

Audio Data Input (DIN, BCKI, LRCI)

The input is in 16-bit, 2s-complement, MSB-first, serial data format.

System Clock (XTI, XTO, CKO)

The system clock operates at 384fs. The clock can be generated either externally (input on XTI) or internally (crystal oscillator between XTI and XTO). The clock is output on CKO.

Table 1. System clock

System clock frequency	Clock input	Internal operating frequency	Serial output clock frequency
384fs	External clock on XTI OR Crystal oscillator between XTI and XTO	128fs	192fs

Input timing

Serial input data on DIN is clocked into an SIPO register on the rising edge of the BCKI bit clock, and then converted into parallel data.

The SIPO output data for each channel is latched into the left-channel/right-channel input register on the rising/falling edge of LRCI.

The timing of the arithmetic and output circuits is independent of the input timing. Accordingly, phase differences between LRCI, BCKI and XTI do not cause incorrect operation, and data input clock jitter does not generate jitter in the output clock.

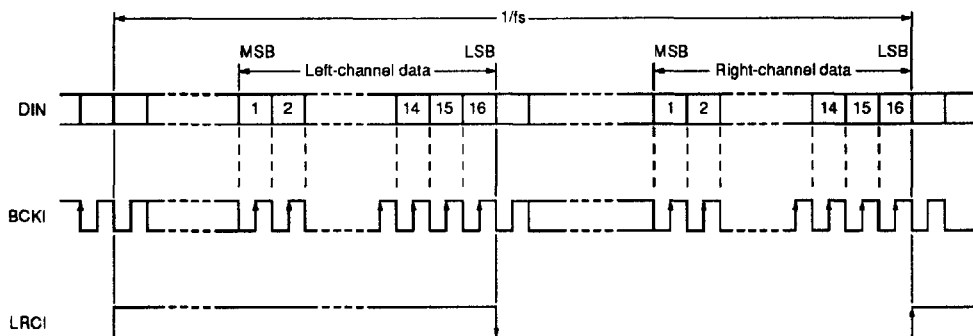


Figure 2. Audio data input timing

Data Output (DOL, DOR, BCKO, WCKO, DG, $\overline{OW16}$, $\overline{OW20}$)

The output is in 8fs L/R alternating, 2s-complement, MSB-first serial format. The output word length is 16-, 18- or 20-bit selectable using $\overline{OW16}$ and $\overline{OW20}$.

The output timing is shown in table 2.

Table 2. Output timing

Parameter	Symbol	Rating
Bit clock rate	t_B	1/192fs
Data word length	t_{DW}	24 t_B

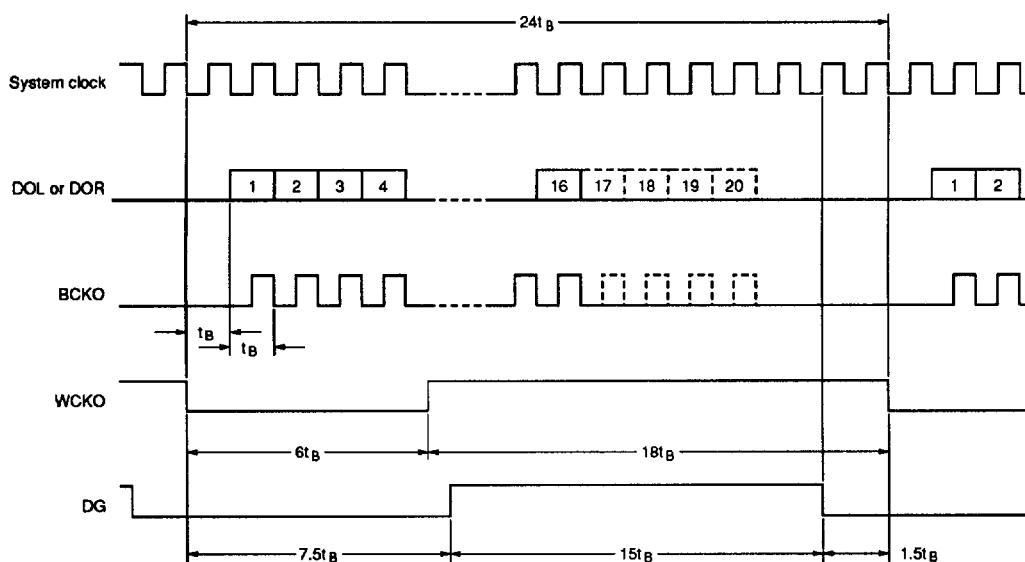


Figure 3. Data output timing

Note

In 18-bit mode, pulses 17 and 18 are output, and in 20-bit mode, pulses 17 to 20 are output.

System Reset

The SM5841C must be reset at power-ON and when \overline{CKSL} changes state by applying at LOW-level pulse on \overline{RST} .

At system reset, the arithmetic and output timing counters are reset on the next LRCI start edge after XTI has stabilized.

A power-ON reset pulse can be applied from a controlling microprocessor, or by connecting a 300 pF capacitor between \overline{RST} and VSS for systems where XTI and LRCI stabilize simultaneously. For

others systems that do not use a microcontroller, XTI and LRCI must stabilize before \overline{RST} goes HIGH. A larger capacitor can be used to ensure that this occurs.

If the system clock becomes corrupted or develops jitter such that the timing increases above $\pm 3/8 \times$ (LRCI clock frequency), then the internal timing will automatically reset on the next LRCI start edge. This timing re-synchronization can generate an output click noise.

Output Muting

When \overline{RST} goes LOW, DOL and DOR go LOW, immediately muting the output words. Muting is released and timing re-synchronized on the third

LRCI rising edge after \overline{RST} goes HIGH. The BCKO and WCKO clock outputs do not stop.

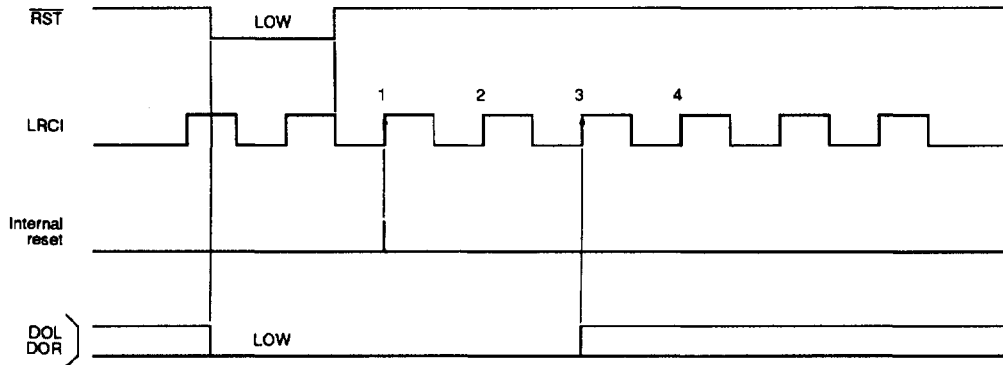


Figure 4. System reset timing and output muting

TIMING DIAGRAMS

Input Timing (DIN, BCKI, LRCI)

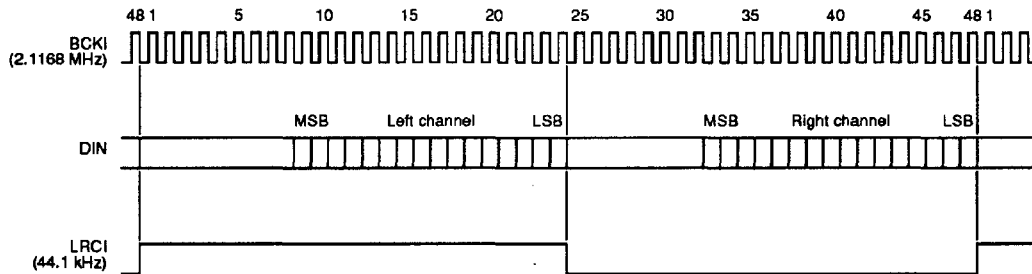


Figure 5. Input timing 1

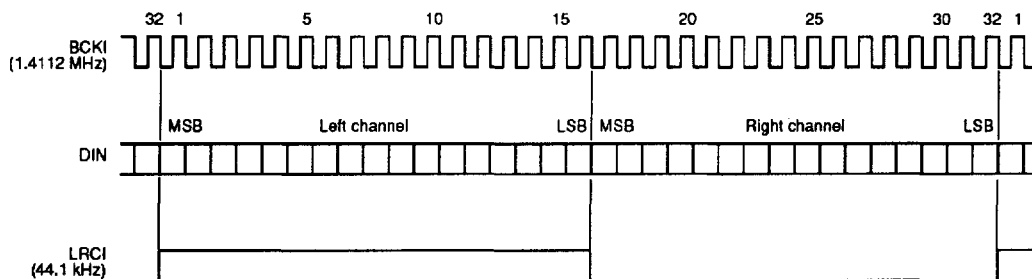


Figure 6. Input timing 2

Output Timing (DOL, DOR, BCKO, WCKO, DG)

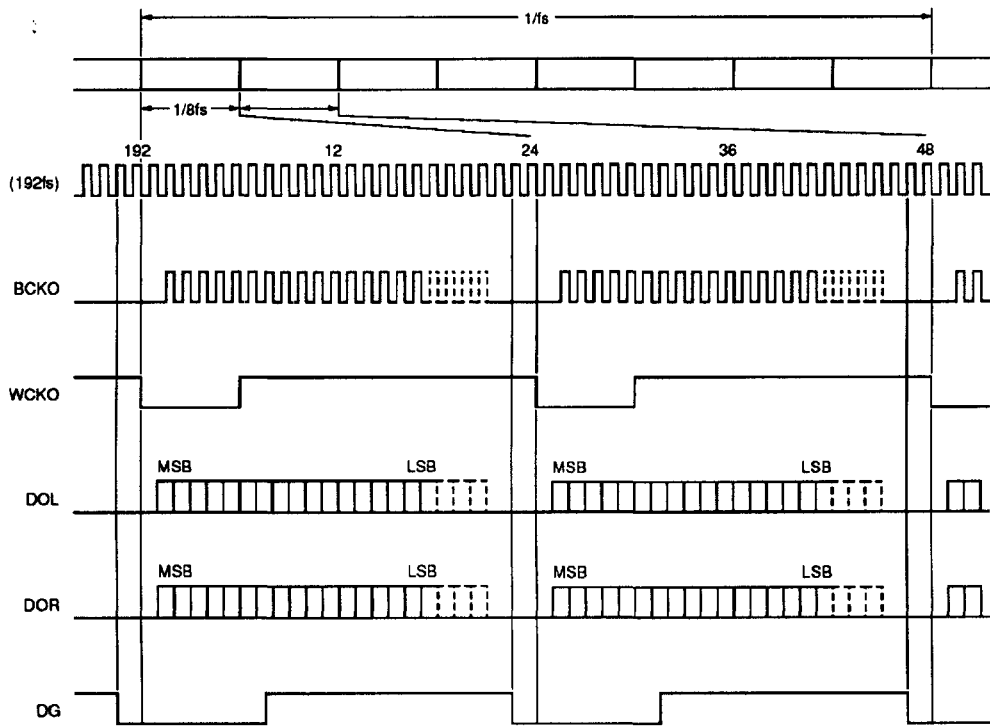


Figure 7. Output timing

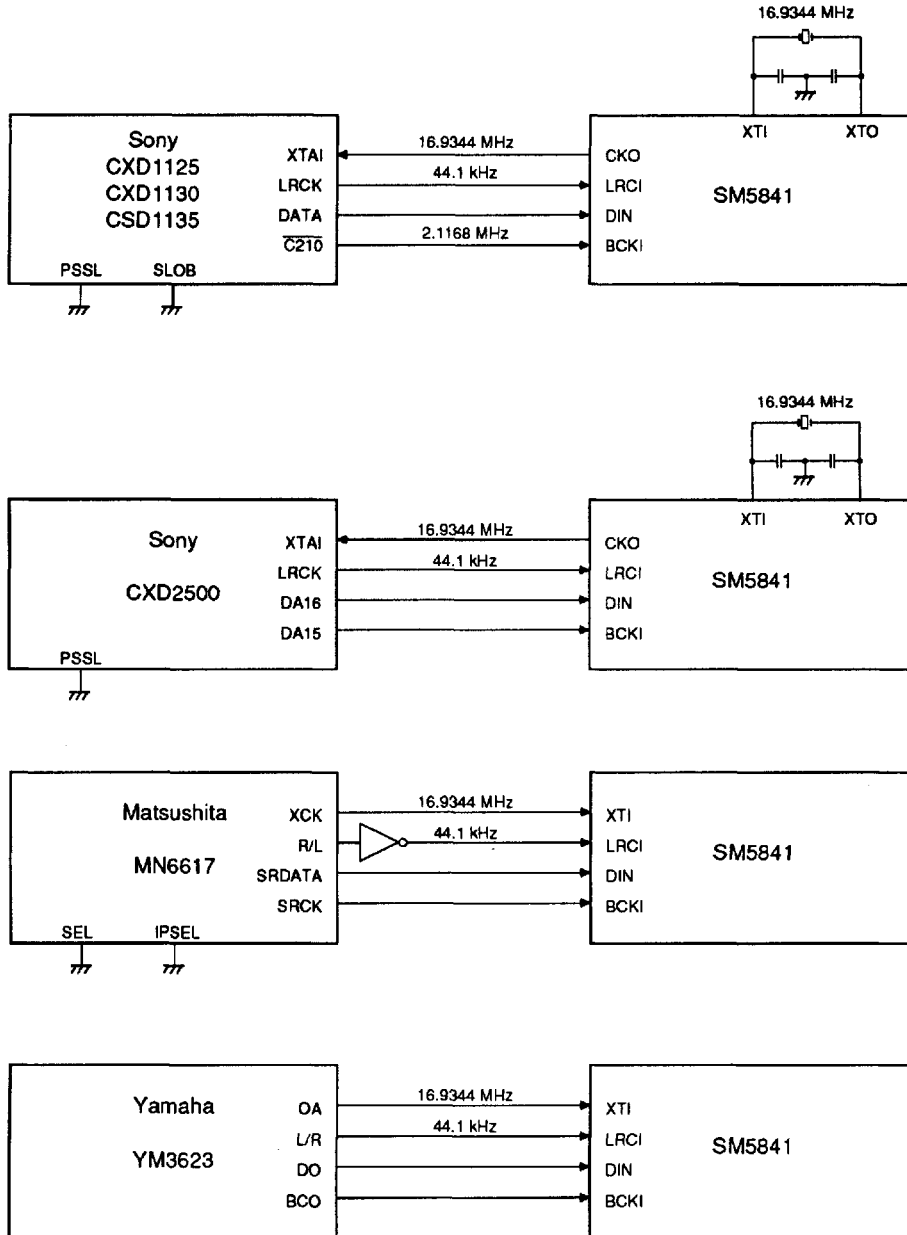
Note

The length of the output word, and hence the number of DOL and DOR bits and BCKO pulses per word, varies depending on the state of $\overline{OW16}$ and $\overline{OW20}$.

APPLICATION CIRCUITS

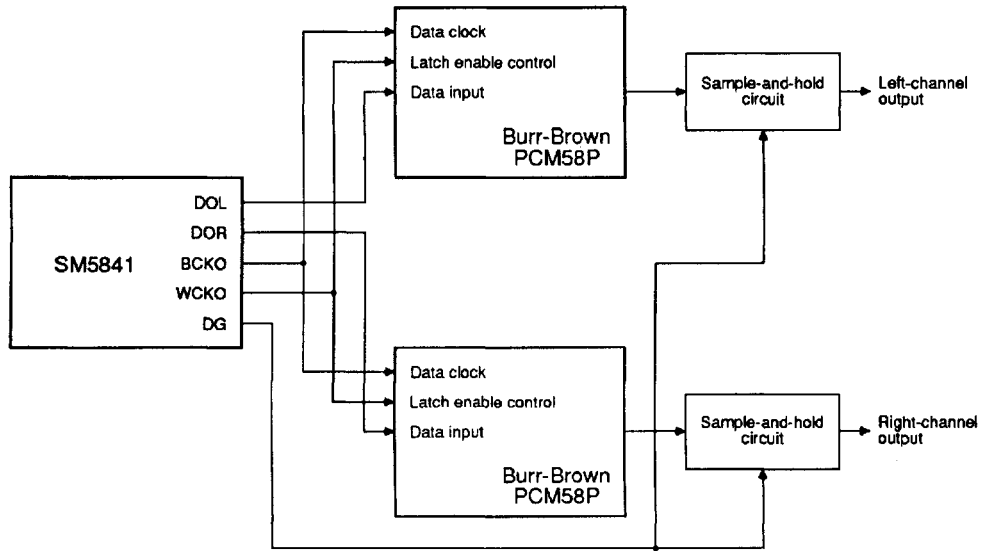
The following interface circuits all use the signal formats shown in the previous section. The timing relationships, however, need to be determined separately for each circuit.

Input Interface Circuits



Output Interface Circuits

18-bit dual D/A converter (8fs L/R alternating output mode)



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