NIPPON PRECISION CIRCUITS INC.

SM5849BF

Asynchronous Sample Rate Converter

OVERVIEW

The SM5849BF is a digital audio signal, asynchronous sample rate converter LSI. It supports 16/20/24-bit word length input data, 16/20/24-bit word length output data, 2kHz to 100kHz input sample rate range, and 4kHz to 200kHz output sample rate range. It also features a built-in digital deemphasis filter and digital attenuator.

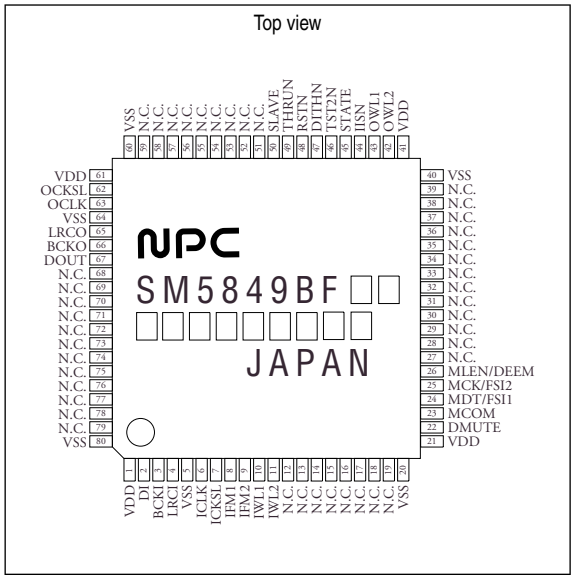
Functions

- Left/right-channel processing (stereo)
- 2 to 100kHz input sample rate range (fsi)
- 4 to 200kHz output sample rate range (fso)
- 0.45 to 2.2-times variable sample rate conversion ratio (fso/fsi)
- Asynchronous input and output timing (clock inputs)
- System clock inputs (input and output clocks independent)
  - 256fsi or 384fsi input system clock select
  - 256fso or 384fso output system clock select
- Deemphasis filter
  - IIR-type filter
  - 44.1, 48 or 32kHz
- Digital attenuator
  - 11-bit data, 1025 levels
  - Smooth attenuation change
  - +12dB gain shift function
- Direct mute function
- Through mode operation
  - Direct connection from input to output
- Output data clocks (LRCO, BCKO)
  - Slave mode: external input
  - Master mode: output system clock generated internally
- Dither round-off processing
  - Dither round-off ON/OFF selectable
- 3.3V single supply
- 80-pin QFP
- Silicon-gate CMOS process

ORDERING INFORMATION

Device	Package
SM5849BF	80-pin QFP

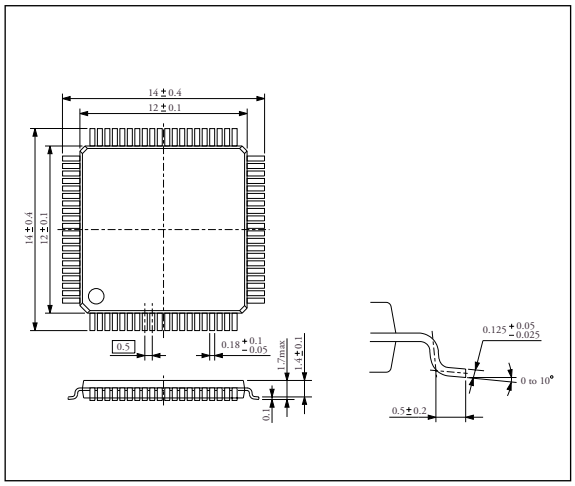
PINOUT



PACKAGE DIMENSIONS

(Unit: mm)

80-pin QFP



FEATURES

Filter Characteristics and Converter Efficiency

- 24-bit internal data word length
- Deemphasis filter characteristics (IIR filter)
  - ±0.03dB gain deviation from ideal filter characteristics
- Anti-aliasing LPF characteristics
  - Output/input sample rate conversion ratio automatic filter select (6 FIR filters)
    - Up converter LPF
      1.0 to 2.2 times
    - Down converter LPF I
      0.92 times: 48.0 to 44.1kHz
    - Down converter LPF II
      0.73 times: 44.1 to 32.0kHz
    - Down converter LPF III
      0.67 times: 48.0 to 32.0kHz
    - Down converter LPF IV
      0.5 times: 48.0 to 24.0kHz
    - Down converter LPF V
      0.45 times: 48.0 to 22.1kHz
  - ±0.00005dB passband ripple
  - > 110dB stopband attenuation
- Converter noise levels
  - ≤ −110dB internal calculation (quantization) noise
  - −98dB (16-bit output), −122dB (20-bit output), and −146dB (24-bit output) word rounding noise
- Output S/N ratio (theoretical values)

Output signal word length	S/N ratio		
	16-bit input word length	20-bit input word length	24-bit input word length
16 bits	94.8dB	97.7dB	97.7dB
20 bits	97.7dB	109.5dB	109.7dB
24 bits	97.7dB	109.7dB	110dB

Interfaces

- Input data format
  - 2s-complement, L/R alternating, serial
  - IIS/non-IIS format

Mode	Word length	Data position	Data sequence
1	16 bits	Right justified	MSB first
2		Right justified	LSB first
3		Left justified	MSB first
4		IIS	MSB first
5	20 bits	Right justified	MSB first
6		Right justified	LSB first
7		Left justified	MSB first
8		IIS	MSB first
9	24 bits	Right justified	MSB first
10		Right justified	LSB first
11		Left justified	MSB first
12		IIS	MSB first

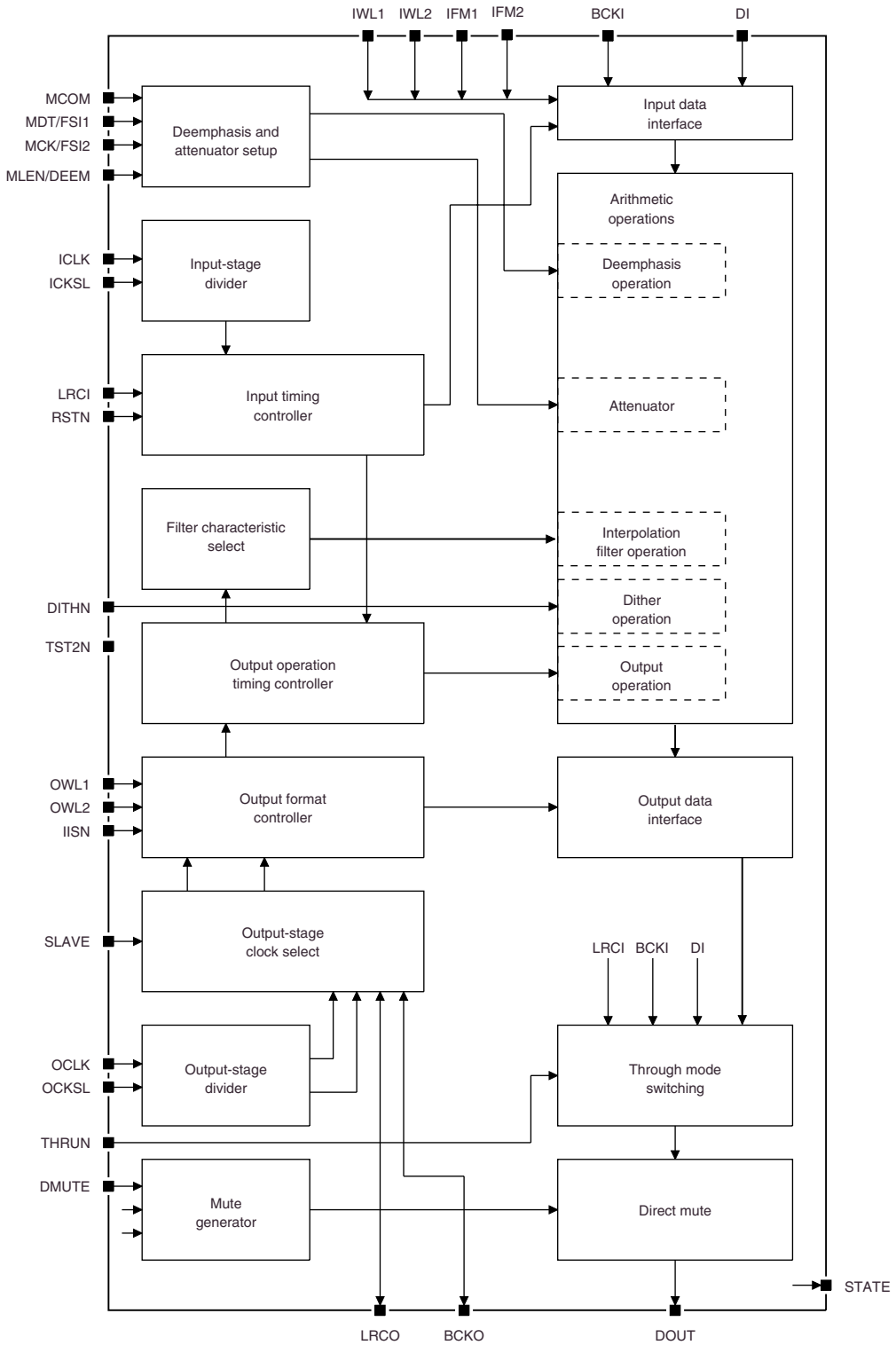
- Output data format
  - 2s-complement, MSB first, L/R alternating, serial
  - Continuous bit clock

Mode	Word length	IIS selection	Data position
1	16 bits	Normal (non IIS)	Right justified
2	20 bits		
3	24 bits		
4	24 bits		Left justified
5	16 bits	IIS	
6	20 bits		
7	24 bits		

APPLICATIONS

- Digital audio equipment-interface sample rate conversion (AV amplifiers, CD-R, DAT, MD and 8mm VTRs)
- Commercial recording/editing equipment sample rate conversion

BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Number</th><th>Name</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>1</td><td>VDD</td><td>–</td><td>Supply voltage</td></tr>
<tr><td>2</td><td>DI</td><td>Ip</td><td>Digital input signal</td></tr>
<tr><td>3</td><td>BCKI</td><td>Ip</td><td>Bit clock input</td></tr>
<tr><td>4</td><td>LRCI</td><td>Ip</td><td>Word clock input</td></tr>
<tr><td>5</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>6</td><td>ICLK</td><td>I</td><td>System clock input</td></tr>
<tr><td>7</td><td>ICKSL</td><td>Ip</td><td>System clock select. 384fs clock when HIGH, and 256fs clock when LOW.</td></tr>
<tr><td>8</td><td>IFM1</td><td>Ip</td><td rowspan="2">Input format select
<table><tr><th>IFM1</th><th>IFM2</th><th>Data position</th></tr><tr><td>LOW</td><td>LOW</td><td>Right justified</td></tr><tr><td>LOW</td><td>HIGH</td><td>Right justified[1]</td></tr><tr><td>HIGH</td><td>LOW</td><td>Left justified</td></tr><tr><td>HIGH</td><td>HIGH</td><td>IIS</td></tr></table>1. Data is in LSB first sequence</td></tr>
<tr><td>9</td><td>IFM2</td><td>Ip</td></tr>
<tr><td>10</td><td>IWL1</td><td>Ip</td><td rowspan="2">Input word length select
<table><tr><th>IWL1</th><th>IWL2</th><th>Data length</th></tr><tr><td>LOW</td><td>LOW</td><td>16 bits</td></tr><tr><td>LOW</td><td>HIGH</td><td>24 bits</td></tr><tr><td>HIGH</td><td>LOW</td><td>20 bits</td></tr><tr><td>HIGH</td><td>HIGH</td><td>24 bits</td></tr></table></td></tr>
<tr><td>11</td><td>IWL2</td><td>Ip</td></tr>
<tr><td>12</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>13</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>14</td><td>NC</td><td>–</td><td>No connection</td></tr>
<tr><td>15</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>16</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
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<tr><td>20</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>21</td><td>VDD</td><td>–</td><td>Supply voltage</td></tr>
<tr><td>22</td><td>DMUTE</td><td>Ip</td><td>Direct mute pin. Muting ON when HIGH.</td></tr>
<tr><td>23</td><td>MCOM</td><td>Ip</td><td>Microcontroller control select. Microcontroller control when HIGH.</td></tr>
<tr><td>24</td><td>MDT/FSI1</td><td>Ip</td><td>When MCON = HIGH: Microcontroller interface data input (MDT)
When MCON = LOW: Deemphasis filter fs select 1 (FSI1)</td></tr>
<tr><td>25</td><td>MCK/FSI2</td><td>Ip</td><td>When MCON = HIGH: Microcontroller interface clock (MCK)
When MCON = LOW: Deemphasis filter fs select 2 (FSI2)</td></tr>
<tr><td>26</td><td>MLEN/DEEM</td><td>Ip</td><td>When MCOM is HIGH: Microcontroller interface latch enable (MLEN)
When MCOM is LOW: Deemphasis function select (DEEM)</td></tr>
<tr><td>27</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>28</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>29</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>30</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>31</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
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<tr><td>33</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>34</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
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<tr><td>36</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>37</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
</table>

<table>
<tr><th>Number</th><th>Name</th><th>I/O[1]</th><th>Description</th></tr>
<tr><td>38</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>39</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>40</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>41</td><td>VDD</td><td>–</td><td>Supply voltage</td></tr>
<tr><td>42</td><td>OWL2</td><td>Ip</td><td rowspan="2">Output word length select
<table><tr><th>OWL1</th><th>OWL2</th><th>Data length</th></tr><tr><td>LOW</td><td>LOW</td><td>16 bits</td></tr><tr><td>LOW</td><td>HIGH</td><td>24 bits</td></tr><tr><td>HIGH</td><td>LOW</td><td>20 bits</td></tr><tr><td>HIGH</td><td>HIGH</td><td>24 bits[1]</td></tr></table>1. Data is in left justified sequence.</td></tr>
<tr><td>43</td><td>OWL1</td><td>Ip</td></tr>
<tr><td>44</td><td>IISN</td><td>Ip</td><td>IIS output mode select. Normal mode when HIGH, and IIS mode when LOW.</td></tr>
<tr><td>45</td><td>STATE</td><td>O</td><td>Status output</td></tr>
<tr><td>46</td><td>TST2N</td><td>Ip</td><td>IC test mode pin 2. Test mode when LOW. Leave HIGH or open circuit for normal operation.</td></tr>
<tr><td>47</td><td>DITHN</td><td>Ip</td><td>Output dither control pin. Dither when LOW, and normal mode when HIGH.</td></tr>
<tr><td>48</td><td>RSTN</td><td>Ip</td><td>Reset input. Reset when LOW.</td></tr>
<tr><td>49</td><td>THRUN</td><td>Ip</td><td>Through mode set. Normal mode when HIGH, and through mode when LOW.</td></tr>
<tr><td>50</td><td>SLAVE</td><td>Ip</td><td>Slave mode set. Slave mode when HIGH, and master mode when LOW.</td></tr>
<tr><td>51</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>52</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
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<tr><td>60</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>61</td><td>VDD</td><td>–</td><td>Supply voltage</td></tr>
<tr><td>62</td><td>OCKSL</td><td>Ip</td><td>Output system clock select. 384fs when HIGH, and 256fs when LOW.</td></tr>
<tr><td>63</td><td>OCLK</td><td>I</td><td>Output system clock input</td></tr>
<tr><td>64</td><td>VSS</td><td>–</td><td>Ground</td></tr>
<tr><td>65</td><td>LRCO</td><td>O</td><td>Word clock output</td></tr>
<tr><td>66</td><td>BCKO</td><td>O</td><td>Bit clock output</td></tr>
<tr><td>67</td><td>DOUT</td><td>O</td><td>Data output</td></tr>
<tr><td>68</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
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<tr><td>75</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>76</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>77</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>78</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>79</td><td>NC</td><td>–</td><td>No connection (must be open)</td></tr>
<tr><td>80</td><td>VSS</td><td>–</td><td>Ground</td></tr>
</table>

1. Ip = input pin with internal pull-up resistor

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Rating[1]	Unit
Supply voltage range	V_{DD}	–0.3 to 4.0	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–55 to 125	°C
Power dissipation	P_D	400	mW

1. Ratings also apply at supply switch ON and OFF.

Recommended Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	3.0 to 3.6	V
Operating temperature range	T_{opr}	–40 to 85	°C

DC Electrical Characteristics

V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = –40 to 85°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	No output load	–	70	100	mA
HIGH-level input voltage[1]	V_{IH1}		2.0	–	–	V
LOW-level input voltage[1]	V_{IL1}		–	–	0.8	V
HIGH-level input voltage[2]	V_{IH2}		2.0	–	–	V
LOW-level input voltage[2]	V_{IL2}		–	–	0.8	V
HIGH-level output voltage[3]	V_{OH}	I_{OH} = –1.0mA	V_{DD}–0.4	–	–	V
LOW-level output voltage[3]	V_{OL}	I_{OL} = 1.0mA	–	–	0.4	V
HIGH-level input current[2]	I_{IH}	V_{IN} = V_{DD}	–	–	1.0	µA
LOW-level input current[2]	I_{IL}	V_{IN} = 0V	–	–	90	µA
Input leakage current[1]	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA
	I_{LL}	V_{IN} = 0V	–	–	1.0	µA

1. Pins ICLK and OCLK.
2. Pins DI, BCKI, LRCI, ICKSL, IFM1, IFM2, IWL1, IWL2, DMUTE, MCOM, MDT/FSI1, MCK/FSI2, MLEN/DEEM, OWL1, OWL2, IISN, DITHN, TST2N, RSTN, THRUN, SLAVE, OCKSL.
3. Pins STATE, LRCO, BCKO, DOUT.

AC Electrical Characteristics

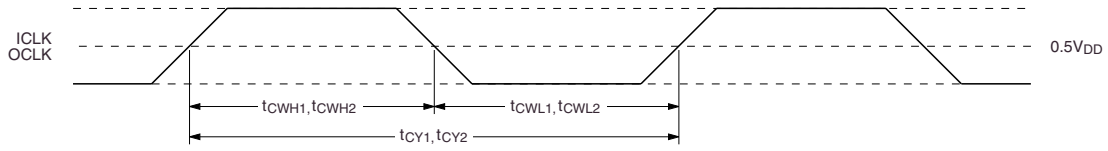
Input clock (ICLK)

Parameter	Symbol	Condition	Rating			Unit
		System clock	min	typ	max	
HIGH-level clock pulsewidth	t_{CWH1}	256fsi	17.5	–	–	ns
		384fsi	11.7	–	–	
LOW-level clock pulsewidth	t_{CWL1}	256fsi	17.5	–	–	ns
		384fsi	11.7	–	–	
Clock pulse cycle	t_{CY1}	256fsi	39.0	–	2000	ns
		384fsi	26.0	–	1300	

Output clock (OCLK)

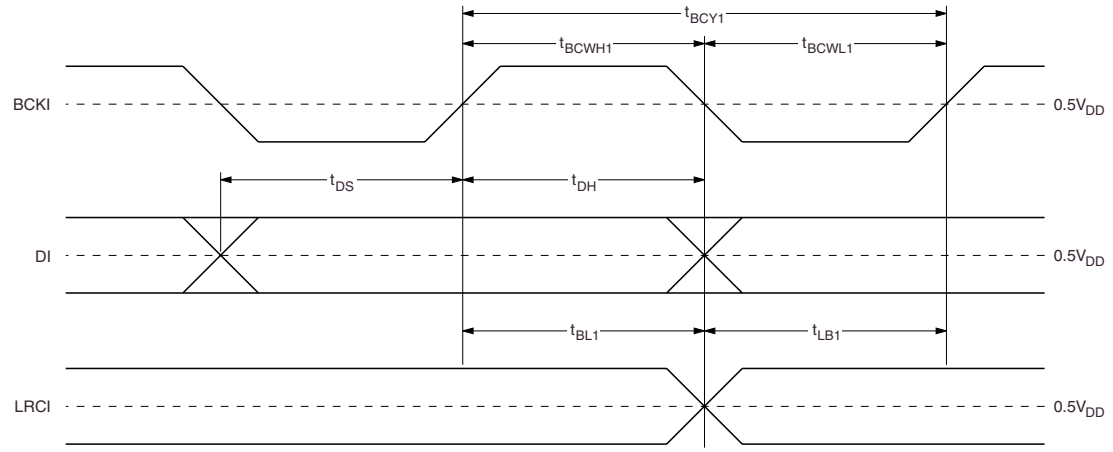
Parameter	Symbol	Condition	Rating			Unit
		System clock	min	typ	max	
HIGH-level clock pulsewidth	t_{CWH2}	256fso	8.7	–	–	ns
		384fso	5.8	–	–	
LOW-level clock pulsewidth	t_{CWL2}	256fso	8.7	–	–	ns
		384fso	5.8	–	–	
Clock pulse cycle	t_{CY2}	256fso	19.5	–	1000	ns
		384fso	13.0	–	650	

ICLK and OCLK timing



Serial inputs (DI, LRCI, BCKI)

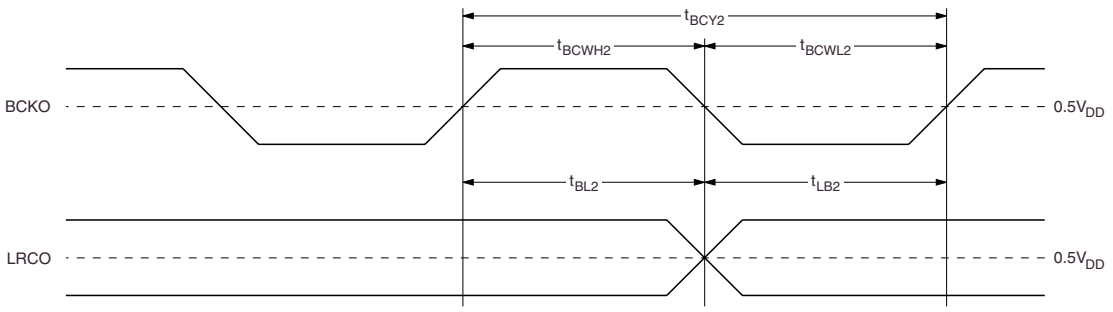
Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH1}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL1}	50	–	–	ns
BCKI pulse cycle	t_{BCY1}	100	–	–	ns
DI setup time	t_{DS}	50	–	–	ns
DI hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL1}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB1}	50	–	–	ns



Serial inputs (LRCO, BCKO: SLAVE = HIGH)

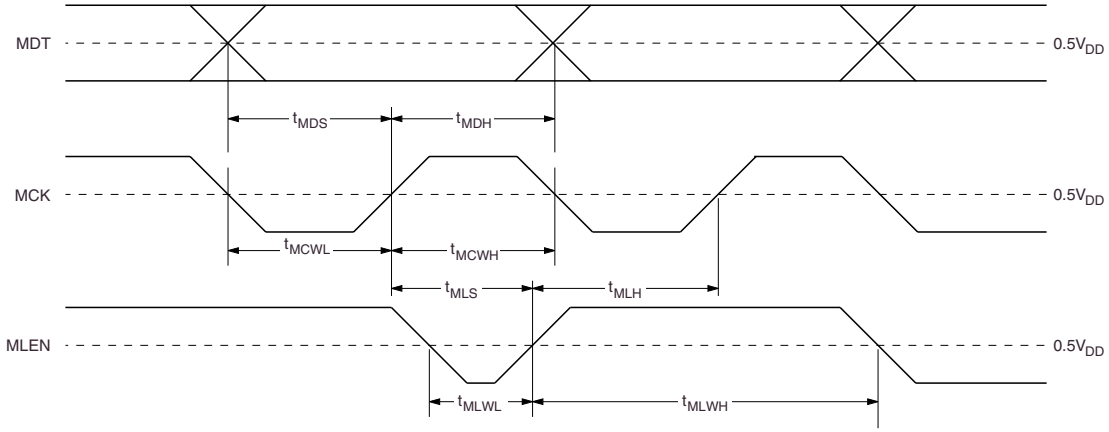
Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKO HIGH-level pulsewidth	t_{BCWH2}	39	–	–	ns
BCKO LOW-level pulsewidth	t_{BCWL2}	39	–	–	ns
BCKO pulse cycle	t_{BCY2}	78	–	–	ns
Last BCKO rising edge to LRCO edge	t_{BL2}	39	–	–	ns
LRCO edge to first BCKO rising edge	t_{LB2}	39	–	–	ns

Note: BCKO clock inputs exceeding 64 fso cannot be detected, and will cause incorrect operation.



Microcontroller interface (MCK, MDT, MLEN)

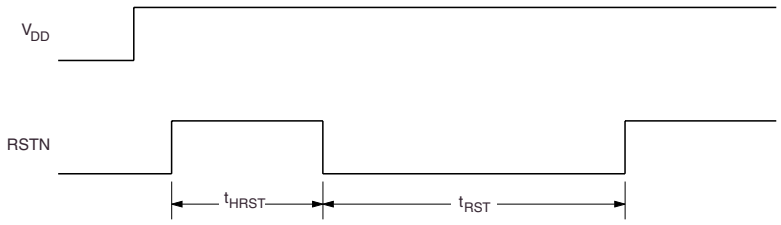
Parameter	Symbol	Rating			Unit
		min	typ	max	
MCK LOW-level pulsewidth	t_{MCWL}	50	–	–	ns
MCK HIGH-level pulsewidth	t_{MCWH}	50	–	–	ns
MDT setup time	t_{MDS}	50	–	–	ns
MDT hold time	t_{MDH}	50	–	–	ns
MLEN LOW-level pulsewidth	t_{MLWL}	50	–	–	ns
MLEN HIGH-level pulsewidth	t_{MLWH}	50	–	–	ns
MLEN setup time	t_{MLS}	50	–	–	ns
MLEN hold time	t_{MLH}	50	–	–	ns



Reset input (RSTN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
First HIGH-level pulsewidth after supply ON	t_{HRST}	–	640	–	t_{CY}
RSTN pulsewidth	t_{RST}	64	–	–	t_{CY}

Note: t_{CY} is the system clock input cycle time.
t_{RST} = approximately 3.8µs when t_{CY} = 59ns.



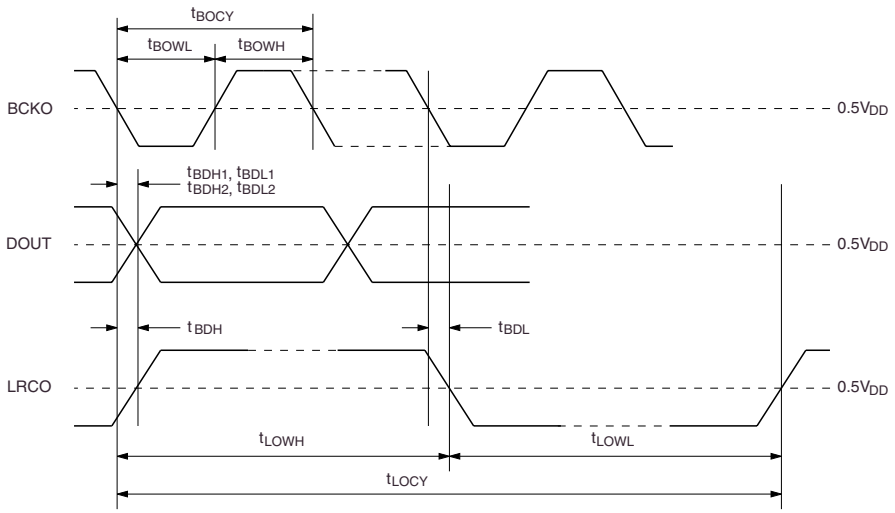
Serial outputs (DOUT, BCKO, LRCO)

SLAVE = LOW, C_L = 15pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LRCO pulse cycle	t_{LOCY}		–	1/fso	–	ns
LRCO LOW-level pulsewidth	t_{LOWL}		–	1/2fso	–	ns
LRCO HIGH-level pulsewidth	t_{LOWH}		–	1/2fso	–	ns
BCKO pulse cycle	t_{BOCY}	OCKSL = LOW	–	1/64fso	–	ns
		OCKSL = HIGH	–	1/48fso	–	
BCKO LOW-level pulsewidth	t_{BOWL}	OCKSL = LOW	–	1/128fso	–	ns
		OCKSL = HIGH	–	1/96fso	–	
BCKO HIGH-level pulsewidth	t_{BOWH}	OCKSL = LOW	–	1/128fso	–	ns
		OCKSL = HIGH	–	1/96fso	–	
BCKO to DOUT and LRCO delay time	t_{BDH1}	BCKO fall to DOUT, LRCO rise	–5	–	20	ns
	t_{BDL1}	BCKO fall to DOUT, LRCO fall	–5	–	20	ns

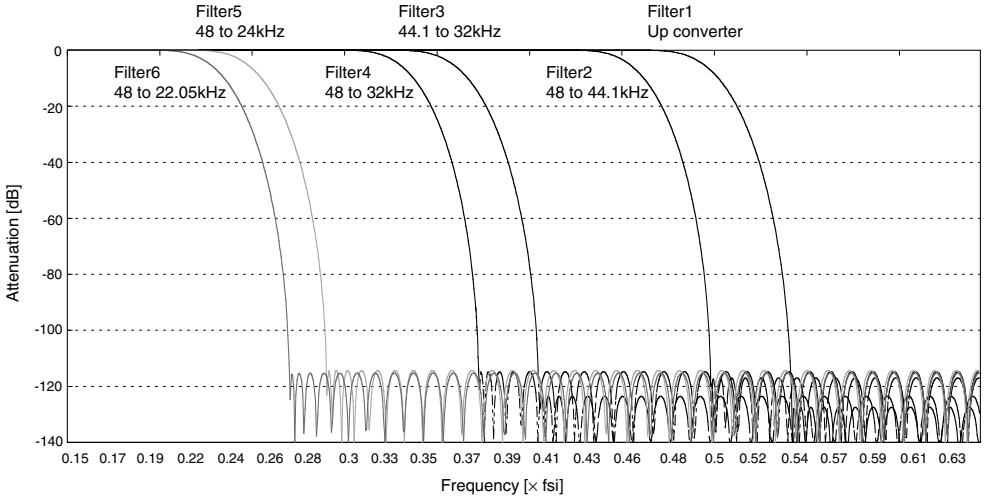
SLAVE = HIGH, C_L = 15pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKO to DOUT delay time	t_{BDH2}	BCKO fall to DOUT rise	0	–	50	ns
	t_{BDL2}	BCKO fall to DOUT fall	0	–	50	ns

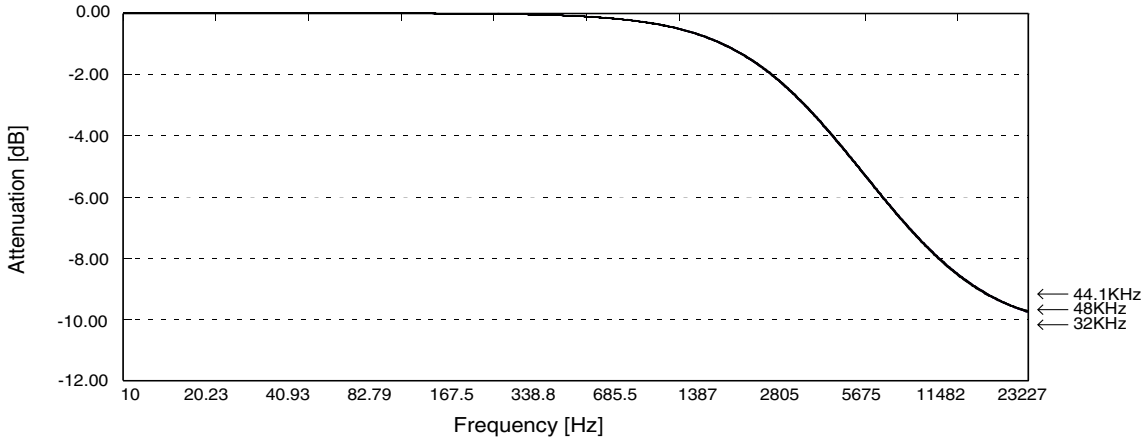


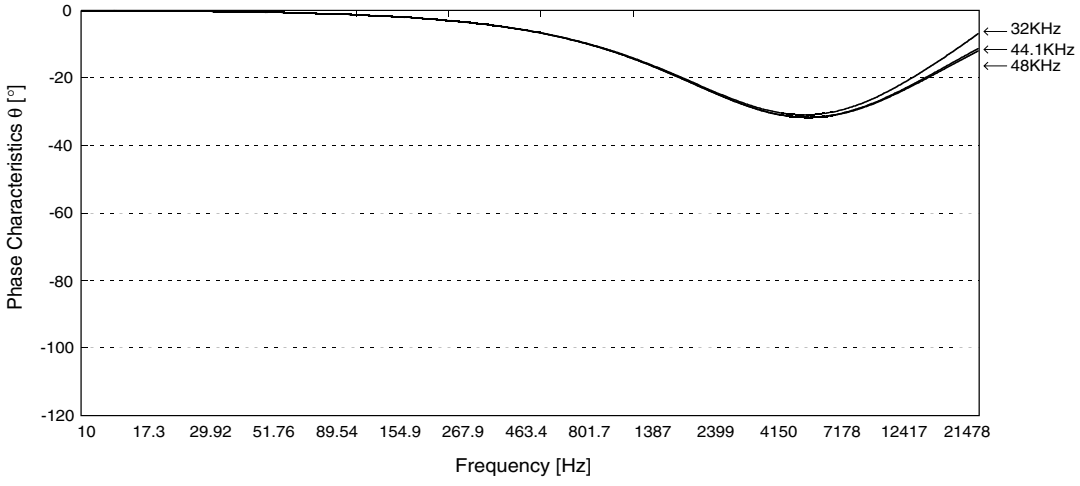
Filter Characteristics

Anti-aliasing filter frequency characteristic



Deemphasis filter frequency characteristic





FUNCTIONAL DESCRIPTION

Input Data Interface (DI, LRCI, BCKI, IFM1, IFM2, IWL1, IWL2)

Table 1. Input data format (IFM1, IFM2, IWL1, IWL2)

Mode	IFM1	IFM2	IWL1	IWL2	Word length	Data position	Data sequence
1	LOW	LOW	LOW	LOW	16 bits	Right justified	MSB first
2	LOW	HIGH				Right justified	LSB first
3	HIGH	LOW				Left justified	MSB first
4	HIGH	HIGH				IIS	MSB first
5	LOW	LOW	HIGH	LOW	20 bits	Right justified	MSB first
6	LOW	HIGH				Right justified	LSB first
7	HIGH	LOW				Left justified	MSB first
8	HIGH	HIGH				IIS	MSB first
9	LOW	LOW	LOW or HIGH	HIGH	24 bits	Right justified	MSB first
10	LOW	HIGH				Right justified	LSB first
11	HIGH	LOW				Left justified	MSB first
12	HIGH	HIGH				IIS	MSB first

Attenuator and Deemphasis Selection

The attenuator is set using the microcontroller interface. When the attenuator is used, deemphasis settings also need to be set using the microcontroller interface. The microcontroller interface comprises MDT, MCK and MLEN, and is used to transfer all input serial data.

Table 2. Attenuator and deemphasis function select

Function	Function set method	
	External pins (MCOM = LOW)	Microcontroller interface (MCOM = HIGH)
Deemphasis ON/OFF	DEEM	FDEEM
Deemphasis frequency (fsi) select	FSI1, FSI2	FFSI1, FFSI2
Attenuator data set	N/A (no attenuation)	11 bits (B0 to B10)
Test mode select	N/A (test mode 1)	FTST1, FTST2

MCON should not be switched after a power-ON reset.

When MCOM is HIGH, serial data received on MDT, MCK and MLEN sets the attenuation data and control flag data.

When MCOM is LOW, the logic levels on FSI1, FSI2 and DEEM select the device function.

Microcontroller Interface (MCOM, MDT, MCK, MLEN)

When MCOM is HIGH, the microcontroller interface is active, comprising MDT (data), MCK (clock) and MLEN (latch enable clock) interface pins.

Input data on MDT is synchronized to the MCK clock. Data is read into the input stage shift register on the rising edge of MCK. Accordingly, the input data should change on the falling edge of MCK. Input data enters an internal SIPO (serial-to-parallel converter register), and then the parallel data is latched into the mode register on the rising edge of the latch enable clock MLEN.

The mode register addressed is determined by bit D1 of the 12 data bits before MLEN goes HIGH. If this bit is LOW, then the data is read into the attenuation data register as shown in figure 1. If this bit is HIGH, then the data is read into the mode flag register as shown in figure 2. The function of each bit in the mode flag register is described in table 3.

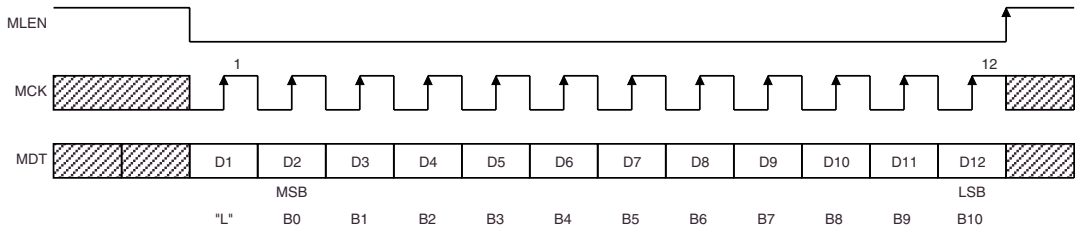


Figure 1. Attenuation data format (D1 = LOW)

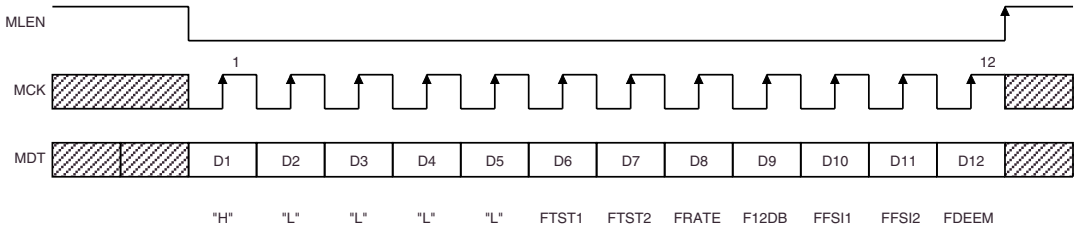


Figure 2. Mode flag data format (D1 = HIGH)

Table 3. Mode flag description

<table>
<tr><th rowspan="2">D1</th><th rowspan="2">Bit</th><th rowspan="2">Mode flag</th><th colspan="3">Mode function select</th><th rowspan="2">Reset mode</th></tr>
<tr><th>Parameter</th><th>LOW/HIGH</th><th>Select</th></tr>
<tr><td rowspan="8">HIGH</td><td>D2 to D7</td><td>(Not used)</td><td>Test mode select</td><td></td><td>IC test mode flags.
Not used for normal operation.
D2 to D7 should be set LOW.</td><td>LOW</td></tr>
<tr><td rowspan="2">D8</td><td rowspan="2">FRATE</td><td rowspan="2">Input/output rate</td><td>HIGH</td><td>Set the input/output sample rate ratio for each output sample</td><td rowspan="2">LOW</td></tr>
<tr><td>LOW</td><td>Set the input/output sample rate ratio with high accuracy every 2048 output samples</td></tr>
<tr><td rowspan="2">D9</td><td rowspan="2">F12DB</td><td rowspan="2">Attenuator</td><td>HIGH</td><td>+12dB gain shift</td><td rowspan="2">LOW</td></tr>
<tr><td>LOW</td><td>No gain shift (normal operation)</td></tr>
<tr><td>D10</td><td>FFSI1</td><td>Deemphasis filter fs select 1</td><td></td><td rowspan="2">fsi select
<table><tr><th>FFSI2</th><th>FFSI1</th><th>fsi</th></tr><tr><td>LOW</td><td>LOW</td><td rowspan="2">44.1kHz</td></tr><tr><td>LOW</td><td>HIGH</td></tr><tr><td>HIGH</td><td>LOW</td><td>48.0kHz</td></tr><tr><td>HIGH</td><td>HIGH</td><td>32.0kHz</td></tr></table></td><td>LOW</td></tr>
<tr><td>D11</td><td>FFSI2</td><td>Deemphasis filter fs select 2</td><td></td><td>LOW</td></tr>
<tr><td rowspan="2">D12</td><td rowspan="2">FDEEM</td><td rowspan="2">Deemphasis control ON/OFF</td><td>HIGH</td><td>Deemphasis filter ON</td><td rowspan="2">LOW</td></tr>
<tr><td>LOW</td><td>Deemphasis filter OFF</td></tr>
</table>

Deemphasis (DEEM, FSI1, FSI2 pins or FDEEM, FFSI1, FFSI2 flags)

The digital deemphasis filter is an IIR filter with variable coefficients to faithfully reproduce the gain and phase characteristics of analog deemphasis filters.

The filter coefficients are selected by FSI1 (or FFSI1 flag) and FSI2 (or FFSI2 flag) to correspond to the sampling frequencies fs = 44.1, 48.0 and 32.0kHz.

Table 4. Deemphasis ON/OFF

DEEM (MCOM = LOW)	FDEEM (MCOM = HIGH)	Deemphasis
HIGH		ON
LOW		OFF

Table 5. Deemphasis fs select (FSI1, FSI2 pins or FFSI1, FFSI2 flags)

MCOM = LOW (MCOM = HIGH)		fs
FSI1 (FFSI1)	FSI2 (FFSI2)	
LOW	LOW	44.1kHz
HIGH	LOW	
LOW	HIGH	48.0kHz
HIGH	HIGH	32.0kHz

Attenuation (MDT, MCK, MLEN)

The digital attenuator coefficients are read in as serial data on the microcontroller interface. Data on MDT is read into the internal shift register on the rising edge of MCK, and then 12 bits are latched internally on the rising edge of MLEN.

When the leading bit is 0 (D1 = LOW), the following 11 bits are read into the attenuation register and used as an unsigned integer in MSB first format. See figure 3.

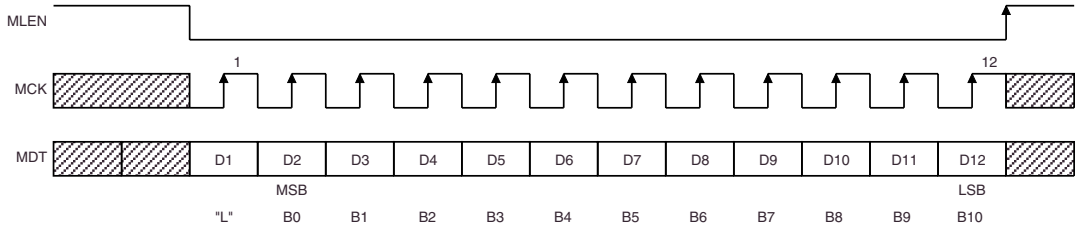


Figure 3. Attenuation data format (microcontroller interface)

Although the attenuation data comprises 11 bits, only 1025 levels are valid as given by the following.

$$\mathrm{DATT} = \sum_{i=0}^{10} a_i \times 2^{(10-i)}$$

The gain of the attenuator for values of DATT from 001H to 400H are given by the following equations. Note that when the F12DB flag is HIGH, the gain is shifted by a fixed +12.0412dB.

$$\mathrm{Gain} = 20 \times \log\left(\frac{\mathrm{DATT}}{1024}\right)[\mathrm{dB}]$$

when F12DB = LOW

$$= 20 \times \log\left(\frac{\mathrm{DATT}}{256}\right)[\mathrm{dB}]$$

when F12DB = HIGH

After a system reset initialization, DATT is set to 400H and the F12DB flag is LOW, corresponding to 0dB gain. (The F12DB flag is described in table 3.)

Table 6. Attenuator settings

D1	Attenuation data DATT	F12DB = LOW (default)		F12DB = HIGH	
		Gain (dB)	Linear expression	Gain (dB)	Linear expression
LOW	000H	–∞	0.0	–∞	0.0
	001H	–60.206	1/1024	–48.165	1/256
	↓	↓	↓	↓	↓
	100H	–12.041	256/1024	0.0	256/256
	↓	↓	↓	↓	↓
	3FFH	–0.0085	1023/1024	12.032	1023/256
	400H (to 7FFH)	0	1.0	12.041	4.0

Attenuator operation

A change in the attenuation data DATT causes the gain to change smoothly from its previous value towards the new setting. The new attenuation data is stored in the attenuation data register and the current attenuation level is stored in a temporary register. Consequently, if a new attenuation level is read in before the previously set level is reached, the gain changes smoothly from the current value towards the latest setting as shown in figure 4.

The attenuation counter output changes, and hence the gain changes, by 1 step every output sample. The time taken to reduce the gain from 0dB (or 12dB) to −∞dB is (1024/fso), which corresponds to approximately 23.2ms when fso = 44.1kHz.

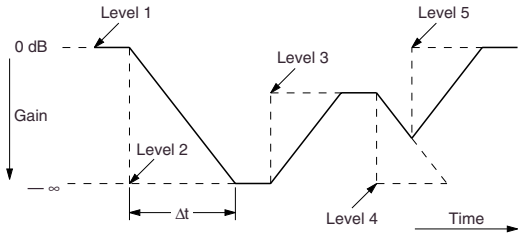


Figure 4. Attenuator operation example

Mute (DMUTE)

Direct mute

Table 7. DMUTE operation ON/OFF

DMUTE	Function
LOW	Normal data is output from the next output word (mute OFF)
HIGH	0 data is output from the next output word (mute ON)

Other mute operations

The direct mute function is also invoked at the following times.

- When the reset input (RSTN) changes.
- When the fs setting changes, for deemphasis, using either FSI1, FSI2 inputs or FFSI1, FFSI2 flags.[1]
- When the ICKSL, IFM1, or IFM2 setting changes.
- When the ICLK input system clock stops.

Table 8. Other mute operations

Input	Function
RSTN = LOW	0 data is output from the next output word (mute ON)
RSTN = HIGH	Normal data is output from the 3073rd output word (mute OFF)
FSI1, FSI2 input settings changed (MCOM = LOW).[1] FFSI1, FFSI2 input settings changed (MCOM = HIGH).[1]	0 data is output from the next output word (mute ON). Normal data is output from the 3073rd output word (mute OFF)
ICKSL, IFM1, IFM2 input settings change.	
ICLK input system clock stops.	0 data is output from the next output word (mute ON)
ICLK input system clock restarts.	Normal data is output from the 3073rd output word (mute OFF)

1. Mute function does not operate when the deemphasis filter ON/OFF is switched (DEEM (MCOM = LOW), FDEEM (MCOM = HIGH)).

Internal Operating Status (STATE)

Internally, all functions are performed on 24-bit serial data, and the conversion rate and filter type are selected accordingly. The output format is 24-bit left-justified.

Table 9. Status data description

<table>
<tr><th>Output bit position</th><th colspan="2">Content</th></tr>
<tr><td>1 to 20</td><td colspan="2">(Output data cycle/input data cycle) – 129
Ex.
1st 20th
00.111111111111011111 ⇒ 1.0 times
01.111111111111011111 ⇒ 2.0 times (1/2 conversion rate ratio)
00.011111111111011111 ⇒ 0.5 times (2.0 conversion rate ratio)</td></tr>
<tr><td>21</td><td colspan="2">Not used.</td></tr>
<tr><td>22</td><td>DA2</td><td rowspan="3">Selected filter type
<table><tr><th>DA2</th><th>DA1</th><th>DA0</th><th>Filter type</th><th>Conversion frequency (example)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Up converter</td></tr><tr><td>0</td><td>0</td><td>1</td><td>2</td><td>48 to 44.1kHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>3</td><td>44.1 to 32kHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4</td><td>48 to 32kHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>5</td><td>96 to 48kHz, 48 to 24kHz</td></tr><tr><td>1</td><td>0</td><td>1</td><td>6</td><td>96 to 44.1kHz, 48 to 22.05kHz</td></tr></table></td></tr>
<tr><td>23</td><td>DA1</td></tr>
<tr><td>24</td><td>DA0</td></tr>
</table>

Note that when THRUN is LOW, LRCO and BCKO are not guaranteed to be synchronized to the STATE output.

Input System Clock (ICLK, ICKSL)

The input system clock can be set to run at either 256fsi or 384fsi, where fsi is the input frequency on LRCI.

Note that ICLK and LRCI should be divided from a common clock source or PLL to maintain synchronism.

Table 10. ICKSL and input system clock

ICKSL	ICLK system clock rate
HIGH	384fsi
LOW	256fsi

Output System Clock (OCLK, OCKSL)

The output system clock can be set to run at either 256fso or 384fso, where fso is the output frequency on LRCO. In through mode, OCLK and OCKSL have no function and are not used.

Note that even in slave mode, a suitable clock must be input on OCLK. A malfunction prevention circuit uses this clock so that operation continues when the ICLK stops.

Table 11. SLAVE, OCKSL and output system clock

SLAVE	OCKSL	OCLK system clock rate
LOW	HIGH	384fso
	LOW	256fso
HIGH	×	Not used

Output Data Interface and Output Clock Selection (LRCO, BCKO, DOUT, SLAVE)

Table 12. Output mode description

THRUN	SLAVE	Function		
		Mode	Description	LRCO, BCKO state
HIGH	LOW	Master mode	Output word clock (LRCO) and output bit clock (BCKO) are divided from OCLK.	Outputs
	HIGH	Slave mode	Output word clock (LRCO) and output bit clock (BCKO) are supplied externally.	Inputs[1]
LOW	×	Through mode	Output word clock (LRCO), output bit clock (BCKO) and output data (DOUT) are the same as LRCI, BCKI and DI, respectively. DMUTE is valid.	Outputs

1. The number of BCKO input clock cycles should not exceed 64 per word. Correct operation is not guaranteed beyond these limits.

Output Format Control (OWL1, OWL2, IISN)

The output is in MSB-first, 2s-complement, L/R alternating, bit serial format with a continuous bit clock.

Mode	Inputs			Output format		
	IISN	OWL2	OWL1	Word length	IIS selection	Data position
1	HIGH	LOW	LOW	16 bits	Normal (non IIS)	Right justified
2		LOW	HIGH	20 bits		
3		HIGH	LOW	24 bits		
4		HIGH	HIGH	24 bits		Left justified
5	LOW	LOW	LOW	16 bits	IIS	
6		LOW	HIGH	20 bits		
7		HIGH	×	24 bits		

Output Timing Calculation

The output timing is controlled to maintain the desired ratio between the output data cycle and the input data cycle.

Output round-off processing

The internal processor data length and output data length are different, making output data round-off processing necessary. The SM5849BF supports selectable normal round-off processing and trigonometric function dither round-off processing*.

*TPDF: Triangular Probability Density Function

DITHN	Output round-off processing
HIGH	Normal round-off
LOW	Dither round-off

Filter Characteristic Selection

Conversion rates from 0.45 to 2.2 times are supported using the following 6 filter types.

The ratio between the output sample rate and input sample rate is measured automatically and the most suitable filter type for this ratio is selected automatically.

Table 13. fs ratio and filter selection

Filter mode	fs ratio (fso/fsi)	Selects range	Conversion frequency (example)
1	1.0 to 2.2	≥ 0.969697	Up converter
2	0.91875	0.864865 to 0.969697	48.0 to 44.1kHz
3	0.72562	0.711111 to 0.864865	44.1 to 32.0kHz
4	0.66667	0.627451 to 0.711111	48 to 32kHz
5	0.50000	0.492308 to 0.627451	48 to 24kHz, 96 to 48kHz
6	0.459375	≤ 0.492308	48 to 22.05kHz, 96 to 44.1kHz

When the selected fs conversion ratio and the actual sample rate conversion ratio do not coincide, the following phenomenon occur.

Table 14. Mismatch condition and response

Condition[1]	Response
Actual sample rate conversion ratio is lower than the selected filter conversion ratio	The audio band high-pass develops aliasing noise.
Actual sample rate conversion ratio is higher than the selected filter conversion ratio	The audio band high-pass is cut off.

1. An output noise may be generated if the fs conversion ratio changes at a rate greater 0.119%/sec.

System Reset (RSTN)

At power-ON, all device functions must be reset. The device is reset by applying a LOW-level pulse on RSTN. At system reset, the internal arithmetic operation, output timing counter and internal flag register operation are synchronized on the next LRCI rising edge. Note that all flags are set to their defaults (all LOW).

A power-ON reset signal can be applied from an external microcontroller. For systems where ICLK, BCKI, and LRCI are stable at power ON, initialization can be performed by connecting a 0.001µF capacitor between RSTN and VSS. Otherwise, a capacitor value should be chosen such that RSTN does not go HIGH until after LRCI, BCKI, and ICLK have stabilized.

Through Mode (THRUN)

Table 15. Through mode function description

THRUN	Mode	Description
LOW	Through mode	Direct connections are made: LRCI to LRCO, BCKI to BCKO, and DI to DOUT. DMUTE is valid.
HIGH	Normal mode	Sample rate converter operation

Synchronizing Internal Arithmetic Timing

The clock on LRCI should pass through 1 cycle for every 384 (ICKSL = HIGH) or 256 (ICKSL = LOW) ICLK clock cycles to maintain correct internal arithmetic sequence. If the number of ICLK cycles is different, increases or decreases, or any jitter is present, device operation could be affected.

There is a fixed-value tolerance within which the internal sequence and LRCI clock timing are not adversely affected.

Table 16. ICLK and clock tolerance

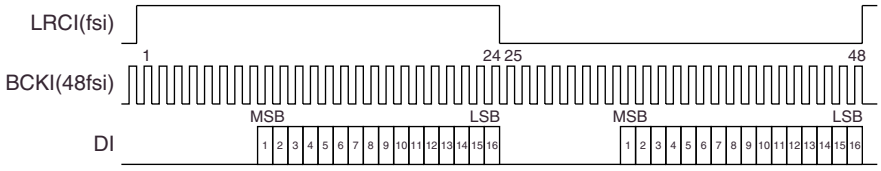
ICKSL	Allowable clock variation
HIGH (384fs mode)	+8 to –6 cycles
LOW (256fs mode)	+4 to –3 cycles

Whenever the allowable tolerance is exceeded, the internal sequence start-up may be delayed or fail. When this occurs, there is a possibility that a click noise will be generated.

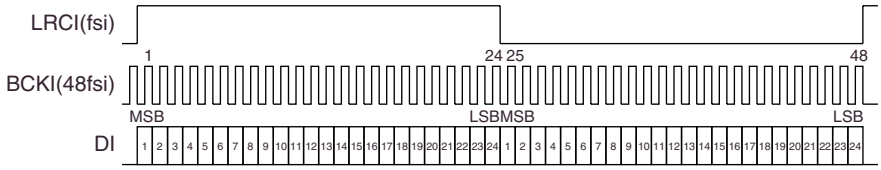
TIMING DIAGRAMS

Input Timing Examples (DI, BCKI, LRCI)

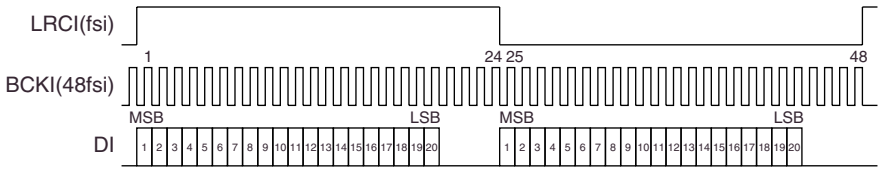
Audio data input timing (right-justified 16-bit word, IFM1 = L, IFM2 = L, IWL1 = L, IWL2 = L)



Audio data input timing (right-justified 24-bit word, IFM1 = L, IFM2 = L, IWL1 = H, IWL2 = H)

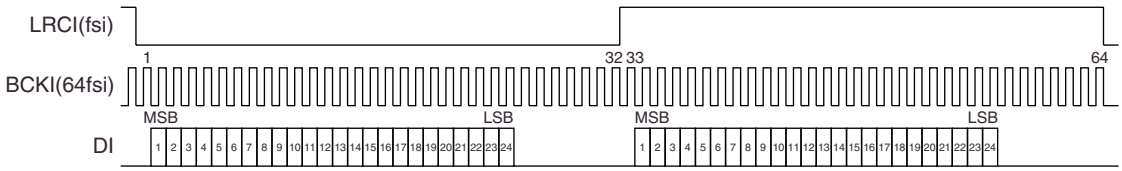


Audio data input timing (left-justified 20-bit word, IFM1 = H, IFM2 = L, IWL1 = H, IWL2 = L)

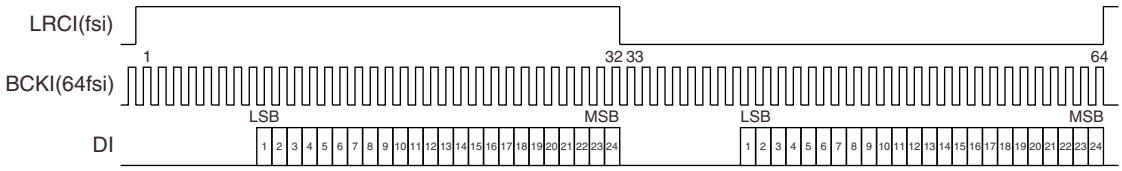


All data bits after the LSB (20th bit) are ignored. Note that more than 20 BCKI cycles are required.

Audio data input timing (IIS-format 24-bit word, IFM1 = H, IFM2 = H, IWL1 = L, IWL2 = H)

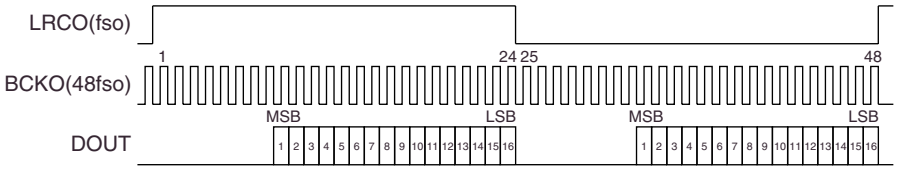


Audio data input timing (right-justified 24-bit word, LSB first, IFM1 = H, IFM2 = H, IWL1 = L, IWL2 = H)

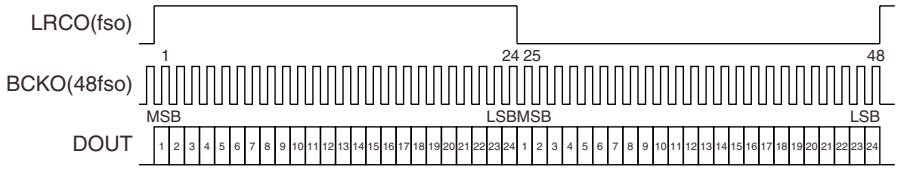


Output Timing Examples (DOUT, BCKO, LRCO)

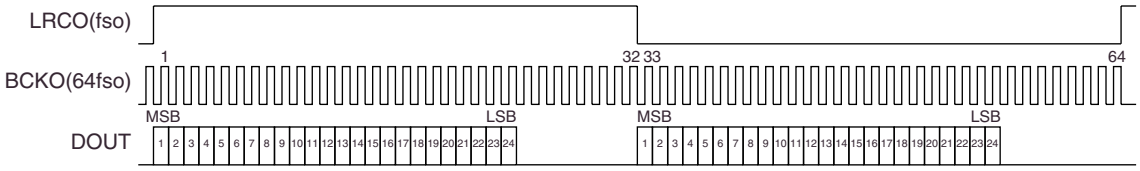
Audio data output timing (right-justified 16-bit word, IISN = H, OWL1 = L, OWL2 = L)



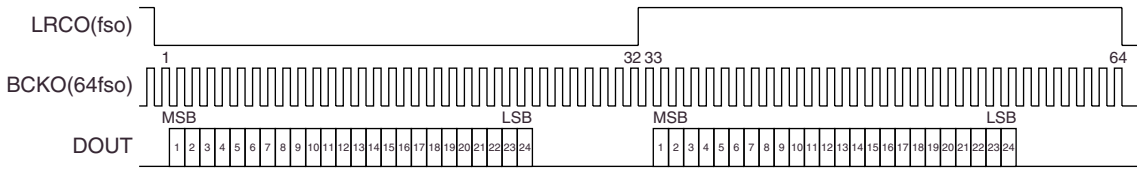
Audio data output timing (right-justified 24-bit word, IISN = H, OWL1 = L, OWL2 = H)



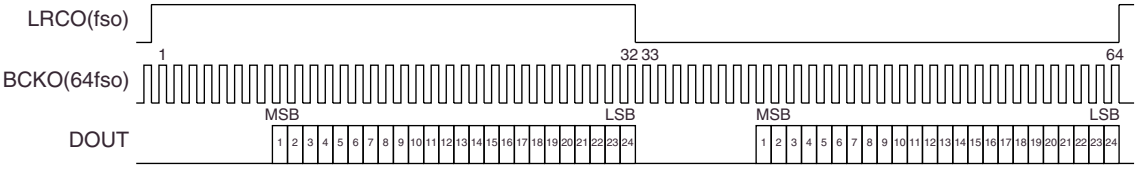
Audio data output timing (left-justified 24-bit word, IISN = H, OWL1 = H, OWL2 = H)



Audio data output timing (IIS-format 24-bit word, IISN = L, OWL1 = L, OWL2 = H)



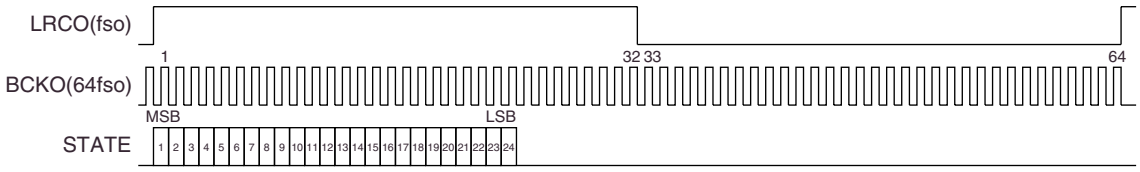
Audio data output timing (right-justified 24-bit word, IISN = H, OWL1 = L, OWL2 = H)



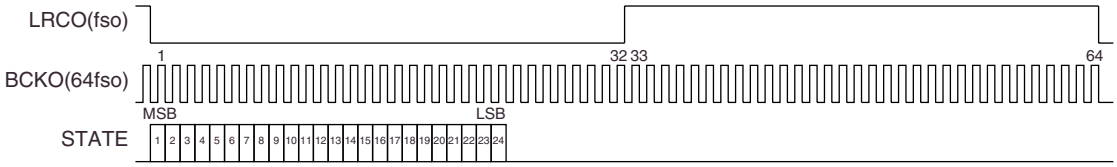
State Data Output Timing

State data output timing

IISN = H

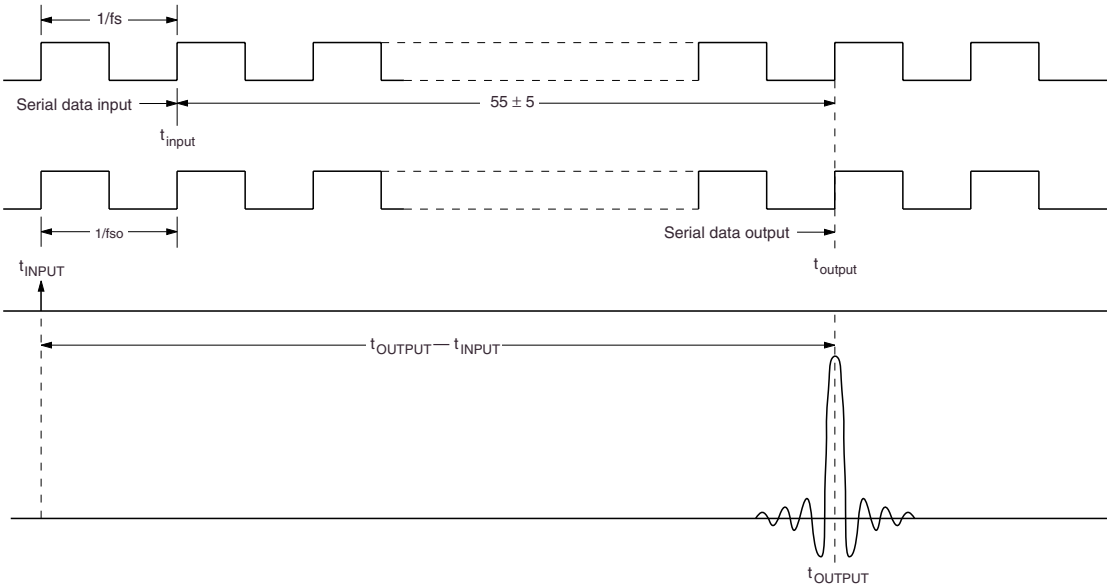


IISN = L



Delay Time

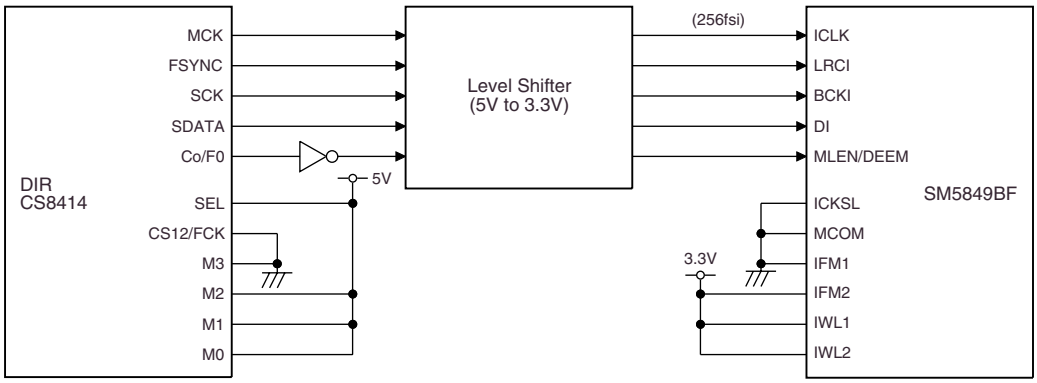
t_{INPUT} is the time when the serial input data read in is completed (on the rising edge of LRCI). t_{OUTPUT} is the time when the serial output data read out is completed (on the rising edge of LRCO). The delay between input and output is given by $t_{OUTPUT} - t_{INPUT} = (55 \pm 5)/fsi$.



TYPICAL APPLICATIONS

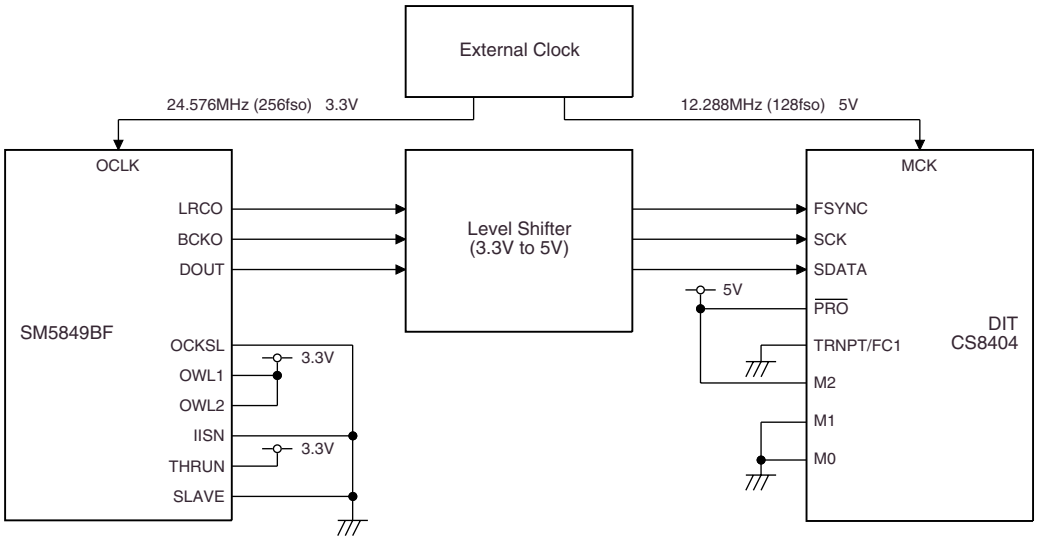
Input Interface Circuit

Digital audio interface receiver (CS8414)



Output Interface Circuit

Digital audio interface receiver (CS8404)



APPLICATION NOTE

Delay in the slave mode

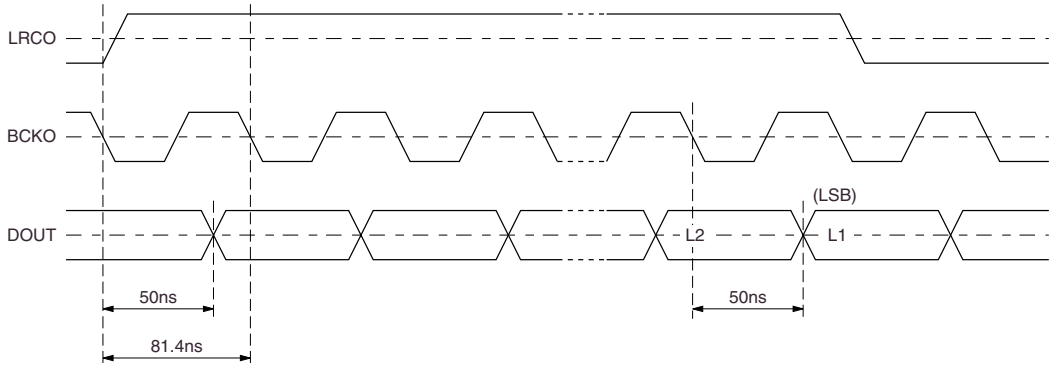
In the slave mode , the delay (tBDH2, tBDL2) of DUOT from BCKO is MIN = 0ns, MAX = 50ns which is rather wide width.

As specified in AC Electrical Characteristics, and BCKO is prohibited from inputting longer than 64fso.

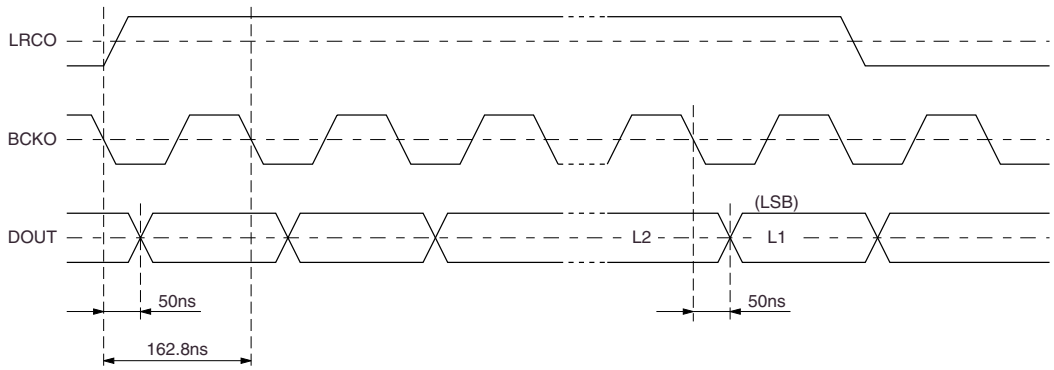
When tBDH2, tBDL2 is maximum 50ns, ideal timing may not be attained for the following devise, depending on the OCLK cycle (example 1).

Please use considering the timing in the following examples in the slave mode.

(example 1) OCLK = 20.3ns (fs = 192kHz), OCKSL = L (256fs), BCKO (64fso) = 81.4ns, IISN = H, OWL1 = L, OWL2 = H



(example 2) OCLK = 27.1ns (fs = 96kHz), OCKSL = H (384fs), BCKO (64fso) = 162.8ns, IISN = H, OWL1 = L, OWL2 = H



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