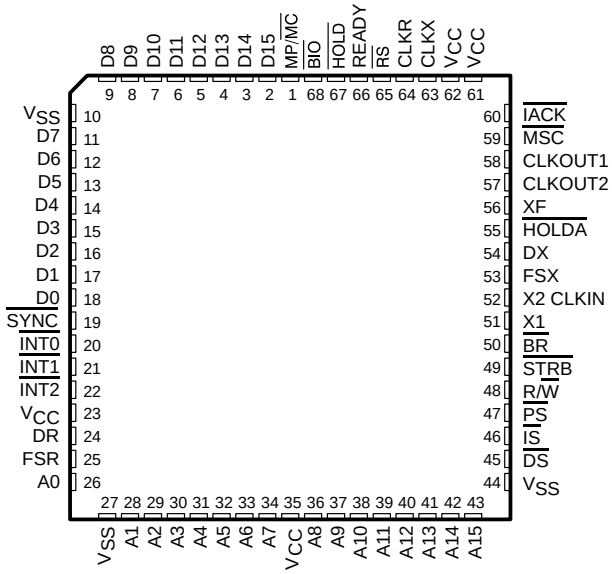
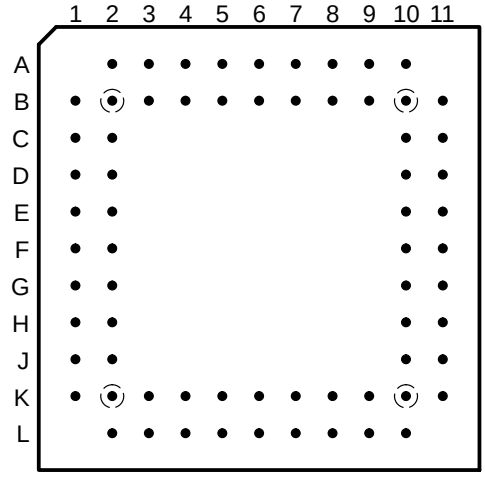
SGUS007D – AUGUST 1988 – REVISED OCTOBER 2001

- **Military Temperature Range**
  - **–55°C to 125°C**
- **100-ns or 80-ns Instruction Cycle Times**
- **544 Words of Programmable On-Chip Data RAM**
- **4K Words of On-Chip Program ROM**
- **128K Words of Data/Program Space**
- **16 Input and 16 Output Channels**
- **16-Bit Parallel Interface**
- **Directly Accessible External Data Memory Space**
  - **Global Data Memory Interface**
- **16-Bit Instruction and Data Words**
- **16 × 16-Bit Multiplier With a 32-Bit Product**
- **32-Bit ALU and Accumulator**
- **Single-Cycle Multiply/Accumulate Instructions**
- **0 to 16-Bit Scaling Shifter**
- **Bit Manipulation and Logical Instructions**
- **Instruction Set Support for Floating-Point Operations, Adaptive Filtering, and Extended-Precision Arithmetic**
- **Block Moves for Data/Program Management**
- **Repeat Instructions for Efficient Use of Program Space**
- **Eight Auxiliary Registers and Dedicated Arithmetic Unit for Indirect Addressing**
- **Serial Port for Direct Code Interface**
- **Synchronization Input for Synchronous Multiprocessor Configurations**
- **Wait States for Communication to Slow-Off-Chip Memories/Peripherals**
- **On-Chip Timer for Control Operations**
- **Three External Maskable User Interrupts**
- **Input Pin Polled by Software Branch Instruction**
- **1.6-μm CMOS Technology**
- **Programmable Output Pin for Signaling External Devices**
- **Single 5-V Supply**
- **On-Chip Clock Generator**
- **Packaging:**
  - **68-Pin Leaded Ceramic Chip Carrier (FJ Suffix)**
  - **68-Pin Ceramic Grid Array (GB Suffix)**
  - **68-Pin Leadless Ceramic Chip Carrier (FD Suffix)**

68-Pin FJ and FD Packages
(Top View)



68-Pin GB Package
(Top View)



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description

This data sheet provides design documentation for the SMJ320C25 and the SMJ320C25-50 digital signal processor (DSP) devices in the SMJ320™ family of VLSI digital signal processors and peripherals. The SMJ320 family supports a wide range of digital signal processing applications such as tactical communications, guidance, military modems, speech processing, spectrum analysis, audio processing, digital filtering, high-speed control, graphics, and other computation-intensive applications.

Differences between the SMJ320C25 and the SMJ320C25-50 are specifically identified, as in the following paragraph and in the parameter tables on pages 18 through 24 of this data sheet. When not specifically differentiated, the term SMJ320C25 is used to describe both devices.

The SMJ320C25 has a 100-ns instruction cycle time. The SMJ320C25-50 has an 80-ns instruction cycle time. With these fast instruction cycle times and their innovative memory configurations, these devices perform operations necessary for many real-time digital signal processing algorithms. Since most instructions require only one cycle, the SMJ320C25 is capable of executing 12.5 million instructions per second. On-chip data RAM of 544 16-bit words, on-chip program ROM of 4K words, direct addressing of up to 64K words of external data memory space and 64K words of external program memory space, and multiprocessor interface features for sharing global memory minimize unnecessary data transfers to take full advantage of the capabilities of the instruction set.

Table 1. PGA/CLCC/LCCC Pin Assignments

FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN
A0	K1/26	A12	K8/40	D2	E1/16	D14	A5/3	INT2	H1/22	V_{CC}	H2/23
A1	K2/28	A13	L9/41	D3	D2/15	D15	B6/2	$\overline{IS}$	J11/46	V_{CC}	L6/35
A2	L3/29	A14	K9/42	D4	D1/14	DR	J1/24	MP/$\overline{MC}$	A6/1	V_{SS}	B1/10
A3	K3/30	A15	L10/43	D5	C2/13	DS	K10/45	$\overline{MSC}$	C10/59	V_{SS}	K11/44
A4	L4/31	$\overline{BI0}$	B7/68	D6	C1/12	DX	E11/54	$\overline{PS}$	J10/47	V_{SS}	L2/27
A5	K4/32	$\overline{BR}$	G11/50	D7	B2/11	FSR	J2/25	READY	B8/66	XF	D11/56
A6	L5/33	CLKOUT1	C11/58	D8	A2/9	FSX	F10/53	$\overline{RS}$	A8/65	X1	G10/51
A7	K5/34	CLKOUT2	D10/57	D9	B3/8	$\overline{HOLD}$	A7/67	R/$\overline{W}$	H11/48	X2/CLKIN	F11/52
A8	K6/36	CLKR	B9/64	D10	A3/7	$\overline{HOLDA}$	E10/55	$\overline{STRB}$	H10/49		
A9	L7/37	CLKX	A9/63	D11	B4/6	$\overline{IACK}$	B11/60	$\overline{SYNC}$	F2/19		
A10	K7/38	D0	F1/18	D12	A4/5	$\overline{INT0}$	G1/20	V_{CC}	A10/61		
A11	L8/39	D1	E2/17	D13	85/4	$\overline{INT1}$	G2/21	V_{CC}	B10/62		

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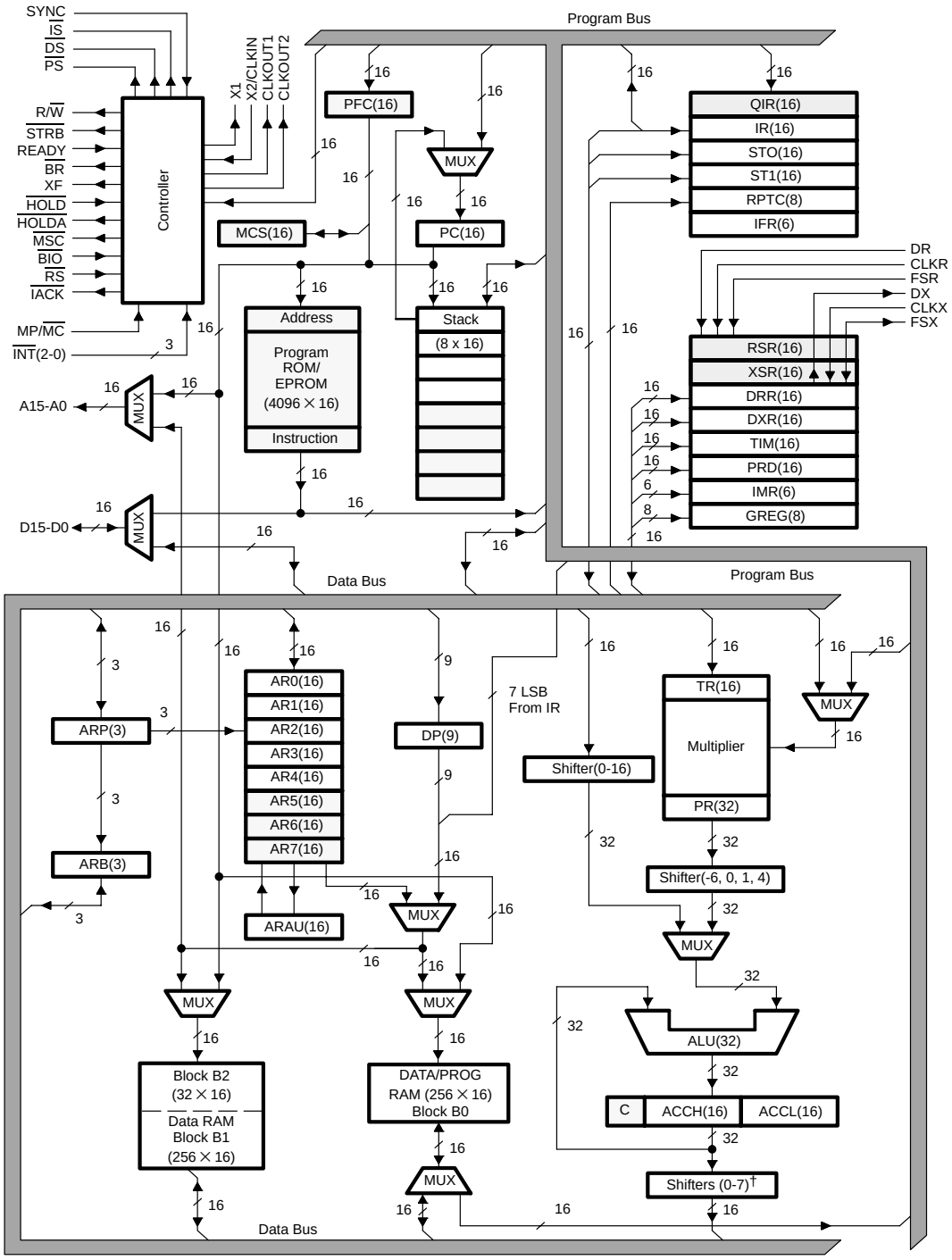
Terminal Functions

SIGNALS	I/O/Z†	DEFINITION
V_{CC}	I	5-V supply pins
V_{SS}	I	Ground pins
X1	0	Output from internal oscillator for crystal
X2/CLKIN	I	Input to internal oscillator from crystal or external clock
CLKOUT1	0	Master clock output (crystal or CLKIN frequency/4)
CLKOUT2	0	A second clock output signal
D15–D0	I/O/Z	16-bit data bus D15 (MSB) through D0 (LSB). Multiplexed between program, data, and I/0 spaces.
A15–A0	O/Z	16-bit address bus A15 (MSB) through A0 (LSB)
$\overline{PS}$,$\overline{DS}$,$\overline{IS}$	O/Z	Program, data, and I/O space select signals
R/$\overline{W}$	O/Z	Read / write signal
$\overline{STRB}$	O/Z	Strobe signal
$\overline{RS}$	I	Reset input
$\overline{INT2}$–$\overline{INT0}$	I	External user interrupt inputs
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select pin
$\overline{MSC}$	0	Microstate complete signal
$\overline{IACK}$	0	Interrupt acknowledge signal
READY	I	Data ready input. Asserted by external logic when using slower devices to indicate that the current bus transaction is complete.
$\overline{BR}$	0	Bus request signal. Asserted when the SMJ320C25 requires access to an external global data memory space.
XF	0	External flag output (latched software-programmable signal)
$\overline{HOLD}$	1	Hold input. When asserted, SMJ320C25 goes into an idle mode and places the data, address, and control lines in the high-impedance state.
$\overline{HOLDA}$	0	Hold acknowledge signal
$\overline{SYNC}$	I	Synchronization input
$\overline{BIO}$	I	Branch control input. Polled by BIOZ instruction
DR	I	Serial data receive input
CLKR	I	Clock for receive input for serial port
FSR	I	Frame synchronization pulse for receive input
DX	O/Z	Serial data transmit output
CLKX	I	Clock for transmit output for serial port
FSX	I/O/Z	Frame synchronization pulse for transmit. Configurable as either an input or an output.

† I/O/Z denotes input/output/high-impedance state.

block diagram



LEGEND:

ACCH	=	Accumulator high	IFR	=	Interrupt flag register	PC	=	Program counter
ACCL	=	Accumulator low	IMR	=	Interrupt mask register	PFC	=	Prefetch counter
ALU	=	Arithmetic logic unit	IR	=	Instruction register	RPTC	=	Repeat instruction counter
ARAU	=	Auxiliary register arithmetic unit	MCS	=	Microcall stack	GREG	=	Global memory allocation register
ARB	=	Auxiliary register pointer buffer	QIR	=	Queue instruction register	RSR	=	Serial port receive shift register
ARP	=	Auxiliary register pointer	PR	=	Product register	XSR	=	Serial port transmit shift register
DP	=	Data memory page pointer	PRD	=	Period register for timer	AR0-AR7	=	Auxiliary registers
DRR	=	Serial port data receive register	TIM	=	Timer	ST0, ST1	=	Status registers
DXR	=	Serial port data transmit register	TR	=	Temporary register	C	=	Carry bit

architecture

The SMJ320C25 increases performance of DSP algorithms through innovative additions to the SMJ320 architecture. Increased throughput on the SMJ320C25 for many DSP applications is accomplished by means of single-cycle multiply/accumulate instructions with a data move option, eight auxiliary registers with a dedicated arithmetic unit, and faster I/O necessary for data-intensive signal processing.

The architectural design of the SMJ320C25 emphasizes overall speed, communication, and flexibility in processor configuration. Control signals and instructions provide floating-point support, block-memory transfers, communication to slower off-chip devices, and multiprocessing implementations.

Two large on-chip RAM blocks, configurable either as separate program and data spaces or as two contiguous data blocks, provide increased flexibility in system design. Programs of up to 4K words can be masked into the internal program ROM. The remainder of the 64K-word program memory space is located externally. Large programs can execute at full speed from this memory space. Programs can also be downloaded from slow external memory to high-speed on-chip RAM. A total of 64K data memory address space is included to facilitate implementation of DSP algorithms. The VLSI implementation of the SMJ320C25 incorporates all of these features as well as many others, such as a hardware timer, serial port, and block data transfer capabilities.

32-bit ALU/accumulator

The SMJ320C25 32-bit arithmetic logic unit (ALU) and accumulator perform a wide range of arithmetic and logical instructions, the majority of which execute in a single clock cycle. The ALU executes a variety of branch instructions dependent on the status of the ALU or a single bit in a word. These instruction provide the following capabilities:

- Branch to an address specified by the accumulator
- Normalize fixed-point numbers contained in the accumulator
- Test a specified bit of a word in data memory.

One input to the ALU is always provided from the accumulator, and the other input can be provided from the product register (PA) of the multiplier or the input scaling shifter which has fetched data from the RAM on the data bus. After the ALU has performed the arithmetic or logical operations, the result is stored in the accumulator.

The 32-bit accumulator is split into two 16-bit segments for storage in data memory. Additional shifters at the output of the accumulator perform shifts while the data is being transferred to the data bus for storage. The contents of the accumulator remain unchanged.

scaling shifter

The SMJ320C25 scaling shifter has a 16-bit input connected to the data bus and a 32-bit output connected to the ALU. The scaling shifter produces a left shift of 0 to 16 bits on the input data, as programmed in the instruction. The LSBs of the output are filled with zeroes, and the MSBs can be either filled with zeroes or sign-extended, depending upon the status programmed into the SXM (sign-extension mode) bit of status register ST1.

16 X 16-bit parallel multiplier

The SMJ320C25 has a 16 x 16-bit hardware multiplier, which is capable of computing a signed or unsigned 32-bit product in a single machine cycle. The multiplier has the following two associated registers:

- A 16-bit temporary register (TR) that holds one of the operands for the multiplier, and
- A 32-bit product register (PR) that holds the product.

Incorporated into the SMJ320C25 instruction set are single-cycle multiply/accumulate instruction that allow both operands to be processed simultaneously. The data for these operations can reside anywhere in internal or external memory and can be transferred to the multiplier each cycle via the program and data buses.

16 X 16-bit parallel multiplier (continued)

Four product shift modes are available at the product register (PR) output that are useful when performing multiply/accumulate operations, fractional arithmetic, or justifying fractional products.

timer

The SMJ320C25 provides a memory-mapped 16-bit timer for control operations. The on-chip timer (TIM) register is a down counter that is continuously clocked by CLKOUT1. A timer interrupt (TINT) is generated every time the timer decrements to zero. The timer is reloaded with the value contained in the period (PRD) register within the next cycle after it reaches zero so that interrupts can be programmed to occur at regular intervals of PRD + 1 cycles of CLKOUT1.

memory control

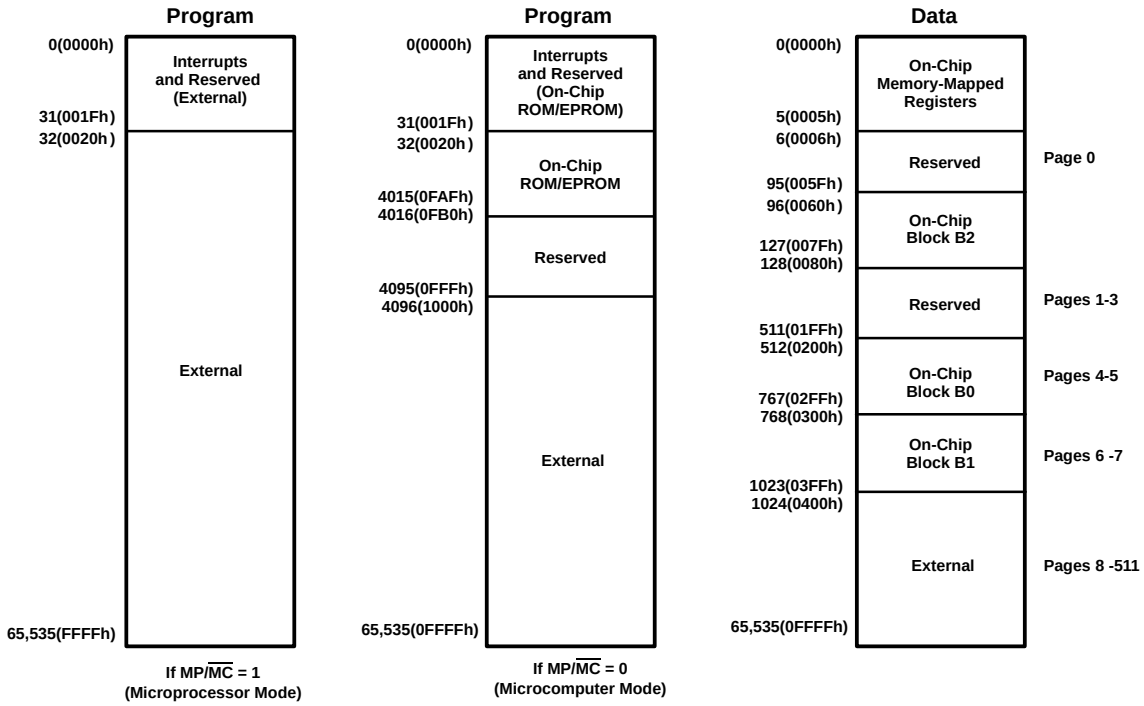
The SMJ320C25 provides a total of 544 16-bit words of on-chip data RAM, divided into three separate blocks (B0, B1, and B2). Of the 544 words, 288 words (blocks B1 and B2) are always data memory, and 256 words (block B0) are programmable as either data or program memory. A data memory size of 544 words allows the SMJ320C25 to handle a data array of 512 words (256 words if on-chip RAM is used for program memory), while still leaving 32 locations for intermediate storage. When using block B0 as program memory, instructions can be downloaded from external program memory into on-chip RAM and then executed.

When using on-chip program RAM, ROM, or high-speed external program memory, the SMJ320C25 runs at full speed without wait states. However, the READY line can be used to interface the SMJ320C25 to slower, less-expensive external memory. Downloading programs from slow off-chip memory to on-chip program RAM speeds processing while cutting system costs.

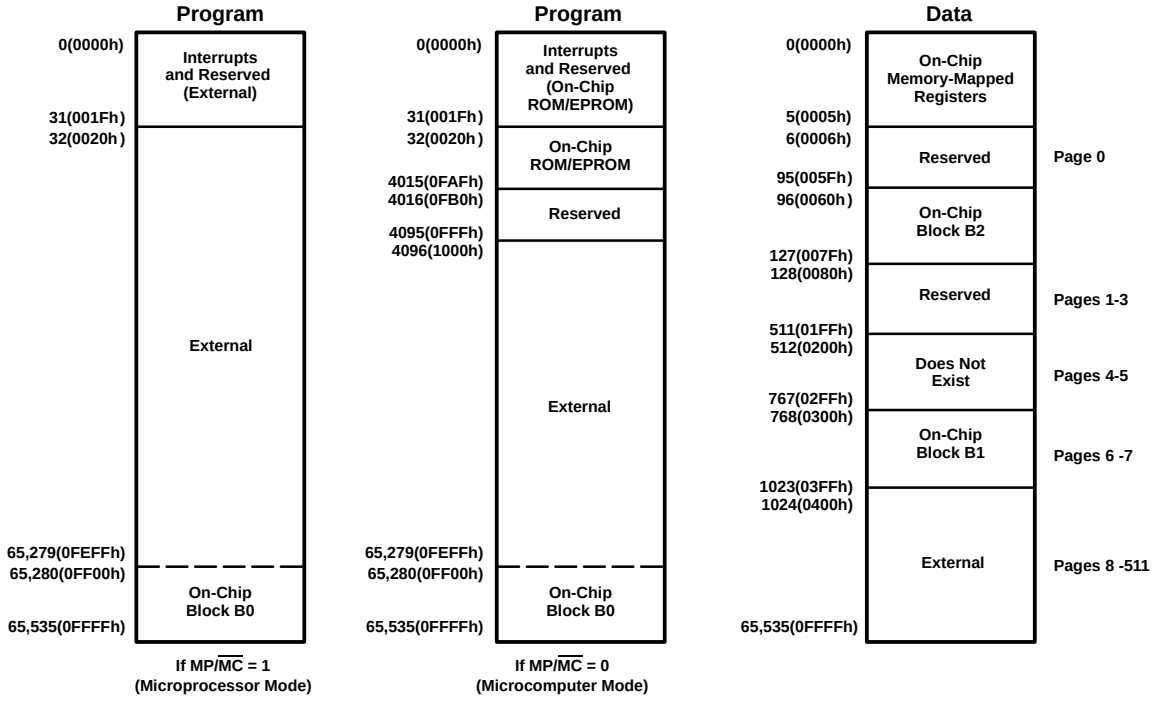
The SMJ320C25 provides three separate address states for program memory, data memory, and I/O. The on-chip memory is mapped into either the 64K-word data memory or program memory space, depending upon the memory configuration. The CNF0 (configure block B0 as data memory) and CNFP (configure block B0 as program memory) instruction allow dynamic configuration of the memory maps through software. Regardless of the configuration, the user can still execute from external program memory.

The SMJ320C25 has six registers which are mapped into the data memory space: a serial port data receive register, serial port data transmit register, timer register, period register, interrupt mask register, and global memory allocation register.

memory control (continued)



(a) Memory Maps After a CNFD Instruction



(b) Memory Maps After a CNFP Instruction

Figure 1. Memory Maps

interrupts and subroutines

The SMJ320C25 has three external maskable user interrupts $\overline{\text{INT2}}$–$\overline{\text{INT0}}$, available for external devices that interrupt the processor. Internal interrupts are generated by the serial port (RINT and XINT), by the timer (TINT), and by the software interrupt (TRAP) instruction. Interrupts are prioritized with reset (RS) having the highest priority and the serial port transmit interrupt (XINT) having the lowest priority. All interrupt locations are on two-word boundaries so that branch instruction can be accommodated in those locations if desired.

A built-in mechanism protects multicycle instructions from interrupts. If an interrupt occurs during a multicycle instruction, the interrupt is not processed until the instruction is completed. This mechanism applies both to instructions that are repeated or become multicycle due to the READY signal.

external interface

The SMJ320C25 supports a wide range of system interfacing requirements. Program, data, and I/O address spaces provide interface to memory and I/O. thus maximizing system throughout. I/O design is simplified by having I/O treated the same way as memory. I/O devices are mapped into the I/O address space using the processor's external address and data buses in the same manner as memory-mapped devices. Interface to memory and I/O devices of varying speeds is accomplished by using the READY line. When transitions are made with slower devices, the SMJ320C25 processor waits until the other device completes its function and signals the processor via the READY line. Then, the SMJ320C25 continues execution.

A full-duplex serial port provides communication with serial devices, such as codecs, serial A/D converters, and other serial systems. The interface signals are compatible with codecs and many other serial devices with a minimum of external hardware. The serial port can also be used for intercommunication between processors in multiprocessing applications.

The serial port has two memory-mapped registers: the data transmit register (DXR) and the data receive register (DRR). Both registers operate in either the byte mode or 16-bit word mode, any can be accessed in the same manner as any other data *memory* location. Each register has an external clock, a framing synchronization pulse, and associated shift registers. One method of multiprocessing can be implemented by programming one device to transmit while the others are in the receive mode.

multiprocessing

The flexibility of the SMJ320C25 allows configurations to satisfy a wide range of system requirements. The SMJ320C25 can be used as follows:

- A standalone processor
- A multiprocessor with devices in parallel
- A slave/host multiprocessor with global memory space
- A peripheral processor interfaced via processor-controlled signals to another device.

For multiprocessing applications, the SMJ320C25 has the capability of allocating global data memory space and communicating with that space via the $\overline{\text{BR}}$ (bus request) and READY control signals. Global memory is data memory shared by more than one processor. Global data memory access must be arbitrated. The 8-bit memory-mapped GREG (global memory allocation register) specifies part of the SMJ320C25s data memory as global external memory. The contents of the register determine the size of the global memory space. If the current instruction addresses an operand within that space, $\overline{\text{BR}}$ is asserted to request control of the bus. The length of the memory cycle is controlled by the READY line.

The SMJ320C25 supports DMA (direct memory access) to its external program/data memory using the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals. Another processor can take complete control of the SMJ320C25s external memory by asserting $\overline{\text{HOLD}}$ low. This causes the SMJ320C25 to place its address, data, and control lines in a high-impedance state, and assert $\overline{\text{HOLDA}}$. Program execution from on-chip memory can proceed concurrently while the device is in the hold mode.

instruction set

The SMJ320C25 microprocessor implements a comprehensive instruction set that supports both numeric-intensive signal processing operations as well as general-purpose applications, such as multiprocessing and high-speed control.

For maximum throughput, the next instruction is prefetched while the current one is being executed. Since the same data lines are used to communicate to external data/program or I/O space, the number of cycles may vary depending upon whether the next data operand fetch is from internal or external program memory. Highest throughput is achieved by maintaining data memory on-chip and using either internal or fast external program memory.

addressing modes

The SMJ320C25 instruction set provides three memory addressing modes: direct, indirect, and immediate addressing.

Both direct and indirect addressing can be used to access data memory. In direct addressing, seven bits of the instruction word are concatenated with the nine bits of the data memory page pointer to form the 16-bit data memory address. Indirect addressing accesses data memory through the eight auxiliary registers. In immediate addressing, the data is based on a portion of the instruction word(s).

In direct memory addressing, the instruction word contains the lower seven bits of the data memory address. This field is concatenated with the nine bits of the data memory page pointer to form the full 16-bit address. Thus, memory is paged in the direct addressing mode with a total of 512 pages, each page containing 128 words.

Eight auxiliary register (AR0–AR7) provide flexible and powerful indirect addressing. To select a specific auxiliary register, the Auxiliary Register Pointer (ARP) is loaded with a value from 0 through 7 for AR0–AR7, respectively.

There are seven types of indirect addressing: auto-increment or auto-decrement, post-indexing by either adding or subtracting the contents of AR0, or single indirect addressing with no increment or decrement and bit-reversal addressing (used in FFTs) with increment or decrement. All operations are performed on the current auxiliary register in the same cycle as the original instruction, followed by anew ARP value being loaded.

repeat feature

A repeat feature, used with instructions such as multiply/accumulates, block moves, I/O transfers, and table read/writes, allows a single instruction to be performed up to 256 times. The repeat counter (RPTC) is loaded with either a data memory value (RPT instruction) or an immediate value (RPTK instruction) .The value of this operand is one less than the number of times that the next instruction is executed. Those instructions that are normally multicycle are pipelined when using the repeat feature, and effectively become single-cycle instructions.

instruction set summary

Table 1 lists the symbols and abbreviations used in Table 1, the instruction set summary, Table 2 consists primarily of single-cycle,single-word instructions. Infrequently used branch, I/O, and CALL instructions are multicycle. The instruction set summary is arranged according to function and alphabetized within each functional grouping.

instruction set summary (continued)

Table 1. Instruction Symbols

SYMBOL	MEANING
B	4-bit field specifying a bit code
CM	2-bit field specifying compare mode
D	Data memory address field
F0	Format status bit
M	Addressing mode bit
K	Immediate operand field
PA	Port address (PA0–PA15 are predefined assembler symbols equal to 0 through 15, respectively)
PM	2-bit field specifying P register output shift code
R	3-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

Table 2. SMJ320C25 Instruction Set Summary

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS	Absolute value of accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	1	1
ADD	Add to accumulator with shift	1	0	0	0	0	←	S	→		M	←			D			→
ADDC‡	Add to accumulator with carry	1	0	1	0	0	0	0	1	1	M	←			D			→
ADDH	Add to high accumulator	1	0	1	0	0	1	0	0	0	M	←			D			→
ADDK‡	Add to accumulator short immediate	1	1	1	0	0	1	1	0	0	←				K			→
ADDS	Add to low accumulator with sign extension suppressed	1	0	1	0	0	1	0	0	1	M	←			D			→
ADDT	Add to accumulator with shift specified by T register	1	0	1	0	0	1	0	1	0	M	←			D			→
ADLK†	Add to accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	1	0
AND	AND with accumulator	1	0	1	0	0	1	1	1	0	M	←			D			→
ANDK†	AND immediate with accumulator with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	1	0	0
CMPL†	Complement accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	1	1
LAC	Load accumulator with shift	1	0	0	1	0	←	S	→		M	←			D			→
LACK	Load accumulator immediate short	1	1	1	0	0	1	0	1	0	←				K			→
LACT†	Load accumulator with shift specified by T register	1	0	1	0	0	0	0	1	0	M	←			D			→
LALK†	Load accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	0	1
NEG†	Negate accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	1	1
NORM†	Normalize contents of accumulator	1	1	1	0	0	1	1	1	0	1	←			D			→
OR	OR with accumulator	1	0	1	0	0	1	1	0	1	M	←			D			→
ORK†	OR immediate with accumulator with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	1	0	1
ROL‡	Rotate accumulator left	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0
ROR‡	Rotate accumulator right	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	0	1
SACH	Store high accumulator with shift	1	0	1	1	0	1	←	X	→	M	←			D			→
SACL	Store low-order accumulator with shift	1	0	1	1	0	0	←	X	→	M	←			D			→
SBLK†	Subtract from accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	1	1
SFL†	Shift accumulator left	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	0
SFR†	Shift accumulator right	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	1
SUB	Subtract from accumulator with shift	1	0	0	0	1	←	S	→		M	←			D			→
SUBB‡	Subtract from accumulator with borrow	1	0	1	0	0	1	1	1	1	M	←			D			→
SUBC	Conditional subtract	1	0	1	0	0	0	1	1	1	M	←			D			→
SUBH	Subtract from high accumulator	1	0	1	0	0	0	1	0	0	M	←			D			→
SUBK‡	Subtract from accumulator short immediate	1	1	1	0	0	1	1	0	1	←				K			→
SUBS	Subtract from low accumulator with sign extension suppressed	1	0	1	0	0	0	1	0	1	M	←			D			→

† These instructions are not included in the TMS320C1x instruction set.
‡ These instructions are not included in the TMS32020 instruction set.

Table 2. SMJ320C25 Instruction Set Summary (continued)

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS																		
MNEMONIC	**DESCRIPTION**	**NO. WORDS**	**INSTRUCTION BIT CODE**															
			15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SUBT†	Subtract from accumulator with shift specified by T register	1	0	1	0	0	0	1	1	0	M	◄	―	―	D	―	―	►
XOR	Exclusive-OR with accumulator	1	0	1	0	0	1	1	0	0	M	◄	―	―	D	―	―	►
XORK†	Exclusive-OR immediate with accumulator with shift	2	1	1	0	1	◄	S	►		0	0	0	0	0	1	1	0
ZAC	Zero accumulator	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
ZALH	Zero low accumulator and load high accumulator	1	0	1	0	0	0	0	0	0	M	◄	―	―	D	―	―	►
ZALR‡	Zero low accumulator and load high accumulator with rounding	1	0	1	1	1	1	0	1	1	M	◄	―	―	D	―	―	►
ZALS	Zero accumulator and load low accumulator with sign extension suppressed	1	0	1	0	0	0	0	0	1	M	◄	―	―	D	―	―	►

AUXILIARY REGISTERS AND DATA PAGE POINTER INSTRUCTIONS																		
MNEMONIC	**DESCRIPTION**	**NO. WORDS**	**INSTRUCTION BIT CODE**															
			15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADRK‡	Add to auxiliary register short immediate	1	0	1	1	1	1	1	1	0	◄	―	―	―	K	―	―	►
CMPR†	Compare auxiliary register with auxiliary register AR0	1	1	1	0	0	1	1	1	0	0	1	0	1	0	0	◄	CM ►
LAR	Load auxiliary register	1	0	0	1	1	0	◄	R	►	M	◄	―	―	D	―	―	►
LARK	Load auxiliary register short immediate	1	1	1	0	0	0	◄	R	►	◄	―	―	―	K	―	―	►
LARP	Load auxiliary register pointer	1	0	1	0	1	0	1	0	1	1	0	0	0	1	◄	R	►
LDP	Load data memory page pointer	1	0	1	0	1	0	0	1	0	M	◄	―	―	D	―	―	►
LDPK	Load data memory page pointer immediate	1	1	1	0	0	1	0	0	◄	―	―	―	―	DP	―	―	►
LRLK†	Load auxiliary register long immediate	2	1	1	0	1	0	◄	R	►	0	0	0	0	0	0	0	0
MAR	Modify auxiliary register	1	0	1	0	1	0	1	0	1	M	◄	―	―	D	―	―	►
SAR	Store auxiliary register	1	0	1	1	1	0	◄	R	►	M	◄	―	―	D	―	―	►
SBRK‡	Subtract from auxiliary register short immediate	1	0	1	1	1	1	1	1	1	◄	―	―	―	K	―	―	►

† These instructions are not included in the TMS320C1x instruction set.
‡ These instructions are not included in the TMS32020 instruction set.

Table 2. SMJ320C25 Instruction Set Summary (continued)

T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS																		
MNEMONIC	**DESCRIPTION**	**NO. WORDS**	**INSTRUCTION BIT CODE**															
			15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
APAC	Add P register to accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	0	1
LPH†	Load high P register	1	0	1	0	1	0	0	1	1	M	◄			D			►
LT	Load T register	1	0	0	1	1	1	1	0	0	M	◄			D			►
LTA	Load T register and accumulate previous product	1	0	0	1	1	1	1	0	1	M	◄			D			►
LTD	Load T register, accumulate previous product, and move data	1	0	0	1	1	1	1	1	1	M	◄			D			►
LTP†	Load T register and store P register in accumulator	1	0	0	1	1	1	1	1	0	M	◄			D			►
LTS†	Load T register and subtract previous product	1	0	1	0	1	1	0	1	1	M	◄			D			►
MAC†	Multiply and accumulate	2	0	1	0	1	1	1	0	1	M	◄			D			►
MACD†	Multiply and accumulate with data move	2	0	1	0	1	1	1	0	0	M	◄			D			►
MPY	Multiply (with T register, store product in P register)	1	0	0	1	1	1	0	0	0	M	◄			D			►
MPYA‡	Multiply and accumulate previous product	1	0	0	1	1	1	0	1	0	M	◄			D			►
MPYK	Multiply immediate	1	1	0	1	◄					K							►
MPYS‡	Multiply and subtract previous product	1	0	0	1	1	1	0	1	1	M	◄			D			►
MPYU‡	Multiply unsigned	1	1	1	0	0	1	1	1	1	M	◄			D			►
PAC	Load accumulator with P register	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	0	0
SPAC	Subtract P register from accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	1	0
SPH‡	Store high P register	1	0	1	1	1	1	1	0	1	M	◄			D			►
SPL‡	Store low P register	1	0	1	1	1	1	1	0	0	M	◄			D			►
SPM†	Set P register output shift mode	1	1	1	0	0	1	1	1	0	0	0	0	0	1	0	◄	PM ►
SQRA†	Square and accumulate	1	0	0	1	1	1	0	0	1	M	◄			D			►
SQRS†	Square and subtract previous product	1	0	1	0	1	1	0	1	0	M	◄			D			►

† These instructions are not included in the TMS320C1x instruction set.
‡ These instructions are not included in the TMS32020 instruction set.

Table 2. SMJ320C25 Instruction Set Summary (continued)

BRANCH/CALL INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	Branch unconditionally	2	1	1	1	1	1	1	1	1	1	←			D			→
BACC†	Branch to address specified by accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	0	1
BANZ	Branch on auxiliary register not zero	2	1	1	1	1	1	0	1	1	1	←			D			→
BBNZ†	Branch if TC bit ≠ 0	2	1	1	1	1	1	0	0	1	1	←			D			→
BBZ†	Branch if TC bit = 0	2	1	1	1	1	1	0	0	0	1	←			D			→
BC‡	Branch on carry	2	0	1	0	1	1	1	1	0	1	←			D			→
BGEZ	Branch if accumulator ≥ 0	2	1	1	1	1	0	1	0	0	1	←			D			→
BGZ	Branch if accumulator > 0	2	1	1	1	1	0	0	0	1	1	←			D			→
BIOZ	Branch on I/O status = 0	2	1	1	1	1	1	0	1	0	1	←			D			→
BLEZ	Branch if accumulator ≤ 0	2	1	1	1	1	0	0	1	0	1	←			D			→
BLZ	Branch if accumulator < 0	2	1	1	1	1	0	0	1	1	1	←			D			→
BNC‡	Branch on no carry	2	0	1	0	1	1	1	1	1	1	←			D			→
BNV†	Branch if no overflow	2	1	1	1	1	0	1	1	1	1	←			D			→
BNZ	Branch if accumulator ≠ 0	2	1	1	1	1	0	1	0	1	1	←			D			→
BV	Branch on overflow	2	1	1	1	1	0	0	0	0	1	←			D			→
BZ	Branch if accumulator = 0	2	1	1	1	1	0	1	1	0	1	←			D			→
CALA	Call subroutine indirect	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	0	0
CALL	Call subroutine	2	1	1	1	1	1	1	1	0	1	←			D			→
RET	Return from subroutine	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	1	0
I/O AND DATA MEMORY OPERATIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLKD†	Block move from data memory to data memory	2	1	1	1	0	1	1	0	1	M	←			D			→
BLKP†	Block move from program memory to data memory	2	1	1	1	1	1	1	0	0	M	←			D			→
DMOV	Data move in data memory	1	0	1	0	1	0	1	1	0	M	←			D			→
FORT†	Format serial port registers	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	1	FO
IN	Input data from port	1	1	0	0	0	←	PA	→		M	←			D			→
OUT	Output data to port	1	1	1	1	0	←	PA	→		M	←			D			→
RFSM‡	Reset serial port frame synchronization mode	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	0
RTXM†	Reset serial port transmit mode	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0
RXF†	Reset external flag	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	0
SFSM‡	Set serial port frame synchronization mode	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	1
STXM†	Set serial port transmit mode	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	1
SXF†	Set external flag	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1
TBLR	Table read	1	0	1	0	1	1	0	0	0	M	←			D			→
TBLW	Table write	1	0	1	0	1	1	0	0	1	M	←			D			→

† These instructions are not included in the TMS320C1x instruction set.
‡ These instructions are not included in the TMS32020 instruction set.

Table 2. SMJ320C25 Instruction Set Summary (concluded)

CONTROL INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT†	Test bit	1	1	0	0	1	←	B		→	M	←			D			→
BITT†	Test bit specified by T register	1	0	1	0	1	0	1	1	1	M	←			D			→
CNFD†	Configure block as data memory	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	0	0
CNFP†	Configure block as program memory	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	0	1
DINT	Disable interrupt	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
IDLE†	Idle until interrupt	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	1
LST	Load status register STO	1	0	1	0	1	0	0	0	0	M	←			D			→
LST1†	Load status register ST1	1	0	1	0	1	0	0	0	1	M	←			D			→
NOP	No operation	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
POP	Pop top of stack to low accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	1
POPD†	Pop top of stack to data memory	1	0	1	1	1	1	0	1	0	M	←			D			→
PSHD†	Push data memory value onto stack	1	0	1	0	1	0	1	0	0	M	←			D			→
PUSH	Push low accumulator onto stack	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	0
RC‡	Reset carry bit	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	0	0
RHM‡	Reset hold mode	1	1	1	0	0	1	1	1	0	0	0	1	1	1	0	0	0
ROVM	Reset overflow mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	0
RPT†	Repeat instruction as specified by data memory value	1	0	1	0	0	1	0	1	1	M	←			D			→
RPTK†	Repeat instruction as specified by immediate value	1	1	1	0	0	1	0	1	1	←			K				→
RSXM†	Reset sign-extension mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	0
RTC‡	Reset test/control flag	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	0
SC‡	Set carry bit	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	0	1
SHM‡	Set hold mode	1	1	1	0	0	1	1	1	0	0	0	1	1	1	0	0	1
SOVM	Set overflow mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	1
SST	Store status register ST0	1	0	1	1	1	1	0	0	0	M	←			D			→
SST1†	Store status register ST1	1	0	1	1	1	1	0	0	1	M	←			D			→
SSXM†	Set sign-extension mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	1
STC‡	Set test/control flag	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	1
TRAP†	Software interrupt	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0

† These instructions are not included in the TMS320C1x instruction set.
‡ These instructions are not included in the TMS32020 instruction set.

development systems and software support

Texas Instruments offers concentrated development support and complete documentation for designing an SMJ320C25-based microprocessor system. When developing an application, tools are provided to evaluate the performance of the processor, to develop the algorithm implementation, and to fully integrate the design's software and hardware modules. When questions arise, additional support can be obtained by calling the nearest Texas Instruments Regional Technology Center (RTC).

Sophisticated development operations are performed with the SMJ320C25 Macro Assembler/linker, Simulator, and Emulator (XDS). The macro assembler and linker are used to translate program modules into object code and link them together. This puts the program modules into a form which can be loaded into the SMJ320C25 Simulator or Emulator. The simulator provides a quick means for initially debugging SMJ320C25 software while the emulator provides the real-time in-circuit emulation necessary to perform system level debug efficiently.

Table 3 gives a complete list of SMJ320C25 software and hardware development tools.

Table 3. SMJ/SMJ320C25 Software and Hardware Support

MACRO ASSEMBLERS/LINKERS		
Host Computer	Operating System	Part Number
DECVAX	VMS	TMDS324210-08
TI/IBM PC	MS/PC-DOS	TMDS3242810-02
SIMULATORS		
Host Computer	Operating System	Part Number
DECVAX	VMS	TMDS3242211-08
TI/IBM PC	MS/PC-DOS	TMDS3242811-02
EMULATORS		
Model	Power Supply	Part Number
XDS/22	Included	TMDS3262221

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . –0.3 V to 7 V
Input voltage range . . . . . –0.3 V to 7 V
Output voltage range . . . . . –0.3 V to 7 V
Continuous power dissipation . . . . . 1.0 W
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

† All voltage values are with respect to V_{SS}.

recommended operating conditions‡

			SMJ320C25-50			SMJ320C25			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{SS}	Supply voltage			0			0		V
V_{IH}	High-level input voltage	READY	3.00			2.35			V
		D15–D0	2.20			2.20			
		FSX	2.20			2.30			
		CLKR, CLKX	3.50			3.50			
		CLKIN	4.00			3.50			
		All others	3.00			3.00			
V_{IL}	Low-level input voltage	D15–D0, FSX, CLKIN, CLKR, CLKX			0.80			0.80	V
		HOLD			0.70			0.70	
		All others			0.80			0.70	
I_{OH}	High-level output current				300			300	μA
I_{OL}	Low-level output current				2			2	mA
T_C	Operating case temperature		–55		125	–55		125	°C

‡ T_C MAX at maximum rated operating conditions at any point on case T_C MIN at initial (time zero) power up

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

electrical characteristics over specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SMJ320C25, SMJ320C25-50			UNIT
				MIN	TYP§	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	24	3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX		0.3	0.6	V
I_Z	Three-state current		V_{CC} = MAX	–20		20	μA
I_I	Input current	X2/CLKIN	V_I = V_{SS} to V_{CC}	–20		20	μA
		All other pins		–10		10	
I_{CC}	Supply current	Normal	V_{CC} = MAX, f_x = MAX			185	mA
		Idle/R5L5				100	
C_i	Input capacitance				15		pF
C_o	Output capacitance				15		pF

§ All typical values are at V_{CC} = 5 V, T_A = 25°C

CLOCK CHARACTERISTICS AND TIMING

The SMJ320C25 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 2). The frequency of CLKOUT1 is one-fourth the crystal fundamental frequency. The crystal should be either fundamental or overtone mode, and parallel resonant, with an effective series resistance of 30 Ω, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF. Note that overtone of crystals require an additional tuned LC circuit (see the application report, *Hardware Interfacing to the TMS320C25*).

PARAMETER		TEST CONDITIONS	SMJ320C25-50			SMJ320C25			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_x	Input clock frequency	T_A = – 55°C MIN	6.7†		50.0	6.7†		40.0	MHz
C1, C2		T_C = 125°C MAX		10			10		pF

† These values are derived from characterization data and are not tested.

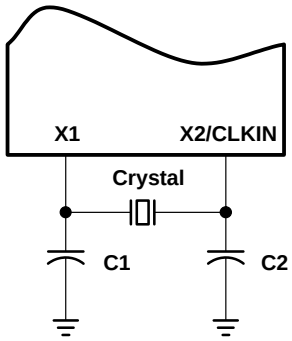


Figure 2. Internal Clock Options

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the following table.

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		SMJ320C25-50		SMJ320C25			UNIT
		MIN	MAX	MIN	NOM	MAX	
$t_{c(C)}$	Cycle time, CLKOUT1/CLKOUT2	80	600	100		600	ns
$t_{d(CIH–C)}$	Delay time, CLKIN high to CLKOUT1/CLKOUT2/STRB high/low	5	28	5		30	(1S
$t_{d(C1–C2)}$	Delay time, CLKOUT1 high to CLKOUT2 low, Delay time, CLKOUT2 high to CLKOUT1 high, etc.	Q – 6	Q + 3	Q – 6	Q	Q + 6	ns
$t_{f(C)}$	Fall time, CLKOUT1/CLKOUT2/STRB		5			5	ns
$t_{r(C)}$	Rise time, CLKOUT1/CLKOUT2/STRB		3			5	ns
$t_{w(CL)}$	Pulse duration, CLKOUT1/CLKOUT2 low	2Q – 7	2Q + 5	2Q – 8	2Q	2Q + 8	ns
$t_{w(CH)}$	Pulse duration, CLKOUT1/CLKOUT2 high	2Q – 5	2Q + 7	2Q – 8	2Q	2Q + 8	ns

† .This parameter is not production tested

NOTE 1: $Q = 1/4t_{c(C)}$

timing requirements over recommended operating conditions (see Note 1)

		SMJ320C25-50		SMJ320C25		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(CI)}$	Cycle time, CLKIN	20	150	25	150	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low, $t_{c(CI)}$ = 25 ns (see Note 2)	8		10	15	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high, $t_{c(CI)}$ = 25 ns (see Note 2)	8		10	15	ns
$t_{su(S)}$	Setup time, SYNC before CLKIN low	4	Q – 4	5	Q – 5	ns
$t_{h(S)}$	Hold time, SYNC from CLKIN low	4		8		ns

NOTES: 1: $Q = 1/4t_{c(C)}$

2. Rise and fall times, assuming a 40–60% duty cycle, are incorporated within this specification CLKIN rise and fall times must be less than 5 ns

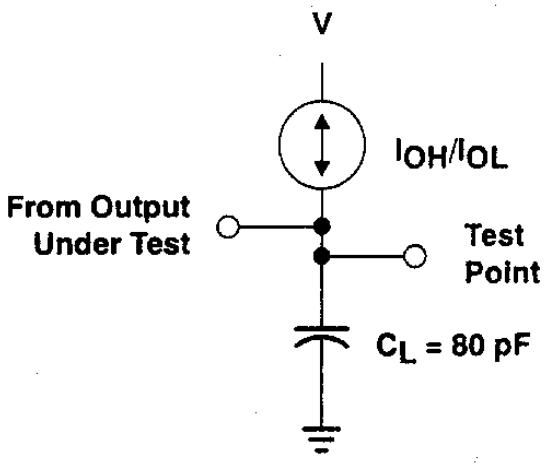
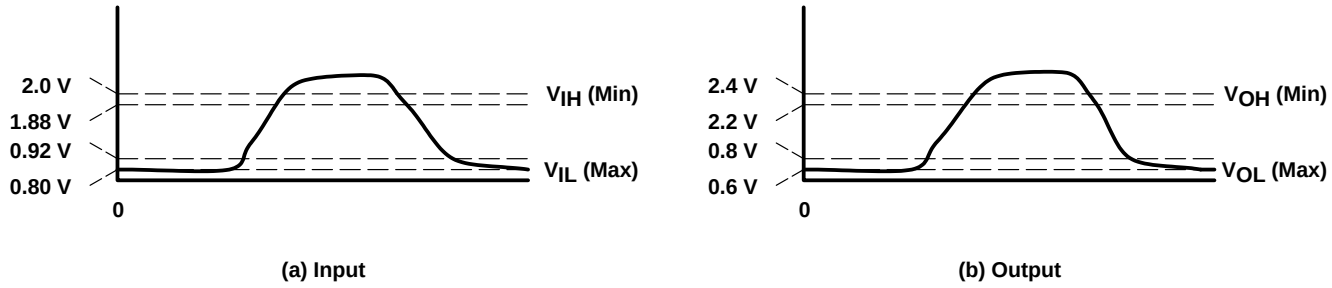


Figure 3. Test Load Circuit



(a) Input (b) Output

Figure 4. Voltage Reference Levels

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		SMJ320C25-50		SMJ320C25			UNIT
		MIN	MAX	MIN	TYP	MAX	
$t_{d(C1–S)}$	$\overline{STRB}$ from CLKOUT1 (if $\overline{STRB}$ is present)	Q – 5	Q + 3	Q – 6	Q	Q + 6	ns
$t_{d(C2–S)}$	CLKOUT2 to $\overline{STRB}$ (if $\overline{STRB}$ is present)	–2	5	–6	0	6	ns
$t_{su(A)}$	Address setup time before $\overline{STRB}$ low (see Note 3)	Q – 13		Q – 12			ns
$t_{h(A)}$	Address hold time after $\overline{STRB}$ high (see Note 3)	Q – 4		Q – 8			ns
$t_{w(SL)}$	$\overline{STRB}$ low pulse duration (no wait states, see Note 4)	2Q – 5	2Q + 5	2Q – 5	2Q	2Q + 5	ns
$t_{w(SH)}$	$\overline{STRB}$ high pulse duration (between consecutive cycles, see Note 4)	2Q – 5	2Q + 5	2Q – 5		2Q + 5	ns
$t_{su(D)W}$	Data write setup time before $\overline{STRB}$ high (no wait states)	2Q – 17		2Q – 20			ns
$t_{h(D)W}$	Data write hold time from $\overline{STRB}$ high	Q – 5		Q – 10	Q		ns
$t_{en(D)}$	Data bus starts being driven after $\overline{STRB}$ low (write cycle)	0†		0†			ns
$t_{dis(D)}$	Data bus three-state after $\overline{STRB}$ high (write cycle)		Q + 15†		Q	Q + 15†	ns
$t_{d(MSC)}$	$\overline{MSC}$ valid from CLKOUT1	–5	10	–10	0	10	ns

† These values are derived from characterization data and not tested.

timing requirements over recommended operating conditions (see Note 1)

		SMJ320C25-50		SMJ320C25		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time, read data from address time (read cycle, see Notes 3 and 5)		3Q – 31		3Q – 35	ns
$t_{su(D)R}$	Setup time, data read before $\overline{STRB}$ high	17		23		ns
$t_{h(D)R}$	Hold time, data read from $\overline{STRB}$ high	0		0		ns
$t_{d(SL–R)}$	Delay time, READY valid after $\overline{STRB}$ low (no wait states)		Q – 20		Q – 20	ns
$t_{d(C2H–R)}$	Delay time, READY valid after CLKOUT2 high		Q – 21		Q – 20	ns
$t_{h(SL–R)}$	Hold time, READY after $\overline{STRB}$ low (no wait states)	Q – 1		Q + 3		ns
$t_{h(C2H–R)}$	Hold time, READY after CLKOUT2 high	Q – 1		Q + 3		ns
$t_{d(M–R)}$	Delay time, READY valid after $\overline{MSC}$ valid		2Q – 25		2Q – 25	ns
$t_{h(M–R)}$	Hold time, READY after $\overline{MSC}$ valid	0		0		ns

NOTES: 1: $0 = 1/4t_{c(C)}$
3. A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and BR timings are all included in timings referenced as ”address”
4. Delays between CLKOUT1 /CLKOUT2 edges and $\overline{STRB}$ edges track each other, resulting in tw(SL) and tw(SH) being 2Q with no wait states.
5. Read data access time is defined as $t_{a(A)} = t_{su(A)} + t_{w(SL)} – t_{su(D)R} + t_{r(C)}$.

$\overline{RS}$, $\overline{INT}$, $\overline{BIO}$, and XF timing

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		SMJ320C25-50			SMJ320C25			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{d(RS)}$	Delay time, CLKOUT1 low to reset state entered			22†			22†	ns
$t_{d(IACK)}$	Delay time, CLKOUT1 to $\overline{IACK}$ valid	–5†	0	7	–8†	0	8	ns
$t_{d(XF)}$	Delay time, XF valid before falling edge of $\overline{STRB}$	Q – 10			Q – 12			ns

timing requirements over recommended operating conditions (see Note 1)

		SMJ320C25-50		SMJ320C25		UNIT
		MIN	MAX	MIN	MAX	
$t_{su(IN)}$	Setup time, $\overline{INT}$/$\overline{BIO}$/$\overline{RS}$ before CLKOUT1 high	25		32		ns
$t_{h(IN)}$	Hold time, $\overline{INT}$/$\overline{BIO}$/$\overline{RS}$ after CLKOUT1 high	0		0		ns
$t_{w(IN)}$	Pulse duration, $\overline{INT}$/$\overline{BIO}$ low	$t_{c(C)}$		$t_{c(C)}$		ns
$t_{w(RS)}$	Pulse duration, $\overline{RS}$ low	$3t_{c(C)}$		$3t_{c(C)}$		ns

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		SMJ320C25-50			SMJ320C25			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{d(C1L-AL)}$	Delay time, $\overline{HOLDA}$ low after CLKOUT1 low	–1		11	–1		10	ns
$t_{dis(AL-A)}$	Disable time, $\overline{HOLDA}$ low to address three-state		0			0		ns
$t_{dis(C1L-A)}$	Disable time, address three-state after CLKOUT1 low ($\overline{HOLD}$ mode, see Note 7)			20†			20†	ns
$t_{d(HH-AH)}$	Delay time, $\overline{HOLD}$ high to $\overline{HOLDA}$ high			19			25	ns
$t_{en(A-C1L)}$	Enable time, address driven before CLKOUT1 low ($\overline{HOLD}$ mode, see Note 7)			8†			8†	ns

timing requirements over recommended operating conditions (see Note 1)

		SMJ320C25-50		SMJ320C25		UNIT
		MIN	MAX	MIN	MAX	UNIT
$t_{d(C2H-H)}$	Delay time, $\overline{HOLD}$ valid after CLKOUT2 high		Q – 19		Q – 24	ns

† These values are derived from characterization data and not tested.

NOTES: 1. $Q = 1/4t_{c(C)}$

6. $\overline{RS}$, $\overline{INT}$, and $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle. However, if the specified setup time is met, the exact sequence shown in the timing diagram occurs. $\overline{INT}$/$\overline{BIO}$ fall time must be less than 8 ns.
7. A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, $\overline{STRB}$, and R/$\overline{W}$ timings are all included in timings referenced as '"address".

serial port timing

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		SMJ320C25-50		SMJ320C25		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(CH-DX)}$	Delay time, DX valid after CLKX rising edge (see Note 8)		75		80	ns
$t_{d(FL-DX)}$	Delay time, DX valid after FSX falling edge (TXM = 0. see Note 8)		40		45	ns
$t_{d(CH-FS)}$	FSX valid after CLKX rising edge (TXM = 1)		40		45	ns

timing requirements over recommended operating conditions (see Note 1)

		SMJ320C25-50		SMJ320C25		UNIT
		MIN	MAX	MIN	MAX	
f_{sx}	Serial port frequency	1.25	6250	1.25	5000	kHz
$t_{c(SCK)}$	Serial port clock (CLKX/CLKR) cycle time	160	800 000	200	800 000	ns
$t_{w(SCK1}$	Serial port clock (CLKX/CLKR) low pulse duration (see Note 9)	64		80		ns
$t_{w(SCK)}$	Serial port clock (CLKX/CLKR) high pulse duration (see Note 9)	64		80		ns
$t_{su(FS)}$	FSX/FSR setup time before CLKX/CLKR falling edge (TXM = 0)	5		18		ns
$t_{h(FS)}$	FSX/FSR hold time after CLKX/CLKR falling edge (TXM = 0)	10		20		ns
$t_{su(DR)}$	OR setup time before CLKR falling edge	5		10		ns
$t_{h(DR)}$	OR hold time after CLKR falling edge	10		20		ns

NOTES: 1: $Q = 1/4t_{c(C)}$
8. The last occurrence of FSX falling and CLKX rising.
9. The duty cycle of the serial port clock must be within 40–60% .Serial port clock (CLKX/CLKR) rise and fall times must be less than 25 ns.

TIMING DIAGRAMS

Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.2 V with the exception of CLKOUT1, CLKOUT2, and $\overline{\text{STRB}}$ timing that are referenced from a falling edge low voltage of 1.1 V and a rising edge low voltage of 2.2 V.

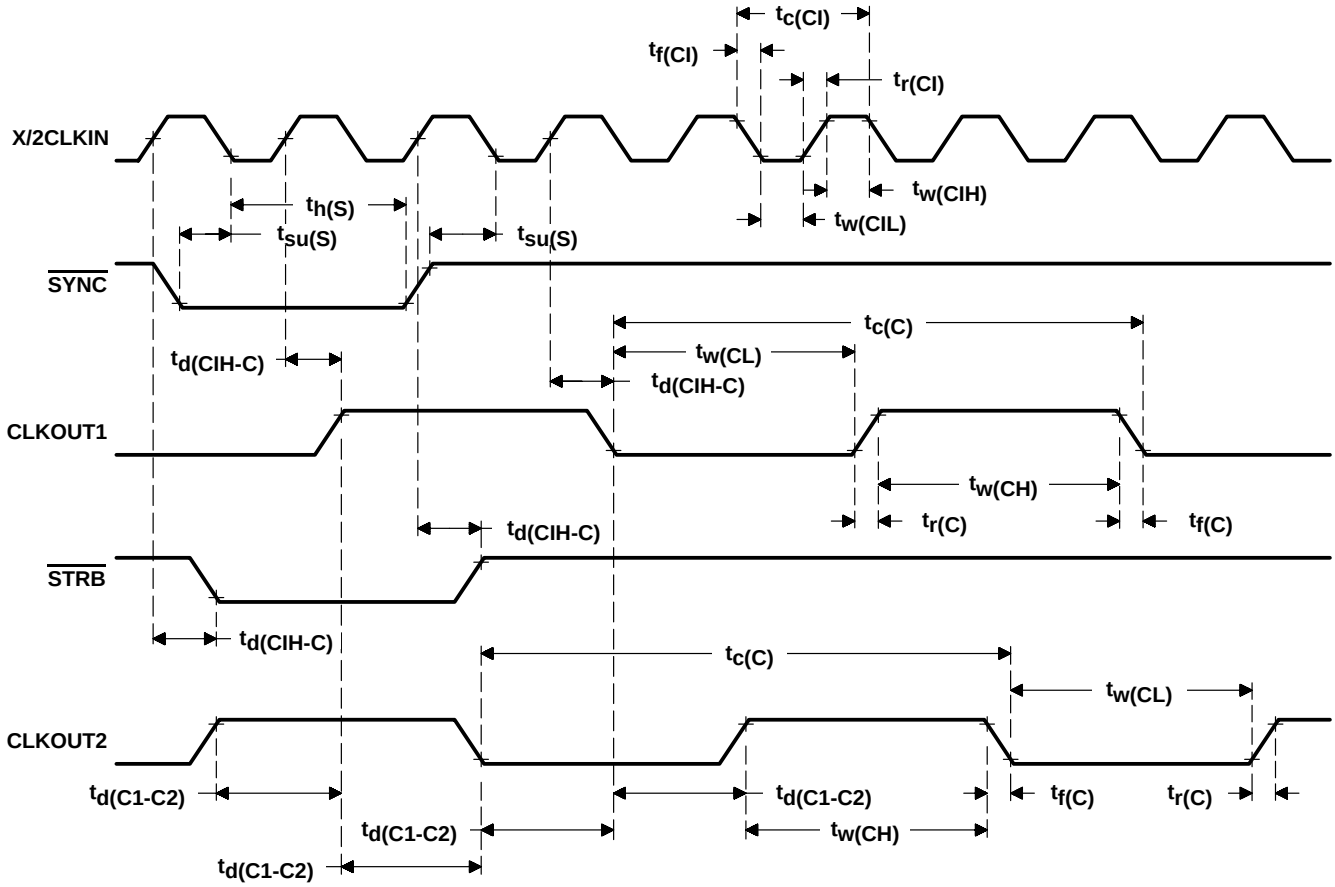


Figure 5. Clock Timing

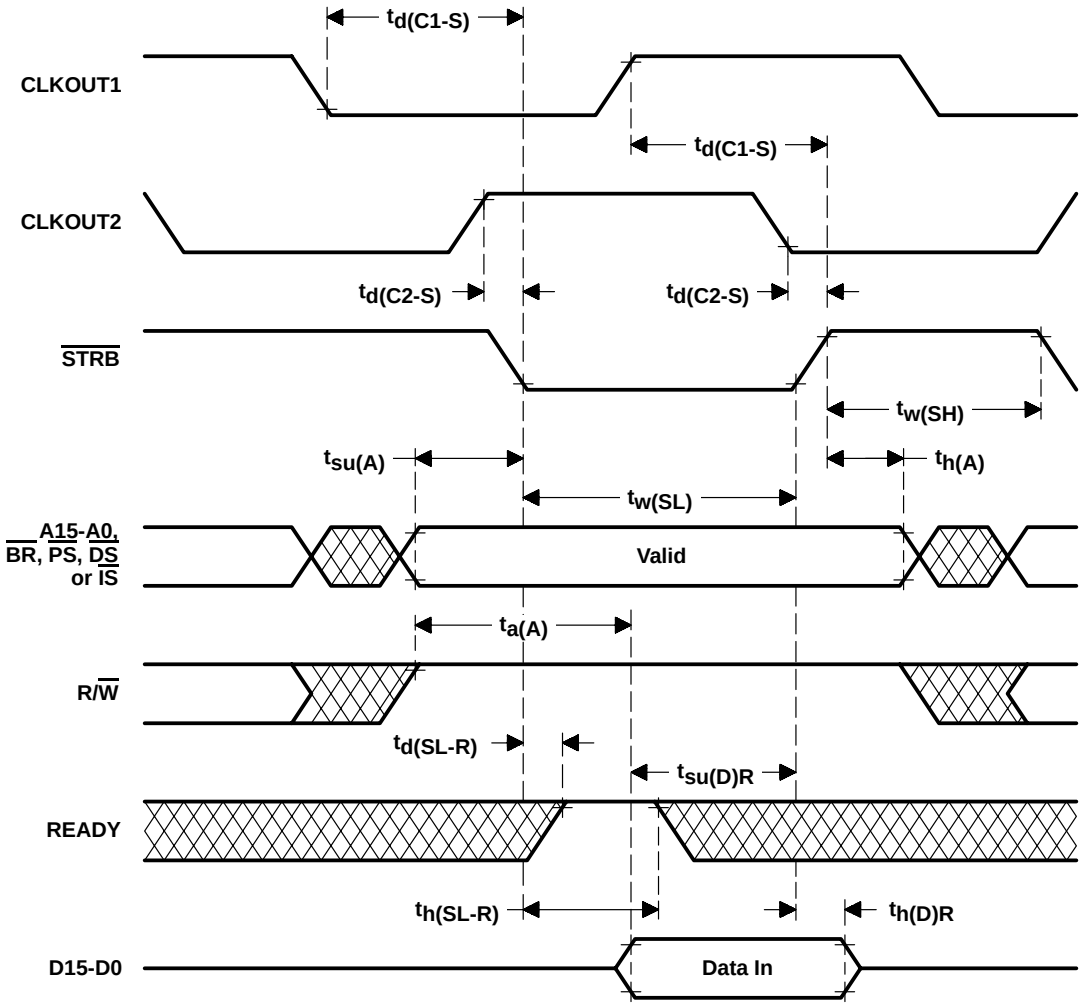


Figure 6. Memory Read Timing

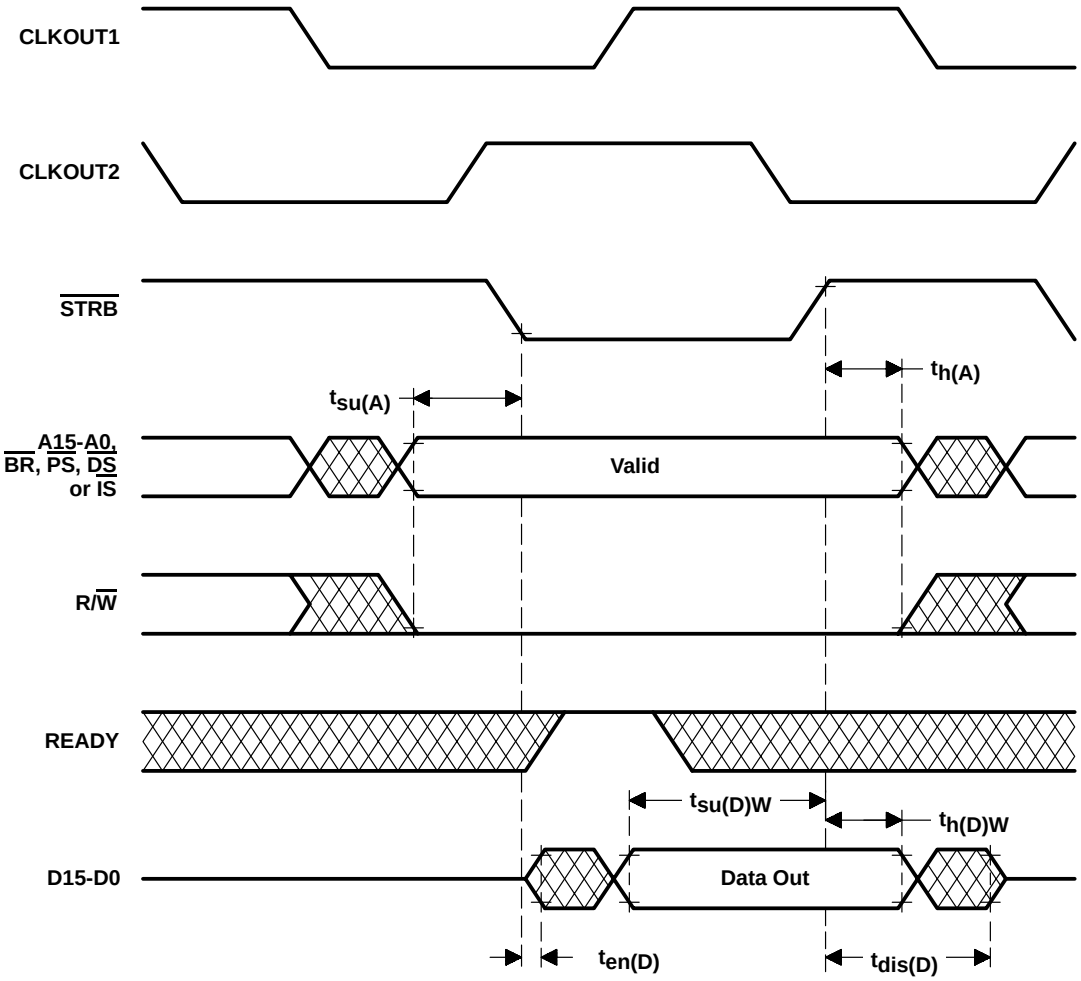


Figure 7. Memory Write Timing

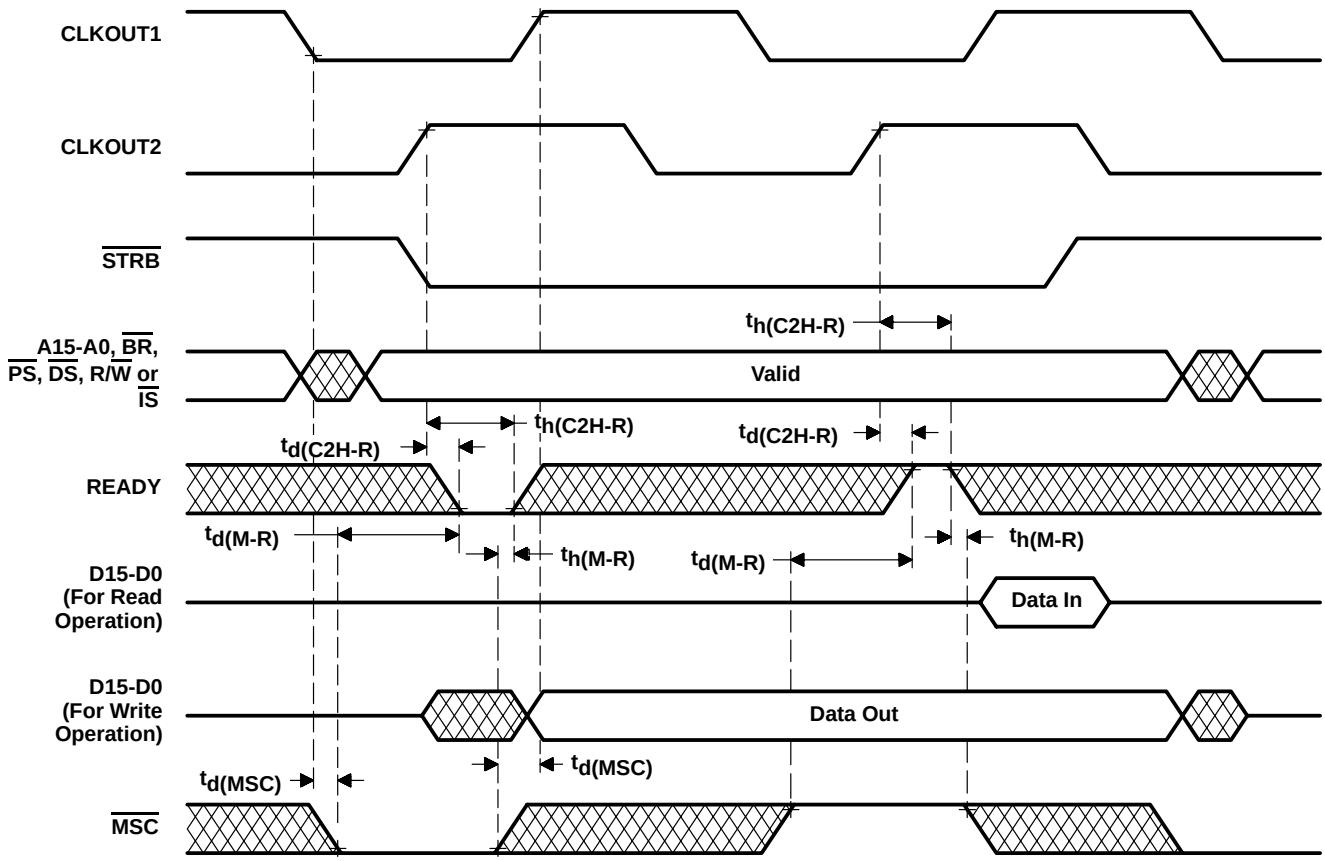
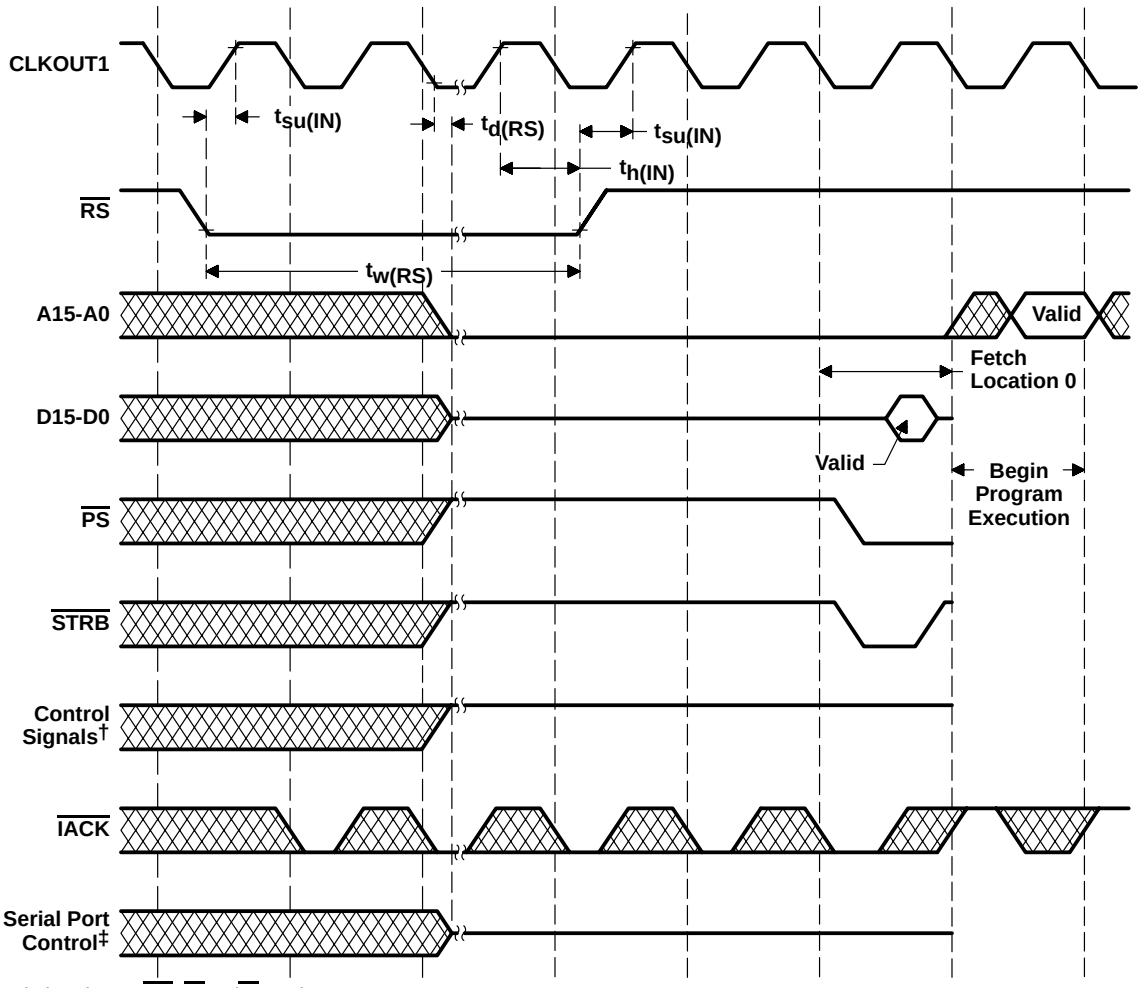


Figure 8. One Wait-State Memory Access Timing



† Control signals are DS, IS, R/W, and XF.
‡ Serial port controls are DX and FSX.

Figure 9. Reset Timing

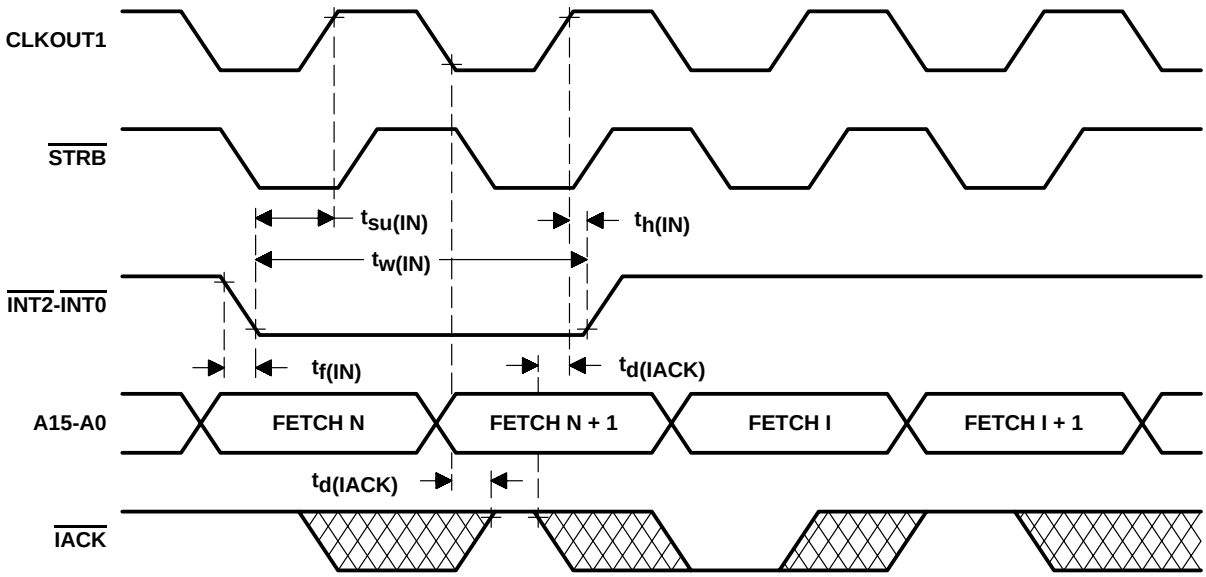


Figure 10. Interrupt Timing

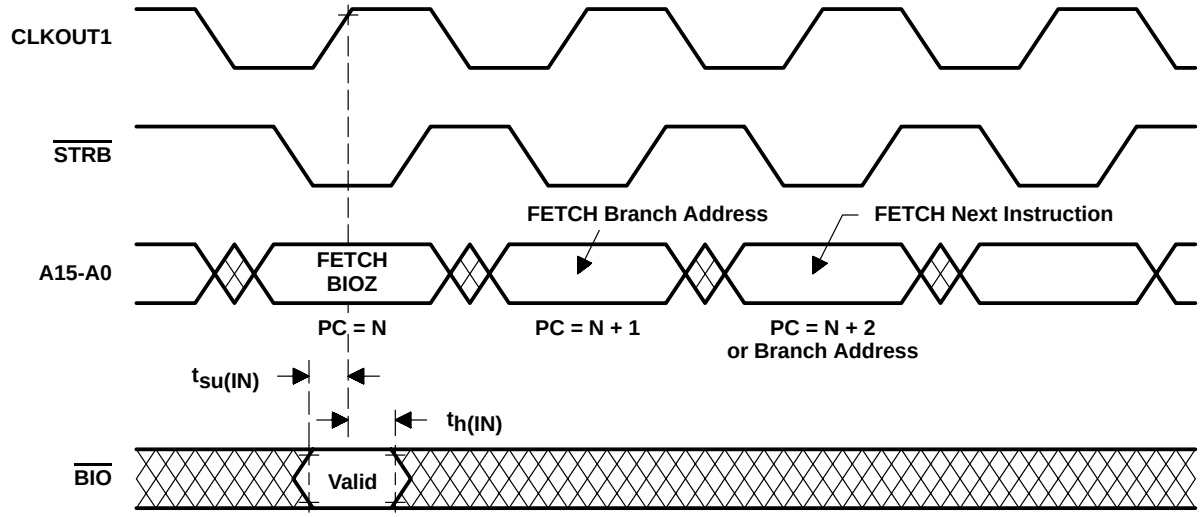


Figure 11. $\overline{\text{BIO}}$ Timing

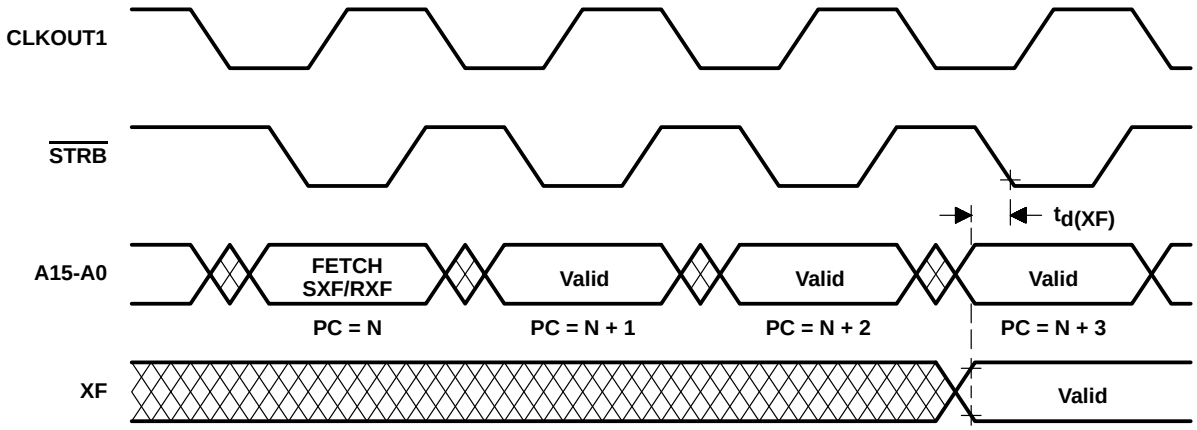
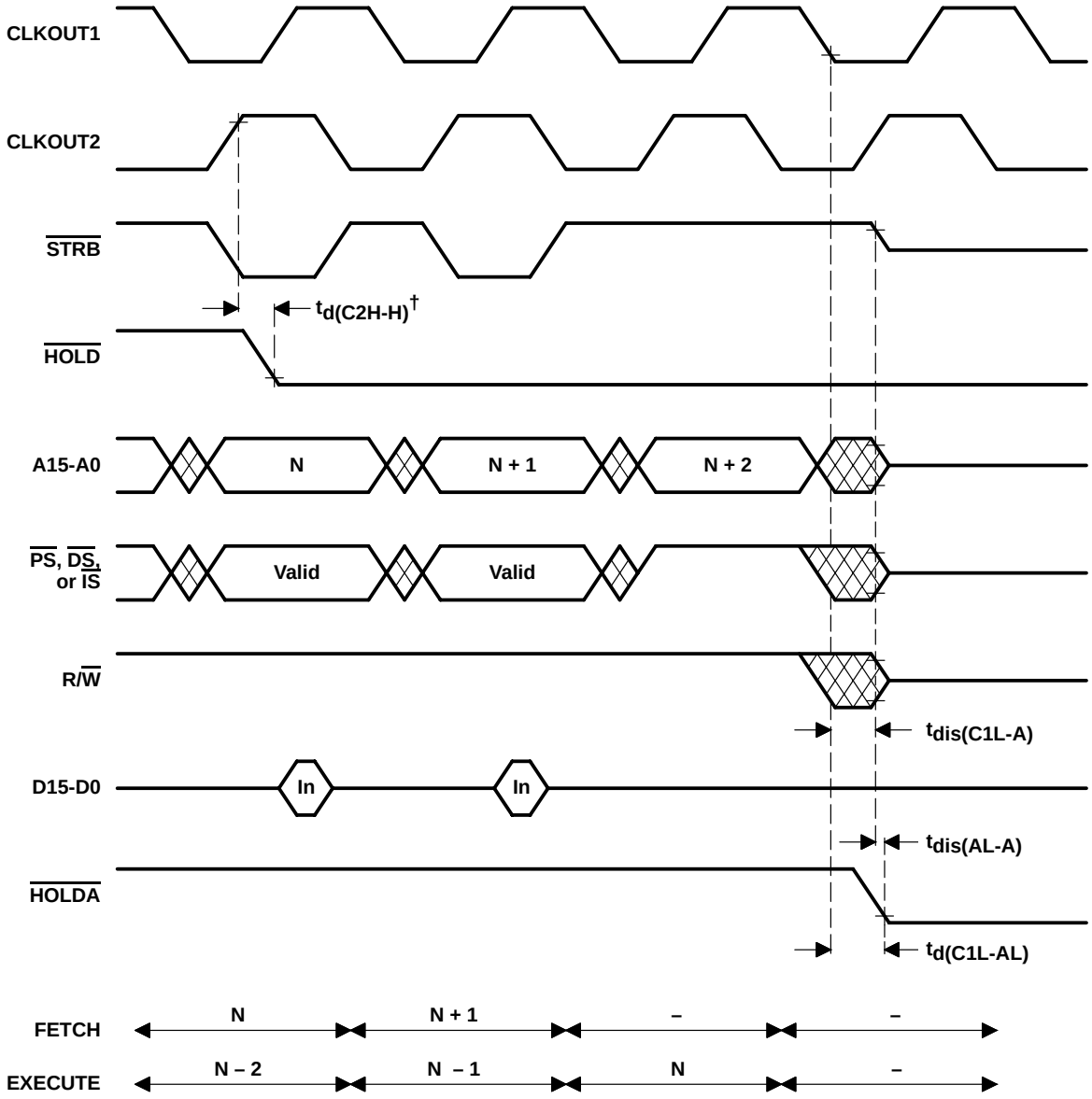
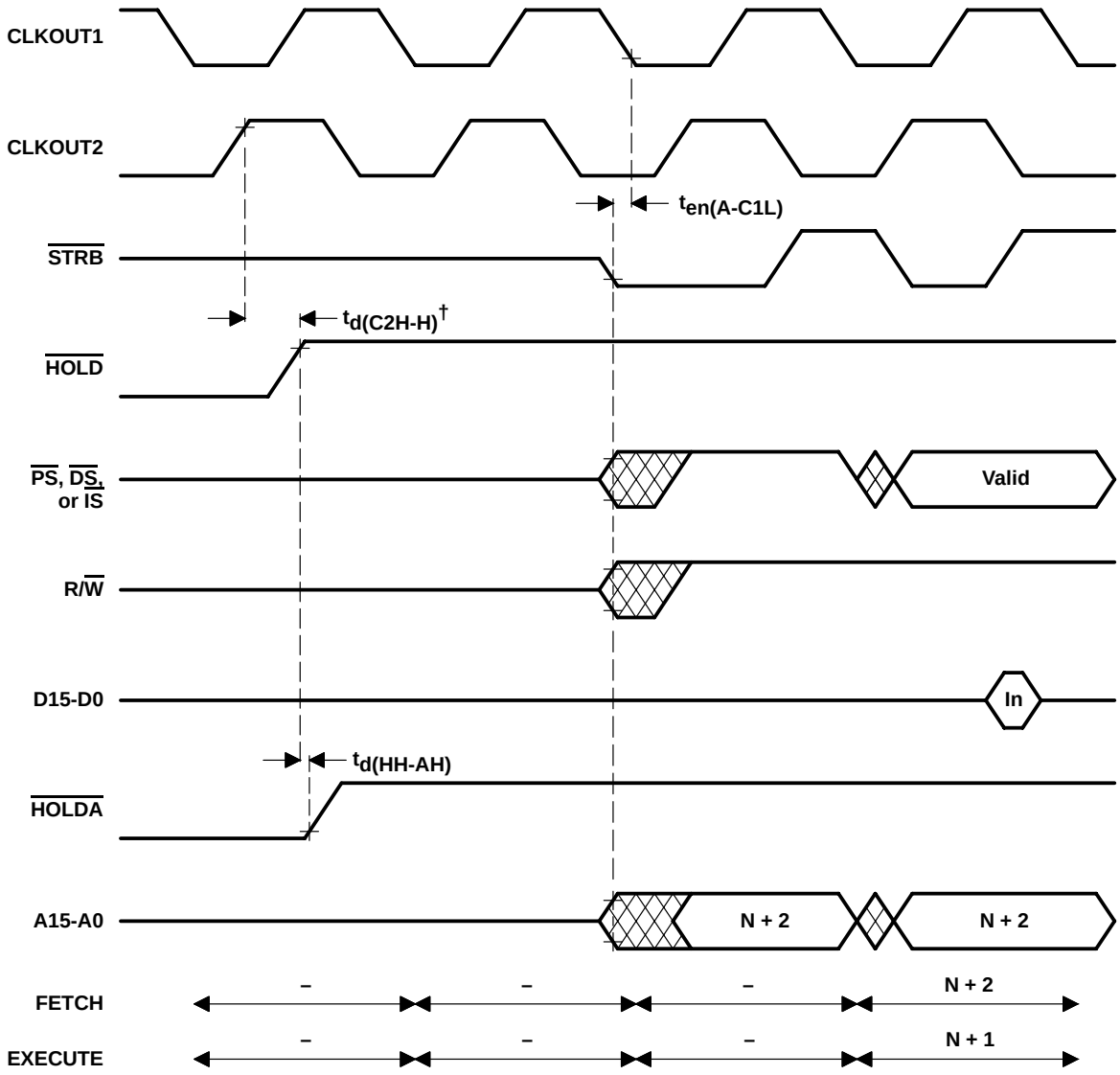


Figure 12. External Flag Timing



† HOLD is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown occurs; otherwise, a delay of one CLKOUT2 cycle occurs.

Figure 13. HOLD Timing (part A)



† $\overline{\text{HOLD}}$ is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown occurs; otherwise, a delay of one CLKOUT2 cycle occurs.

Figure 14. $\overline{\text{HOLD}}$ Timing (part B)

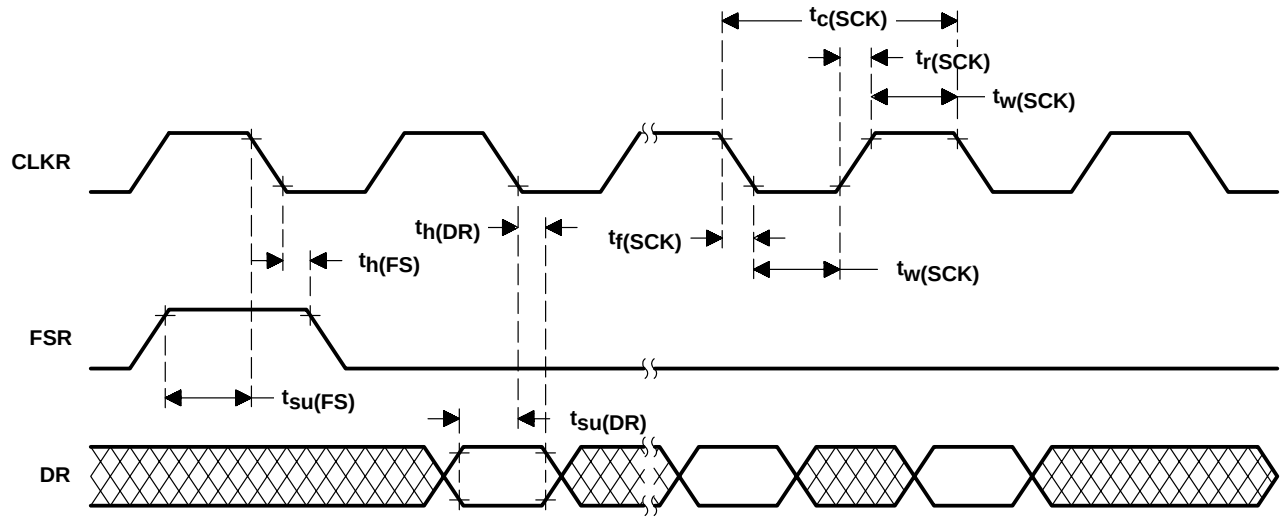


Figure 15. Serial Port Receive Timing

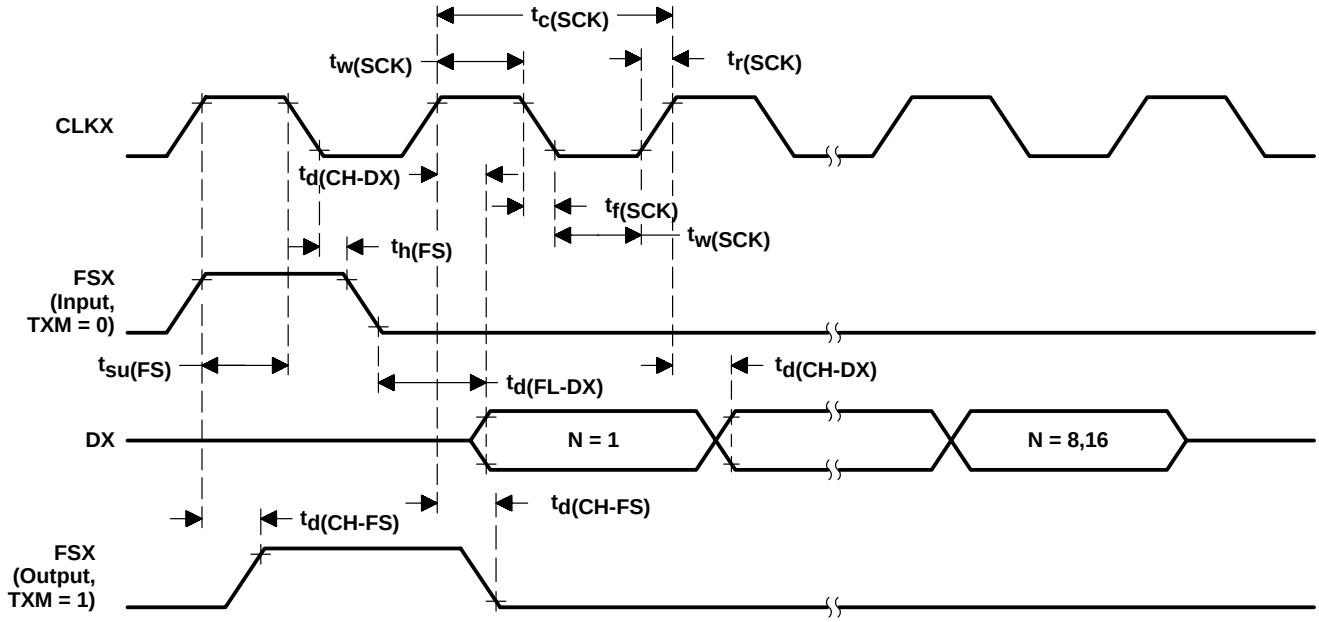


Figure 16. Serial Port Transmit Timing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-8861901XA	ACTIVE	CPGA	GB	68	1	TBD	Call TI	Call TI	
5962-8861901YA	ACTIVE	LCCC	FD	68	1	TBD	Call TI	Call TI	
5962-8861901ZA	ACTIVE	JLCC	FJ	68	1	TBD	Call TI	Call TI	
5962-8861902XA	ACTIVE	CPGA	GB	68	1	TBD	Call TI	Call TI	
5962-8861902ZA	ACTIVE	JLCC	FJ	68	1	TBD	Call TI	Call TI	
SM320C25GBM	ACTIVE	CPGA	GB	68	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C25-50FJM	ACTIVE	JLCC	FJ	68	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C25-50GBM	ACTIVE	CPGA	GB	68	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C25FDM	ACTIVE	LCCC	FD	68	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C25FJM	ACTIVE	JLCC	FJ	68	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C25GBM	ACTIVE	CPGA	GB	68	1	TBD	Call TI	N / A for Pkg Type	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SMJ320C25 :

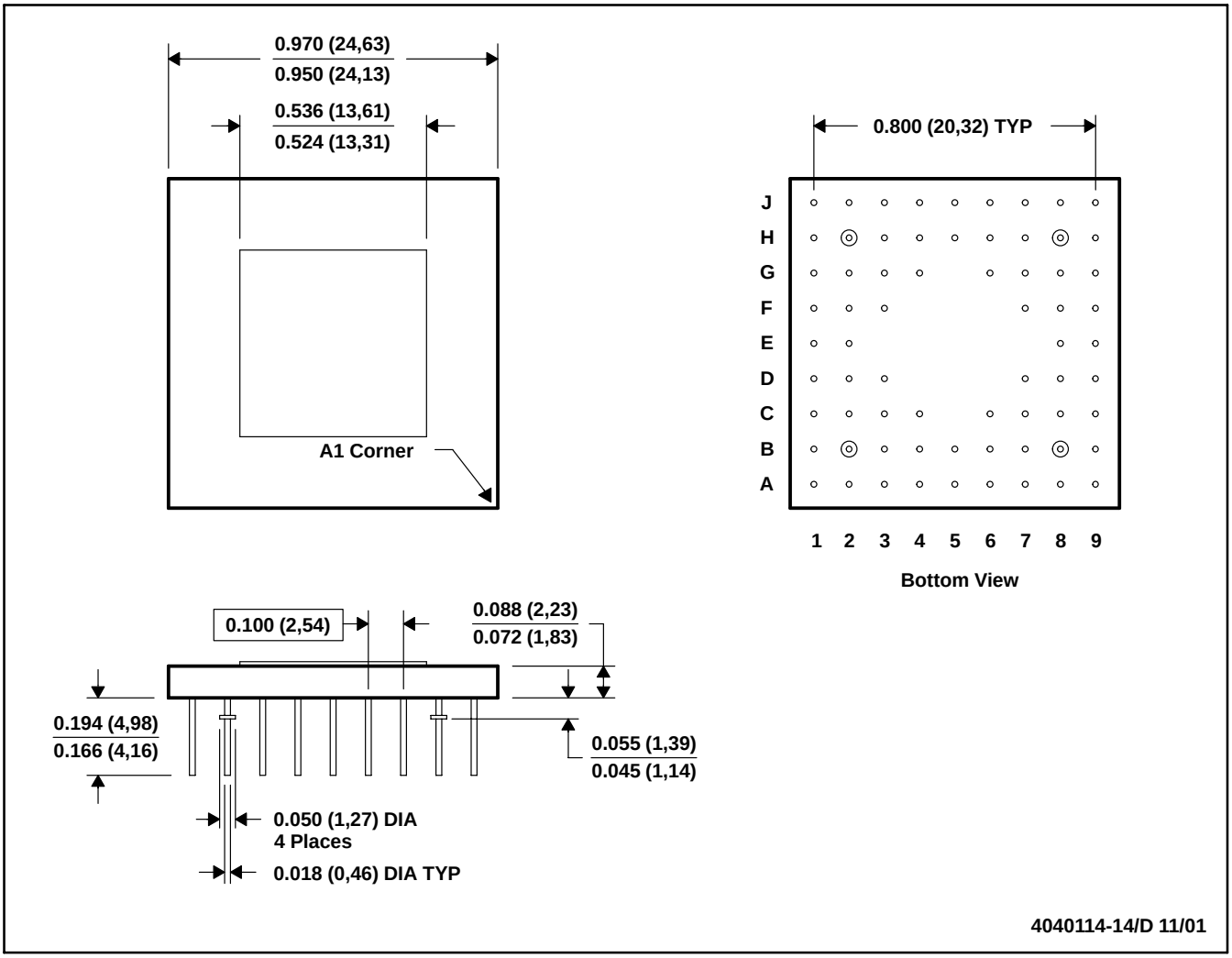
- Catalog: TMS320C25

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

MCPG023A – OCTOBER 1997 – REVISED DECEMBER 2001

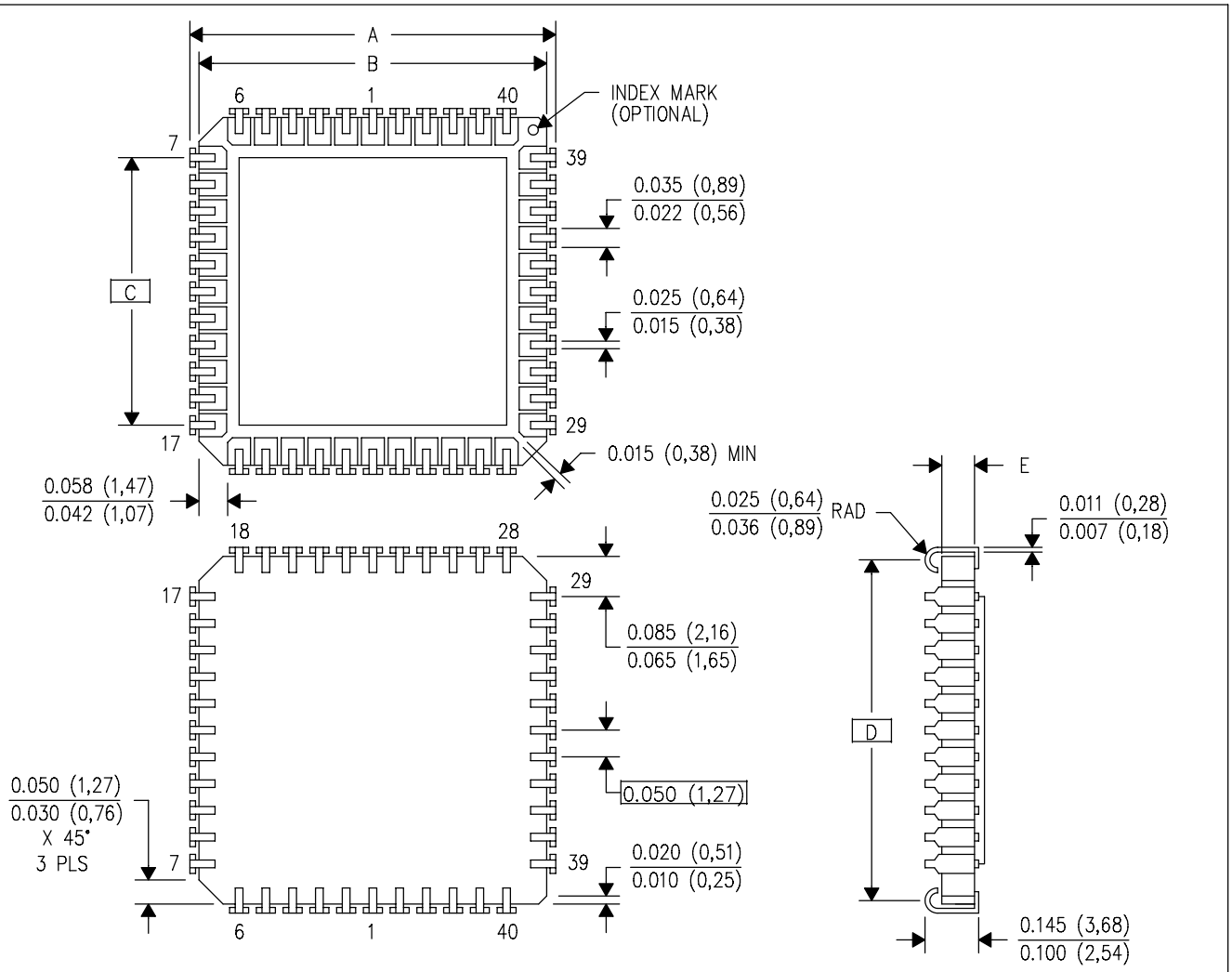
GB (S-CPGA-P68) **CERAMIC PIN GRID ARRAY**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending vendor.
D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edges of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold plated or solder dipped.
G. Falls within MIL STD 1835 CMGA1-PN, CMGA13-PN and JEDEC MO-067 AA, MO-066 AA respectively

FJ (S–CQCC–J**) J–LEADED CERAMIC CHIP CARRIER

44 PINS SHOWN



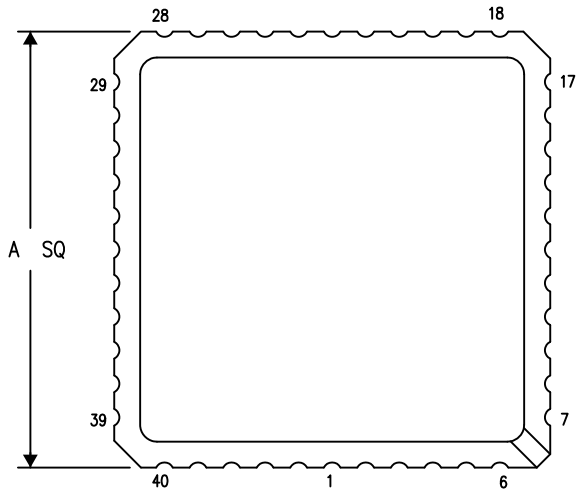
DIM / PINS **	A MAX	A MIN	B MAX	B MIN	C BSC	D BSC	E MAX	E MIN
44	0.700 (17,78)	0.680 (17,27)	0.659 (16,74)	0.641 (16,28)	0.500 (12,70)	0.630 (16,00)	0.080 (2,03)	0.058 (1,47)
68	1.000 (25,40)	0.980 (24,89)	0.960 (24,38)	0.940 (23,88)	0.800 (20,32)	0.930 (23,62)	0.095 (2,41)	0.072 (1,83)

4040139/D 04/03

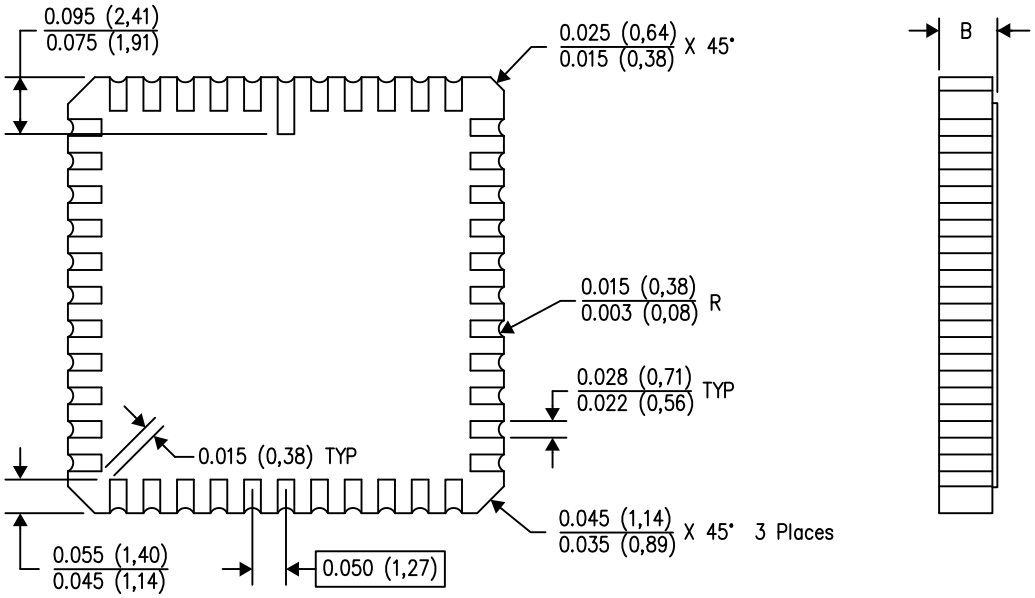
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending on package vendor.
D. This package is hermetically sealed with a metal lid.

FD (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

44 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.064 (1,63)	0.080 (2,03)
28	0.442 (11,23)	0.458 (11,63)	0.064 (1,63)	0.080 (2,03)
44	0.640 (16,26)	0.660 (16,76)	0.069 (1,75)	0.120 (3,05)
52	0.739 (18,78)	0.761 (19,33)	0.082 (2,08)	0.120 (3,05)
68	0.938 (23,83)	0.962 (24,43)	0.082 (2,08)	0.120 (3,05)
84	1.135 (28,83)	1.165 (29,59)	0.082 (2,08)	0.120 (3,05)



4040136/C 08/12

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Falls within JEDEC MS–004.

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