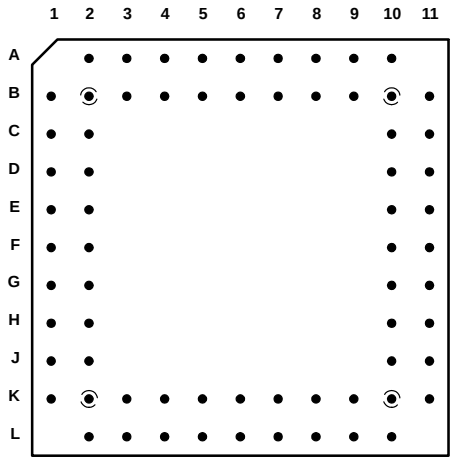
SGUS 016A – AUGUST 1990 – REVISED AUGUST 2001

- 100-ns Instruction Cycle Time
- 1568 Words of Configurable On-Chip Data/Program RAM
- 256 Words of On-Chip Program ROM
- 128K Words of Data/Program Space
- Pin-for-Pin Compatible with the SMJ320C25
- 16 Input and 16 Output Channels
- 16-Bit Parallel Interface
- Directly Accessible External Data Memory Space
- Global Data Memory Interface
- 16-Bit Instruction and Data Words
- 32-Bit ALU and Accumulator
- Single-Cycle Multiply/Accumulate Instructions
- 0 to 16-Bit Scaling Shifter
- Bit Manipulation and Logical Instructions
- Instruction Set Support for Floating-Point Operations, Adaptive Filtering, and Extended-Precision Arithmetic
- Block Moves for Data/Program Management
- Repeat Instructions for Efficient Use of Program Space
- Eight Auxiliary Registers and Dedicated Arithmetic Unit for Indirect Addressing
- Serial Port for Direct Codec Interface
- Synchronization Input for Multiprocessor Configurations
- Wait States for Communications to Slow Off-Chip Memories/Peripherals
- On-Chip Timer for Control Operations
- Three External Maskable User Interrupts

68-PIN GB
PIN GRID ARRAY CERAMIC PACKAGE†
(TOP VIEW)



† See Pin Assignments Table (Page 2) and Pin Nomenclature Table (Page 3) for location and description of all pins.

- Input Pin Polled by Software Branch Instruction
- Programmable Output Pin for Signalling External Devices
- 1.6-μm CMOS Technology
- Single 5-V Supply
- Packaging:
- 68-Pin Leaded Ceramic Chip Carrier (FJ Suffix)
- 68-Pin Leadless Ceramic Chip Carrier (FD Suffix)
- 68-Pin Grid Array Ceramic Package (GB Suffix)
- Military Operating Temperature Range . . . – 55° to 125°C

description

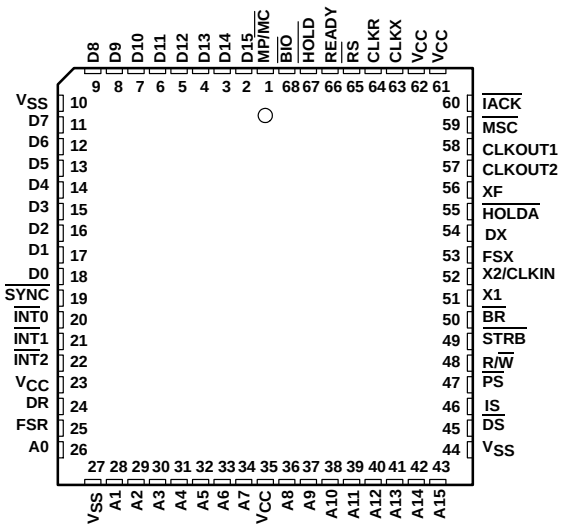
The SMJ320C26 Digital Signal Processor is a member of the TMS320 family of VLSI digital signal processors and peripherals. The TMS320 family supports a wide range of digital signal processing applications, such as telecommunications, modems, image processing, speech processing, spectrum analysis, audio processing, digital filtering, high-speed control, graphics, and other computation intensive applications.

description

With a 100-ns instruction cycle time and an innovative memory configuration, the SMJ320C26 performs operations necessary for many real time digital signal processing algorithms. Since most instructions require only one cycle, the SMJ320C26 is capable of executing ten million instructions per second. On-chip programmable data/program RAM of 1568 words of 16 bits, on-chip program ROM of 256-words, direct addressing of up to 64K-words of external program and 64K-words of data memory space, and multiprocessor interface features for sharing global memory minimize unnecessary data transfers to take full advantage of the capabilities of the processor.

The SMJ320C26 scaling shifter has a 16-bit input connected to the data bus and a 32-bit output connected to the ALU. The scaling shifter produces a left shift of 0 to 16 bits on the input data, as programmed in the instruction. The LSBs of the output are filled with zeroes, and the MSBs may be either filled with zeroes or sign-extended, depending upon the status programmed into the SXM (sign-extension mode) bit of status register ST1.

**68-PIN FJ AND FD
LEADED AND LEADLESS
CERAMIC CHIP CARRIER PACKAGES†
(TOP VIEW)**



† See Pin Assignments Table (Page 2) and Pin Nomenclature Table (Page 3) for location and description of all pins.

PGA/LCCC/JLCC PIN ASSIGNMENTS

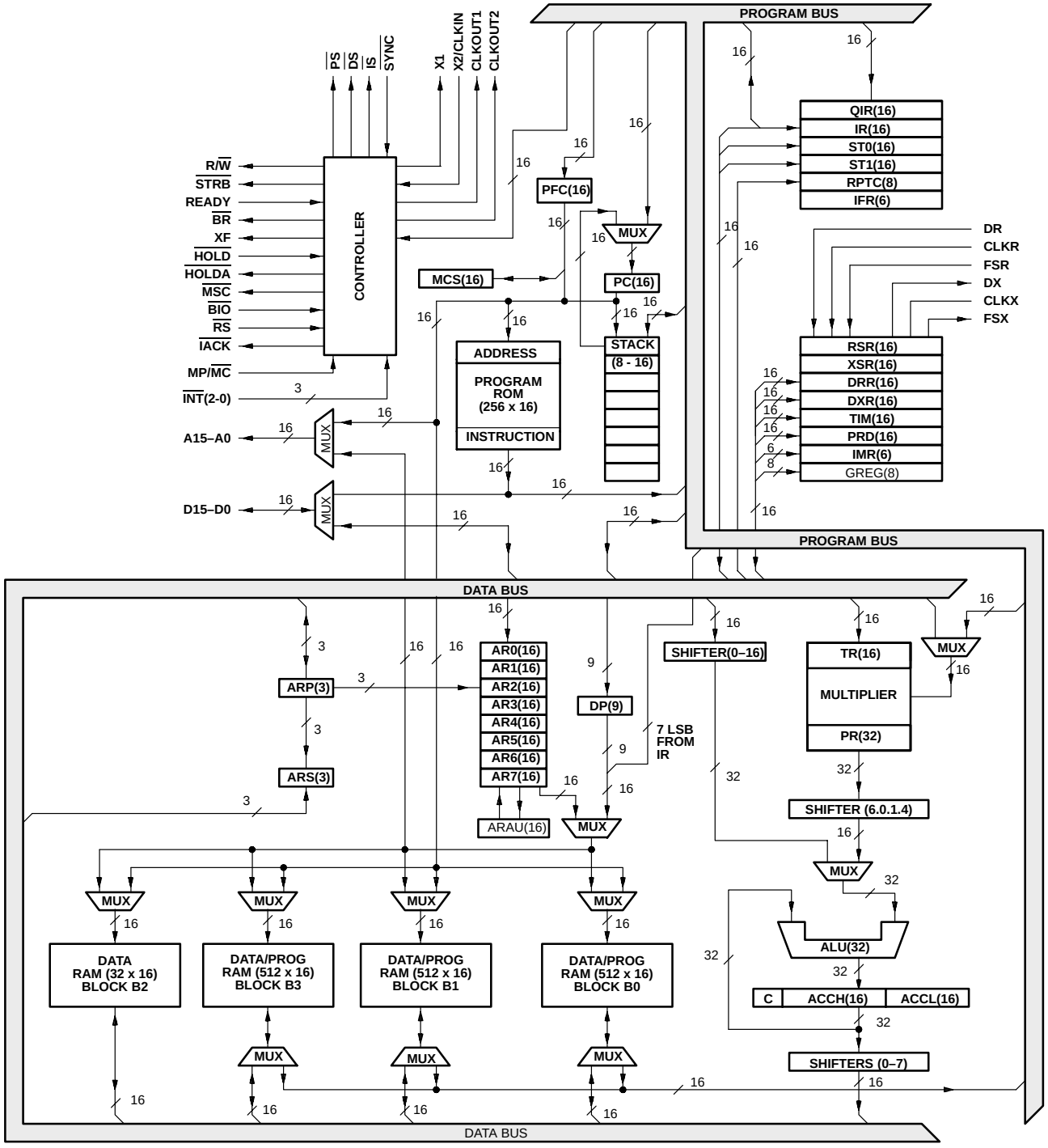
FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN
A0	K1/26	A12	K8/40	D2	E1/16	D14	A5/3	INT2	H1/22	V_{CC}	H2/23
A1	K2/28	A13	L9/41	D3	D2/15	D15	B6/2	$\overline{IS}$	J11/46	V_{CC}	L6/35
A2	L3/29	A14	K9/42	D4	D1/14	DR	J1/24	MP/$\overline{MC}$	A6/1	V_{SS}	B1/10
A3	K3/30	A15	L10/43	D5	C2/13	$\overline{DS}$	K10/45	$\overline{MSC}$	C10/59	V_{SS}	K11/44
A4	L4/31	$\overline{BIO}$	B7/68	D6	C1/12	DX	E11/54	$\overline{PS}$	J10/47	V_{SS}	L2/27
A5	K4/32	$\overline{BR}$	G11/50	D7	B2/11	FSR	J2/25	READY	B8/66	XF	D11/56
A6	L5/33	CLKOUT1	C11/58	D8	A2/9	FSX	F10/53	$\overline{RS}$	A8/65	X1	G10/51
A7	K5/34	CLKOUT2	D10/57	D9	B3/8	$\overline{HOLD}$	A7/67	R/$\overline{W}$	H11/48	X2/CLKIN	F11/52
A8	K6/36	CLKR	B9/64	D10	A3/7	$\overline{HOLDA}$	E10/55	$\overline{STRB}$	H10/49		
A9	L7/37	CLKX	A9/63	D11	B4/6	$\overline{IACK}$	B11/60	$\overline{SYNC}$	F2/19		
A10	K7/38	D0	F1/18	D12	A4/5	$\overline{INT0}$	G1/20	V_{CC}	A10/61		
A11	L8/39	D1	E2/17	D13	B5/4	$\overline{INT1}$	G2/21	V_{CC}	B10/62		

PIN NOMENCLATURE

NAME	I/O/Z†	DEFINITION
V_{CC}	I	5-V supply pins.
V_{SS}	I	Ground pins.
X1	O	Output from internal oscillator for crystal.
X2/CLKIN	I	Input to internal oscillator from crystal or external clock.
CLKOUT1	O	Master clock output (crystal or CLKIN frequency/4).
CLKOUT2	O	A second clock output signal.
D15–D0	I/O/Z	16-bit data bus D15 (MSB) through D0 (LSB). Multiplexed between program, data and I/O spaces.
A15–A0	O/Z	16-bit address bus A15 (MSB) through A0 (LSB).
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data and I/O space select signals.
R/$\overline{W}$	O/Z	Read/write signal.
$\overline{STRB}$	O/Z	Strobe signal.
$\overline{RS}$	I	Reset input.
$\overline{INT2}$, $\overline{INT1}$, $\overline{INT0}$	I	External user interrupt inputs.
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select pin.
$\overline{MSC}$	O	Microstate complete signal.
$\overline{IACK}$	O	Interrupt acknowledge signal.
READY	I	Data ready input. Asserted by external logic when using slower devices to indicate that the current bus transaction is complete.
$\overline{BR}$	O	Bus request signal. Asserted when the SMJ320C26 requires access to an external global data memory space.
XF	O	External flag output (latched software – programmable signal).
$\overline{HOLD}$	I	Hold input. When asserted, SMJ320C26 goes into an idle mode and places the data address and control lines in the high-impedance state.
$\overline{HOLDA}$	O	Hold acknowledge signal.
$\overline{SYNC}$	I	Synchronization input.
$\overline{BIO}$	I	Branch control input. Polled by BIOZ instruction.
DR	I	Serial data receive input.
CLKR	I	Clock input for serial port receiver.
FSR	I	Frame synchronization pulse for receive input.
DX	O/Z	Serial data transmit output.
CLKX	I	Clock input for serial port transmitter.
FSX	I/O/Z	Frame synchronization pulse for transmit. May be configured as either an input or an output.

† I/O/Z denotes input/output/high-impedance state.

functional block diagram



LEGEND:

ACCH	=	Accumulator high	IFR	=	Interrupt flag register	PC	=	Program counter
ACCL	=	Accumulator low	IMR	=	Interrupt mask register	PFC	=	Prefetch counter
ALU	=	Arithmetic logic unit	IR	=	Instruction register	RPTC	=	Repeat instruction counter
ARAU	=	Auxiliary register arithmetic unit	MCS	=	Microcall stack	GREG	=	Global memory allocation register
ARS	=	Auxiliary register pointer buffer	QIR	=	Queue instruction register	RSR	=	Serial port receive shift register
ARP	=	Auxiliary register pointer	PR	=	Product register	XSR	=	**S**erial port to transmit shift register
DP	=	Data memory page pointer	PRD	=	Product register for timer	AR0–AR7	=	Auxiliary registers
DRR	=	Serial port data receive register	TIM	=	Timer	ST0, ST1	=	Status regi**s**ters
DXR	=	Serial port data trademark register	TR	=	Temporary register	C	=	Carry bit

architecture

The SMJ320C26 architecture is based on the SMJ320C25 with a different internal RAM and ROM configuration. The SMJ320C26 integrates 256 words of on-chip ROM and 1568 words of on-chip RAM compared to 4K words of on-chip ROM and 544 words of on-chip RAM for the SMJ320C25. The SMJ320C26 is pin for pin compatible with the SMJ320C25.

Increased throughput on the SMJ320C26 for many DSP applications is accomplished by means of single cycle multiply/accumulate instructions with a data move option, eight auxiliary registers with a dedicated arithmetic unit, and faster I/O necessary for data intensive signal processing.

The architectural design of the SMJ320C26 emphasizes overall speed, communication, and flexibility in the processor configuration. Control signals and instructions provide floating point support, block memory transfers, communication to slower off-chip devices, and multiprocessing implementations.

Three large on-chip RAM blocks, configurable either as separate program and data spaces or as three contiguous data blocks, provide increased flexibility in system design. Programs of up to 256 words can be masked into the internal program ROM. The remainder of the 64K-word program memory space is located externally. Large programs can execute at full speed from this memory space. Programs can also be downloaded from slow external memory to high speed on-chip RAM. A data memory address space of 64K words is included to facilitate implementation of DSP algorithms. The VLSI implementation of the SMJ320C26 incorporates all of these features as well as many others, including a hardware timer, serial port, and block data transfer capabilities.

32-bit ALU accumulator

The SMJ320C26 32-bit Arithmetic Logic Unit (ALU) and accumulator perform a wide range of arithmetic and logic instructions, the majority of which execute in a single clock cycle. The ALU executes a variety of branch instructions dependent on the status of the ALU or a single bit in a word. These instructions provide the following capabilities:

- Branch to an address specified by the accumulator.
- Normalize fixed point numbers contained in the accumulator.
- Test a specified bit of a word in data memory.

One input to the ALU is always provided from the accumulator, and the other input may be provided from the Product Register (PR) of the multiplier or the input scaling shifter which has fetched data from the RAM on the data bus. After the ALU has performed the arithmetic or logical operations, the result is stored in the accumulator.

The 32-bit accumulator is split into two 16-bit segments for storage in data memory. Additional shifters at the output of the accumulator perform shifts while the data is being transferred to the data bus for storage. The contents of the accumulator remain unchanged.

scaling shifter

The SMJ320C26 scaling shifter has a 16-bit input connected to the data bus and a 32-bit output connected to the ALU. The scaling shifter produces a left shift of 0 to 16-bits on the input data, as specified in the instruction word. The LSBs of the output are filled with zeroes, and the MSBs may be either filled with zeroes or sign extended, depending upon the value of the SXM (sign extension mode) bit of status register STO.

16 $\times$ 16 bit parallel multiplier

The SMJ320C26 has a 16 $\times$ 16 bit-hardware multiplier, which is capable of computing a signed or unsigned 32-bit product in a single machine cycle. The multiplier has the following two associated registers:

- A 16-bit Temporary Register (TR) that holds one of the operands for the multiplier, and
- A 32-bit Product Register (PR) that holds the product.

16 × 16 bit parallel multiplier (continued)

Incorporated into the SMJ320C26 instruction set are single-cycle multiply/accumulate instructions that allow both operands to be fetched simultaneously. The data for these operations may reside anywhere in internal or external memory, and can be transferred to the multiplier each cycle via the program and data buses.

Four product shift modes are available at the Product Register (PR) output that are useful when performing multiply/accumulate operations, fractional arithmetic, or justifying fractional products.

timer

The SMJ320C26 provides a memory mapped 16-bit timer for control operations. The on-chip timer (TIM) register is a down counter that is continuously clocked by CLKOUT1. A timer interrupt (TINT) is generated every time the timer decrements to zero, provided the timer interrupt is enabled. The timer is reloaded with the value contained in the period (PRD) register within the next cycle after it reaches zero so that interrupts may be programmed to occur at regular intervals of PRD + 1 cycles of CLKOUT1.

memory control

The SMJ320C26 provides a total of 1568 words of 16 bit on-chip RAM, divided into four separate blocks (B0, B1, B2, and B3). Of the 1568 words, 32 words (block B2) are always data memory, and all other blocks are programmable as either data or program memory. A data memory size of 1568 words allows the SMJ320C26 to handle a data array of 1536 words, while still leaving 32 locations for intermediate storage. When using B0, B1, or B3 as program memory, instructions can be downloaded from external memory into on-chip RAM, and then executed.

When using on-chip program RAM, ROM, or high speed external program memory, the SMJ320C26 runs at full speed without wait states. However, the READY line can be used to interface the SMJ320C26 to slower, less expensive external memory. Downloading programs from slow off-chip memory to on-chip program RAM speeds processing and cuts overall system costs.

The SMJ320C26 provides three separate address spaces for program memory, data memory, and I/O. The on-chip memory is mapped into either the data memory or program memory space, depending upon the choice of memory configuration.

The instruction configuration (parameter) is used as follows to configure the blocks B0, B1, and B3 as program or as data memory.

CONFIGURATION	B0	B1	B3
0	Data	Data	Data
1	Program	Data	Data
2	Program	Program	Data
3	Program	Program	Program

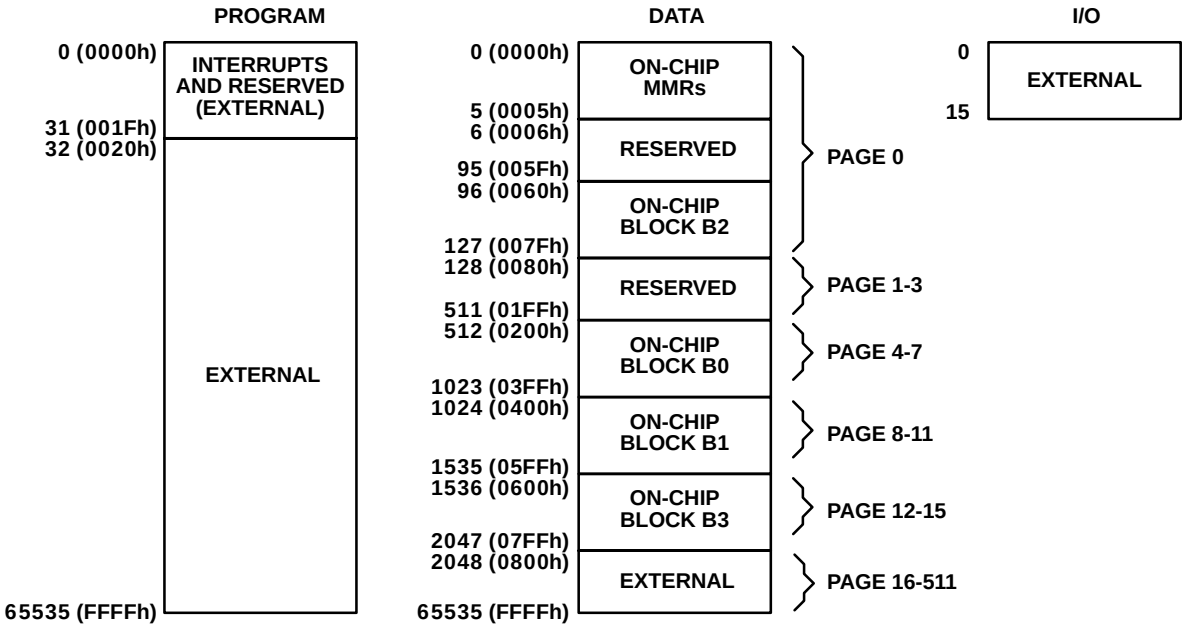
Regardless of the configuration, the user may still execute from external program memory.

The SMJ320C26 provides a ROM of 256 words. The ROM is sufficient to allow the programming of a bootstrap program and interrupt handler, or to implement self test routines.

The SMJ320C26 has six registers that are mapped into the data memory space at the locations 0–5; a serial port data receive register, serial port data transmit register, timer register, period register, interrupt mask register, and global memory allocation register.

memory control (continued)

MEMORY MAPS AFTER A RESET OR CONF 0
1 MP/MC = 1



2 MP/$\overline{MC}$ = 0

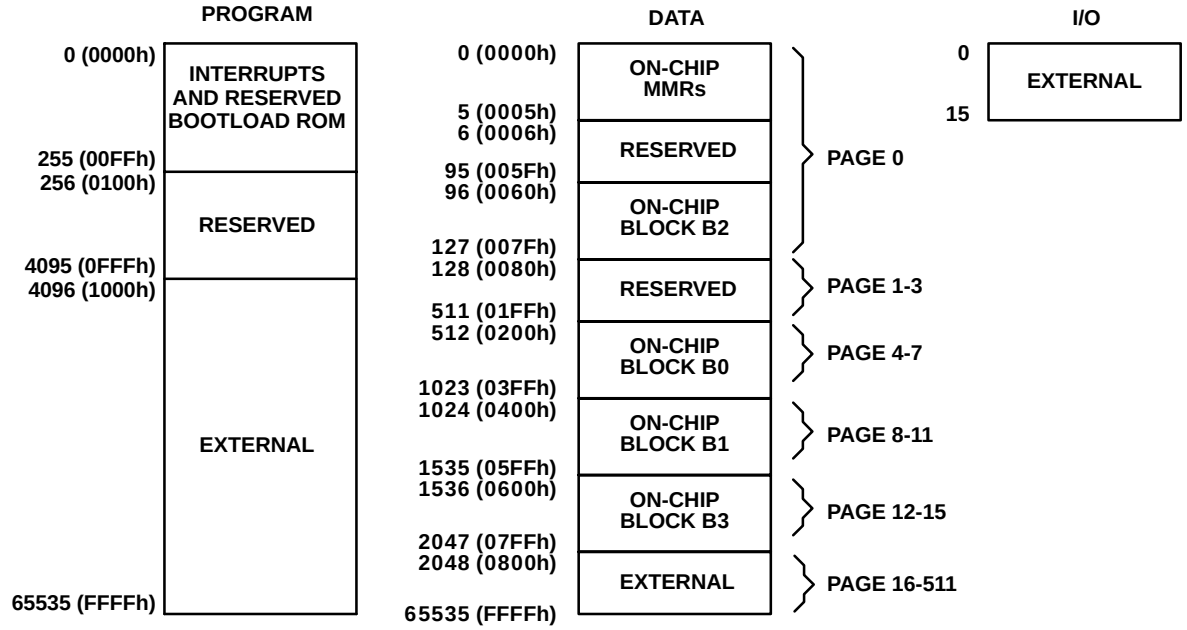
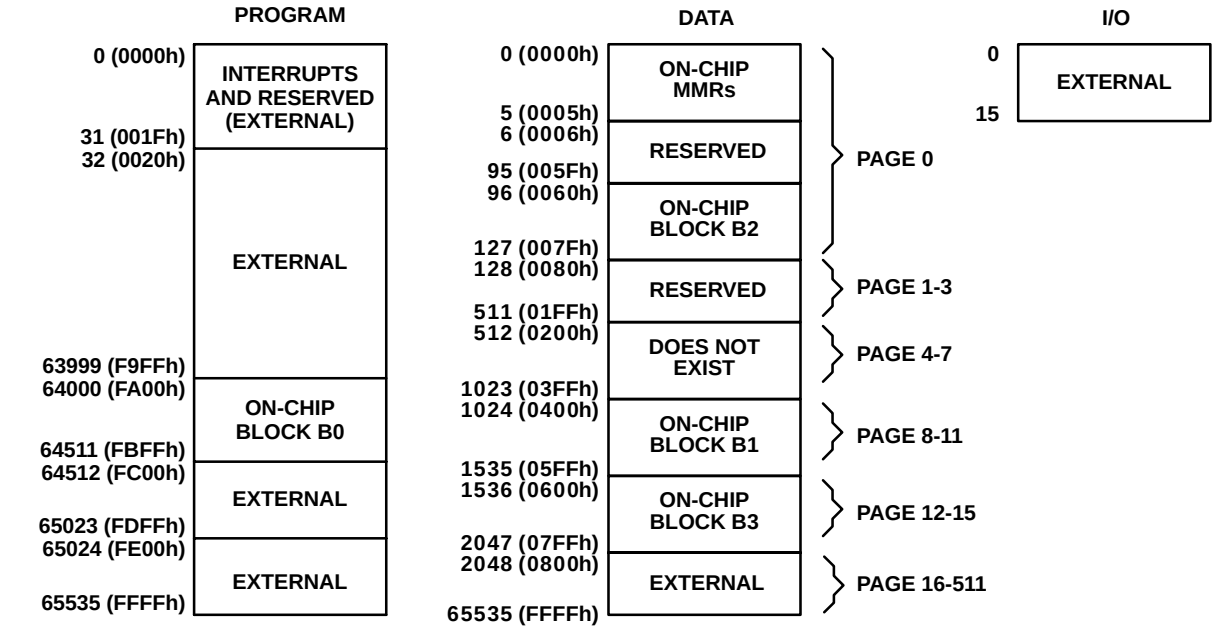


Figure 1A. Memory Maps

memory control (continued)

MEMORY MAPS AFTER CONF 1
1 MP/MC = 1



2 MP/$\overline{MC}$ = 0

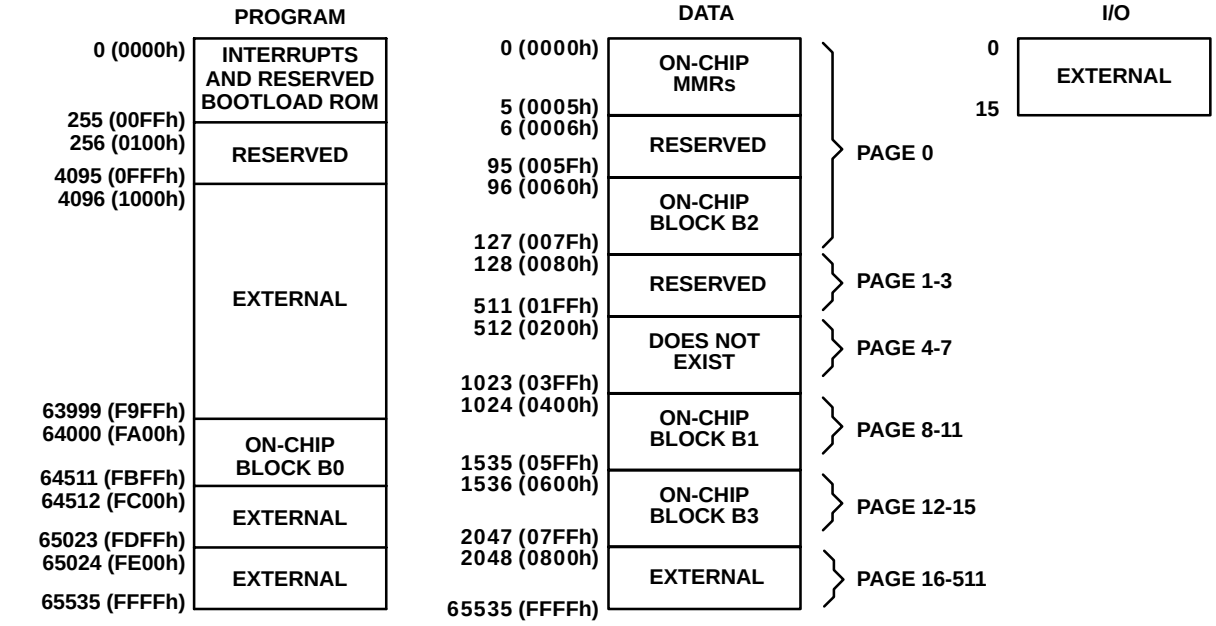
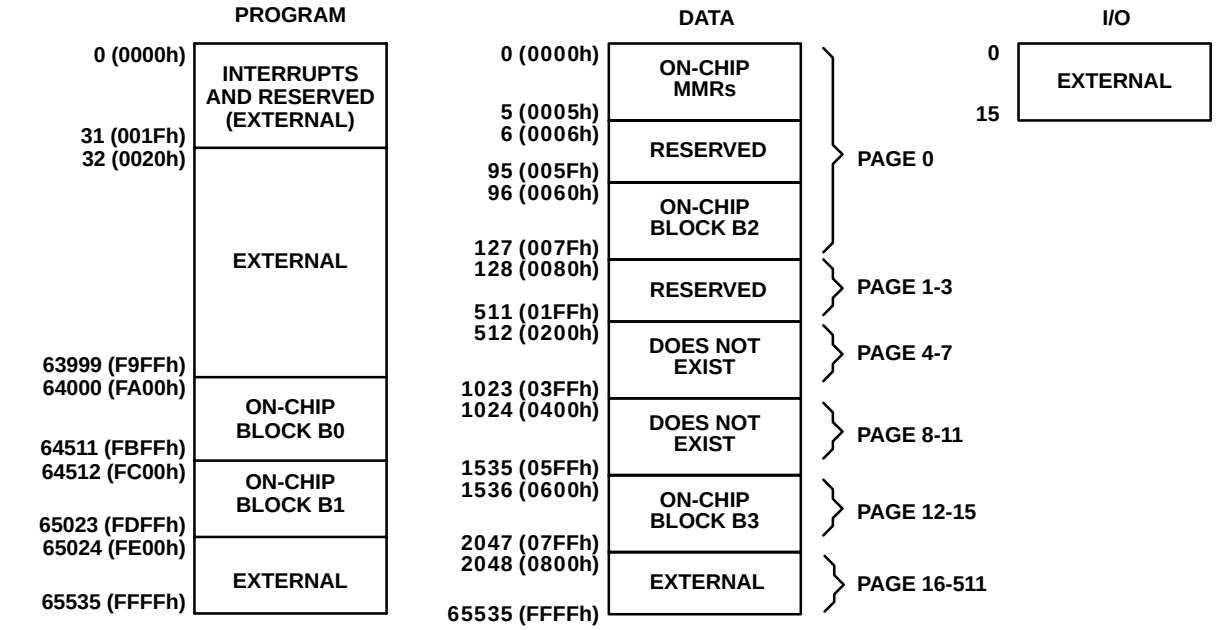


Figure 1B. Memory Maps

memory control (continued)

MEMORY MAPS AFTER CONF 2
1 MP/MC = 1



2 MP/$\overline{MC}$ = 0

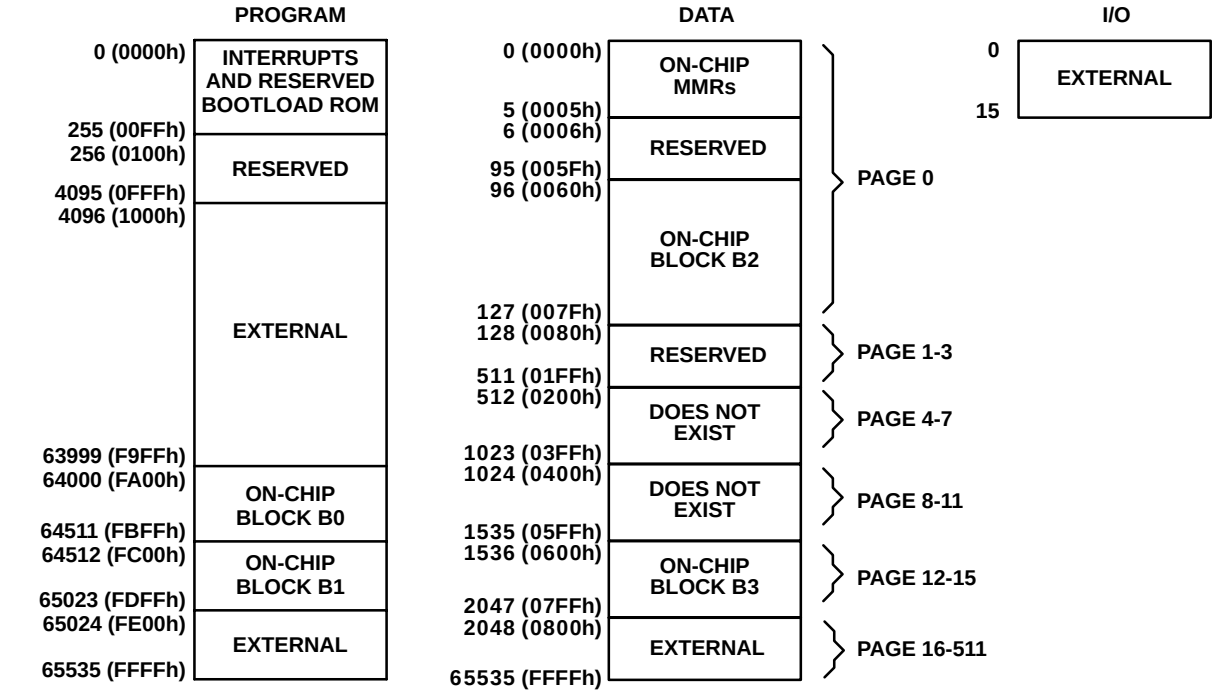
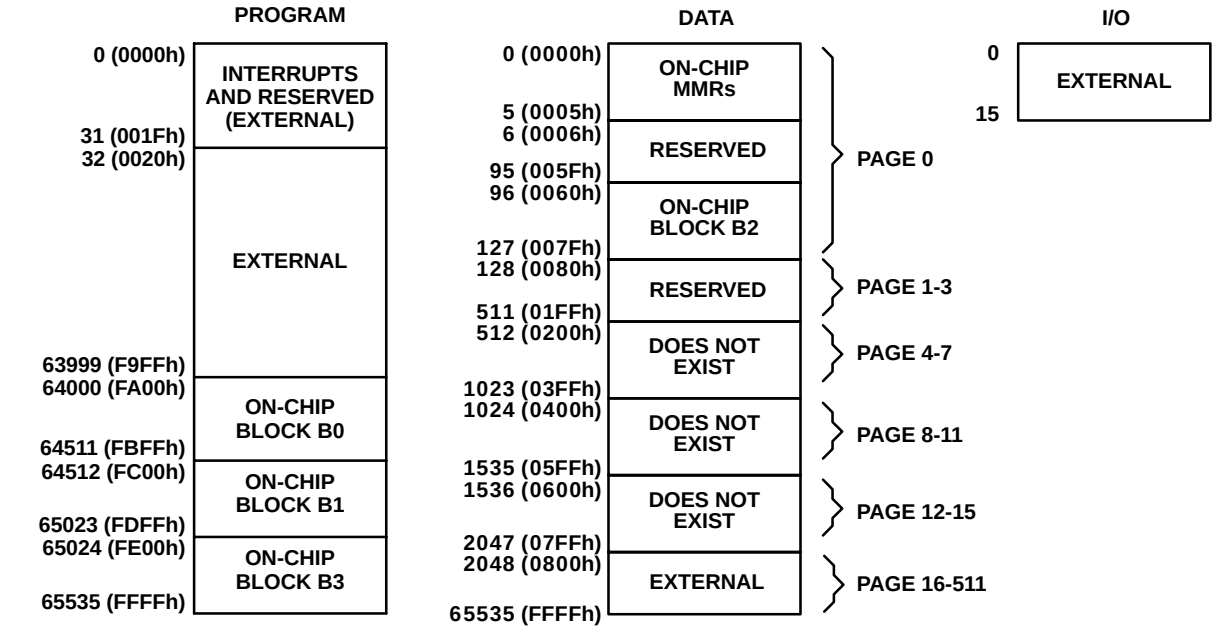


Figure 1C. Memory Maps

memory control (continued)

MEMORY MAPS AFTER CONF 3
1 MP/MC = 1



2 MP/$\overline{MC}$ = 0

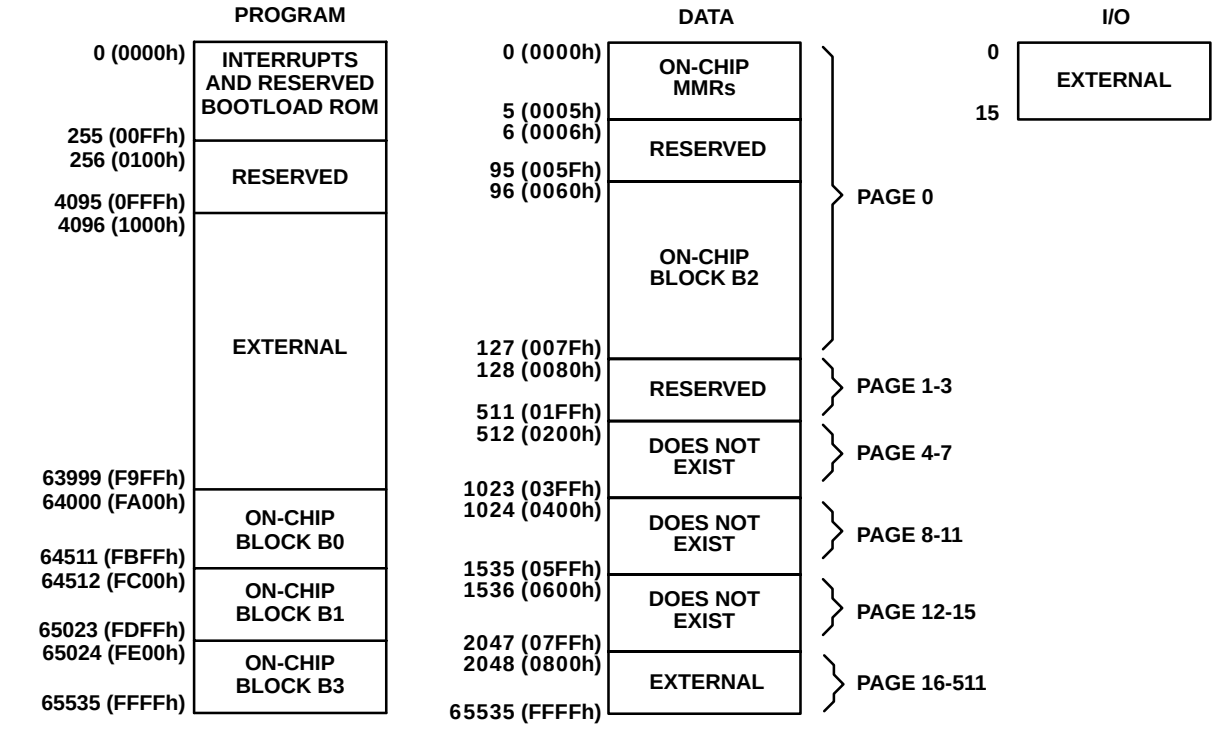


Figure 1D. Memory Maps

interrupts and subroutines

The SMJ320C26 has three external maskable user interrupts $\overline{\text{INT}}$2–$\overline{\text{INT}}$0, available for external devices that interrupt the processor. Internal interrupts are generated by the serial port (RINT and XINT), by the timer (TINT), and by the software interrupt (TRAP) instruction. Interrupts are prioritized with reset ($\overline{\text{RS}}$) having the highest priority and the serial port transmit interrupt (XINT) having the lowest priority. All interrupt locations are on two-words boundaries so that branch instructions can be accommodated in those locations if desired.

A built in mechanism protects multicycle instructions from interrupts. If an interrupt occurs during a multicycle instruction, the interrupt is not processed until the instruction is completed. This mechanism applies both to instructions that are repeated or become multicycle due to the READY signal.

external interface

The SMJ320C26 supports a wide range of system interfacing requirements. Program, data, and I/O address spaces provide interface to memory and I/O, thus maximizing system throughput. I/O design is simplified by having I/O treated the same way as memory. I/O devices are mapped into the I/O address space using the processor's external address and data busses in the same manner as memory-mapped devices. Interface to memory and I/O devices of varying speeds is accomplished by using the READY line. When transactions are made with slower devices, the SMJ320C26 processor waits until the other device completes its function and signals the processor via the READY line, the SMJ320C26 then continues execution.

A serial port provides communication with serial devices, such as codecs, serial A/D converters, and other serial systems. The interface signals are compatible with codecs and many other serial devices with a minimum of external hardware. The serial port may also be used for intercommunication between processors in multiprocessing applications.

The serial port has two memory mapped registers; the data transmit register (DXR) and the data receive register (DRR). Both registers operate in either the byte mode or 16-bit word mode, and may be accessed in the same manner as any other data memory location. Each register has an external clock, a framing signal, and associated shift registers. One method of multiprocessing may be implemented by programming one device to transmit while the others are in the receive mode.

multiprocessing

The flexibility of the SMJ320C26 allows configurations to satisfy a wide range of system requirements. The SMJ320C26 can be used as follows:

- A standalone processor.
- A multiprocessor with devices in parallel.
- A multiprocessor with global memory space.
- A peripheral processor interfaced via processor controlled signals to another device.

For multiprocessing applications, the SMJ320C26 has the capability of allocating global data memory space and communicating with that space via the $\overline{\text{BR}}$ (bus request) and READY control signals. Global memory is data memory shared by more than one processor. Global data memory access must be arbitrated. The 8-bit memory mapped GREG (global memory allocation register) specifies part of the SMJ320C26's data memory as global external memory. The contents of the register determine the size of the global memory space. If the current instruction addresses a location within that space, $\overline{\text{BR}}$ is asserted to request control of the data bus. The length of the memory cycle is controlled by the READY line.

The SMJ320C26 supports DMA (direct memory access) to its external program/data memory using the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals. Another processor can take complete control of the SMJ320C26's external memory by asserting $\overline{\text{HOLD}}$ low. This causes the SMJ320C26 to place its address, data, and control lines in a high impedance state, and assert $\overline{\text{HOLDA}}$.

addressing modes

The SMJ320C26 instruction set provides three memory addressing modes; direct, indirect, and immediate addressing.

Both direct and indirect addressing can be used to access data memory. In direct addressing, seven bits of the instruction word are concatenated with the nine bits of the data memory page pointer to form the 16-bit data memory address. Indirect addressing accesses data memory through the eight auxiliary registers. In immediate addressing, the data is embedded in the instruction word(s).

In direct addressing, the instruction word contains the lower seven bits of the data memory address. This field is concatenated with the nine bits of the data memory page pointer to form the full 16-bit address. Thus, memory is paged in the direct addressing mode with a total of 512 pages, each page containing 128 words.

Eight auxiliary registers (AR0–AR7) provide flexible and powerful indirect addressing. To select a specific auxiliary register, the Auxiliary Register Pointer (ARP) is loaded with a value from 0 through 7 for AR0 through AR7 respectively.

There are seven types of indirect addressing: auto increment, auto decrement, post indexing by either adding or subtracting the contents of AR0, single indirect addressing with no increment or decrement and bit reversal addressing (used in FFTs) with increment or decrement. All operations are performed on the current auxiliary register in the same cycle as the original instruction, followed by an ARP update.

repeat feature

A repeat feature, used with instructions such as multiply/accumulates, block moves, I/O transfers, and table read/writes, allows a single instruction to be executed up to 256 times. The repeat counter (RPTC) is loaded with either a data memory value (RPT instruction) or an immediate value (RPTK instruction). The value of this operand is one less than the number of times that the next instruction is executed. Those instructions that are normally multicycle are pipelined when using the repeat feature, and effectively become single-cycle instructions.

instruction set

The SMJ320C26 microprocessor implements a comprehensive instruction set that supports both numeric intensive signal processing operations as well as general purpose applications, such as multiprocessing and high speed control.

For maximum throughput, the next instruction is prefetched while the current one is being executed. Since the same data lines are used to communicate to external data/program or I/O space, the number of cycles may vary depending upon whether the next data operand fetch is from internal or external program memory. Highest throughput is achieved by maintaining data memory on-chip and using either internal or fast program memory.

Table 1 lists the symbols and abbreviations used in Table 2, the instruction set summary. Table 2 consists primarily of single-cycle, single-word instructions. Infrequently used branch, I-O, and CALL instructions are multicycle. The instruction set summary is arranged according to function and alphabetized within each functional grouping. The symbol (‡) indicates instructions that are not included in the SMJ320C25 instruction set.

instruction set (continued)

Table 1. Instruction Symbols

SYMBOL	MEANING
B	4-bit field specifying a bit code
CM	2-bit field specifying compare mode
D	Data memory address field
FO	Format status bit
M	Addressing mode bit
K	Immediate operand field
PA	Port address (PA0 through PA 15 are predefined assembler symbols equal to 0 through 15 respectively).
PM	2-bit field specifying P register output shift code
R	3-bit operand field specifying auxiliary register
S	4-bit left-shift code
CNF	Internal RAM configuration bits
X	3-bit accumulator left-shift field

instruction set (continued)

Table 2. Instruction Set Summary

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS	Absolute value of accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	1	1
ADD	Add to accumulator with shift	1	0	0	0	0	←	S	→		M	←			D			→
ADDC	Add to accumulator with carry	1	0	1	0	0	0	0	1	1	M	←			D			→
ADDH	Add to high accumulator	1	0	1	0	0	1	0	0	0	M	←			D			→
ADDK	Add to accumulator short immediate	1	1	1	0	0	1	1	0	0		←			D			→
ADDS	Add to low accumulator with sign extension suppressed	1	0	1	0	0	1	0	0	1	M	←			D			→
ADDT†	Add to accumulator with shift specified by T register	1	0	1	0	0	1	0	1	0	M	←			D			→
ADLK†	Add to accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	1	0
AND	AND with accumulator	1	0	1	0	0	1	1	1	0	M	←			D			→
ANDK†	AND immediate with accumulator with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	1	0	0
CMPL†	Complement accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	1	1
LAC	Load accumulator with shift	1	0	0	1	0	←	S	→		M	←			D			→
LACK	Load accumulator immediate short	1	1	1	0	0	1	0	1	0	←				K			→
LACT†	Load accumulator with shift specified by T register	1	0	1	0	0	0	0	1	1	M	←			D			→
LALK†	Load accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	0	1
NEG†	Negate accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	1	1
NORM†	Normalize contents of accumulator	1	1	1	0	0	1	1	1	0	M	X	X	X	0	0	1	0
OR	OR with accumulator	1	0	1	0	0	1	1	0	1	M	←			D			→
ORK†	OR immediate with accumulator with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	1	0	1
ROL	Rotate accumulator left	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0
ROR	Rotate accumulator right	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	0	1
SACH	Store high accumulator with shift	1	0	1	1	0	1	←	X	→	M	←			D			→
SACL	Store low accumulator with shift	1	0	1	1	0	0	←	X	→	M	←			D			→
SBLK†	Subtract from accumulator long immediate with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	0	1	1
SFL†	Shift accumulator left	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	0
SFR†	Shift accumulator right	1	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	1
SUB	Subtract from accumulator with shift	1	0	0	0	1	←	S	→		M	←			D			→
SUBB	Subtract from accumulator with borrow	1	0	1	0	0	1	1	1	1	M	←			D			→
SUBC	Conditional subtract	1	0	1	0	0	0	1	1	1	M	←			D			→
SUBH	Subtract from high accumulator	1	0	1	0	0	0	1	0	0	M	←			D			→
SUBK	Subtract from accumulator short immediate	1	1	1	0	0	1	1	0	1	←				K			→
SUBS	Subtract from low accumulator with sign extension suppressed	1	0	1	0	0	0	1	0	1	M	←			D			→
SUBT†	Subtract from accumulator with shift specified by T register	1	0	1	0	0	0	1	1	0	M	←			D			→
XOR	Exclusive-OR with accumulator	1	0	1	0	0	1	1	0	0	M	←			D			→
XORK†	Exclusive-OR immediate with accumulator with shift	2	1	1	0	1	←	S	→		0	0	0	0	0	1	1	0
ZAC	Zero accumulator	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
ZALH	Zero low accumulator and load high accumulator	1	0	1	0	0	0	0	0	0	M	←			D			→
ZALR	Zero low accumulator and load high accumulator with rounding	1	0	1	1	1	1	0	1	1	M	←			D			→
ZALS	Zero accumulator and load low accumulator with sign extension suppressed	1	0	1	0	0	0	0	0	1	M	←			D			→

† These instructions are not included in the SMJ32010 instruction set.

instruction set (continued)

Table 2. Instruction Set Summary (continued)

AUXILIARY REGISTERS AND DATA PAGE POINTER INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADRK	Add to auxiliary register short immediate	1	0	1	1	1	1	1	1	0	←				D			→
CMPR†	Compare auxiliary register with auxiliary register AR0	1	1	1	0	0	1	1	1	0	0	1	0	1	0	0	◀ CM	▶
LAR	Load auxiliary register	1	0	0	1	1	0	←	R	→	M	←			K			→
LARK	Load auxiliary register short immediate	1	1	1	0	0	0	←	R	→	←				K			→
LARP	Load auxiliary register pointer	1	0	1	0	1	0	1	0	1	M	0	0	0	1	←	R	→
LDP	Load data memory page pointer	1	0	1	0	1	0	0	1	0	M	←						→
LDPK	Load data memory page pointer immediate	1	1	1	0	0	1	0	0	←					D			→
LRLK†	Load auxiliary register long immediate	2	1	1	0	1	0	←	R	→	0	0	0	0	0	0	0	0
MAR	Modify auxiliary register	1	0	1	0	1	0	1	0	1	M	←			DP			→
SAR	Store auxiliary register	1	0	1	1	1	0	←	R	→	M	←			$\overline{D}$			→
SBRK	Subtract from auxiliary register short immediate	1	0	1	1	1	1	1	1	1	←				K			→
T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APAC	Add P register to accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	0	1
LPH†	Load high P register	1	0	1	0	1	0	0	1	1	M	←			D			→
LT	Load T register	1	0	0	1	1	1	1	0	0	M	←			D			→
LTA	Load T register and accumulator previous product	1	0	0	1	1	1	1	0	1	M	←			D			→
LTD	Load T register, accumulate previous product, and move data	1	0	0	1	1	1	1	1	1	M	←			D			→
LTP†	Load T register and store P register in accumulator	1	0	0	1	1	1	1	1	0	M	←			D			→
LTS†	Load T register and subtract previous product	1	0	1	0	1	1	0	1	1	M	←			D			→
MAC†	Multiply and accumulate	2	0	1	0	1	1	1	0	1	M	←			D			→
MACD†	Multiply and accumulate with data move	2	0	1	0	1	1	1	0	0	M	←			D			→
MPY	Multiply (with T register, store product in P register)	1	0	0	1	1	1	0	0	0	M	←			D			→
MPYA	Multiply and accumulate previous product	1	0	0	1	1	1	0	1	0	M	←			D			→
MPYK	Multiply immediate	1	1	0	1	←							K					→
MPYS	Multiply and subtract previous product	1	0	0	1	1	1	0	1	1	M	←			D			→
MPYU	Multiply unsigned	1	1	1	0	0	1	1	1	1	M	←			D			→
PAC	Load accumulator with P register	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	0	0
SPAC	Subtract P register from accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	0	1	1	0
SPH	Store high P register	1	0	1	1	1	1	1	0	1	M	←			D			→
SPL	Store low P register	1	0	1	1	1	1	1	0	0	M	←			D			→
SPM†	Set P register output shift mode	1	1	1	0	0	1	1	1	0	0	0	0	0	1	0	◀ PM	▶
SQRA†	Square and accumulate	1	0	0	1	1	1	0	0	1	M	←			D			→
SQRS†	Square and subtract previous product	1	0	1	0	1	1	0	1	0	M	←			D			→

† These instructions are not included in the SMJ32010 instruction set.

instruction set (continued)

Table 2. Instruction Set Summary (continued)

BRANCH/CALL INSTRUCTIONS																		
MNEMONIC	DESCRITPION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	Branch unconditionally	2	1	1	1	1	1	1	1	1	1	← D →						
BACC†	Branch to address specified by accumulator	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	0	1
BANZ	Branch on auxiliary register not zero	2	1	1	1	1	1	0	1	1	1	← D →						
BBNZ†	Branch if TC bit ≠ 0	2	1	1	1	1	1	0	0	1	1	← D →						
BBZ†	Branch if TC bit = 0	2	1	1	1	1	1	0	0	0	1	← D →						
BC	Branch on carry	2	0	1	0	1	1	1	1	0	1	← D →						
BGEZ	Branch if accumulator ≥ 0	2	1	1	1	1	0	1	0	0	1	← D →						
BGZ	Branch if accumulator > 0	2	1	1	1	1	0	0	0	1	1	← D →						
BIOZ	Branch on I/O status = 0	2	1	1	1	1	1	0	1	0	1	← D →						
BLEZ	Branch if accumulator ≤ 0	2	1	1	1	1	0	0	1	0	1	← D →						
BLZ	Branch if accumulator < 0	2	1	1	1	1	0	0	1	1	1	← D →						
BNC	Branch on no carry	2	0	1	0	1	1	1	1	1	1	← D →						
BNV†	Branch if no overflow	2	1	1	1	1	0	1	1	1	1	← D →						
BNZ	Branch if accumulator ≠ 0	2	1	1	1	1	0	1	0	1	1	← D →						
BV	Branch on overflow	2	1	1	1	1	0	0	0	0	1	← D →						
BZ	Branch if accumulator = 0	2	1	1	1	1	0	1	1	0	1	← D →						
CALA	Call subroutine indirect	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	0	0
CALL	Call subroutine	2	1	1	1	1	1	1	1	0	1	← D →						
RET	Return from subroutine	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1	1	0
I/O AND DATA MEMORY OPERATIONS																		
MNEMONIC	DESCRITPION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLKD	Block move from data memory to data memory	2	1	1	1	1	1	1	0	1	M	← D →						
BLKP†	Block move from program memory to data memory	2	1	1	1	1	1	1	0	0	M	← D →						
DMOV	Data move in data memory	1	0	1	0	1	0	1	1	0	M	← D →						
FORT†	Format serial port registers	1	1	1	0	0	1	1	1	0	0	0	FO	0	1	1	1	
IN	Input data from port	1	1	0	0	0	← PA →				M	← D →						
OUT	Output data to port	1	1	1	1	0	← PA →				M	← D →						
RFSM	Reset serial port frame synchronization mode	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	0
RTXM†	Reset serial port transmit mode	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0
RXF†	Reset external flag	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	0
SFSM	Set serial port frame synchronization mode	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	1
STXM†	Set serial port transmit mode	1	1	1	0	0	1	1	1	0	0	0	1	0	0	0	0	1
SXF†	Set external flag	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1
TBLR	Table read	1	0	1	0	1	1	0	0	0	M	← D →						
TBLW	Table write	1	0	1	0	1	1	0	0	1	M	← D →						

† These instructions are not included in the SMJ32010 instruction set.

instruction set (continued)

Table 2. Instruction Set Summary (concluded)

CONTROL INSTRUCTIONS																		
MNEMONIC	DESCRIPTION	NO. WORDS	INSTRUCTION BIT CODE															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT†	Test bit	1	1	0	0	1	◄	D	►		M	◄			D			►
BITT†	Test bit specified by T register	1	0	1	0	1	0	1	1	1	M	◄			D			►
CONF‡	Configure RAM blocks as Data or program	1	1	1	0	0	1	1	1	0	0	0	1	1	1	1 ◄	CNF	
DINT	Disable interrupt	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
IDLE†	Idle until interrupt	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	1
LST	Load status register ST0	1	0	1	0	1	0	0	0	0	M	◄			D			►
LST1†	Load status register ST1	1	0	1	0	1	0	0	0	1	M	◄			D			►
NOP	No operation	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
POP	Pop top of stack to low accumulator	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	1
POPD†	Pop top of stack to data memory	1	0	1	1	1	1	0	1	0	M	◄			D			►
PSHD†	Push data memory value onto stack	1	0	1	0	1	0	1	0	0	M	◄			D			►
PUSH	Push low accumulator onto stack	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	0	0
RC	Reset carry bit	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	0	0
RHM	Reset hold mode	1	1	1	0	0	1	1	1	0	0	0	1	1	1	0	0	0
ROVM	Reset overflow mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	0
RPT†	Repeat instruction as specified by data memory value	1	0	1	0	0	1	0	1	1	M	◄			D			►
RPTK†	Repeat instruction as specified by immediate value	1	1	1	0	0	1	0	1	1	◄				K			►
RSXM†	Reset sign-extension mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	0
RTC	Reset test/control flag	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	0
SC	Set carry bit	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	0	1
SHM	Set hold mode	1	1	1	0	0	1	1	1	0	0	0	1	1	1	0	0	1
SOVM	Set overflow mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	1
SST	Store status register ST0	1	0	1	1	1	1	0	0	0	M	◄			D			►
SST1†	Store status register ST1	1	0	1	1	1	1	0	0	1	M	◄			D			►
SSXM†	Set sign-extension mode	1	1	1	0	0	1	1	1	0	0	0	0	0	0	1	1	1
STC	Set test/control flag	1	1	1	0	0	1	1	1	0	0	0	1	1	0	0	1	1
TRAP†	Software interrupt	1	1	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0

† These instructions are not included in the SMJ32010 instruction set.
‡ This instruction replaces CNFD and CNFP in the SMJ320C25 instruction set.

development support

Together, Texas Instruments and its authorized third-party suppliers offer an extensive line of development support products to assist the user in all aspects of TMS320 second-generation-based design and development. These products range from development and application software to complete hardware development and evaluation systems. Table 3 lists the development support products for the second-generation TMS320 devices.

System development may begin with the use of the simulator, Software Development System (SWDS), or emulator (XDS) along with an assembler/linker. These tools give the TMS320 user various means of evaluation, from software simulation of the second-generation TMS320s (simulator) to full-speed in-circuit emulation with hardware and software breakpoint trace and timing capabilities (XDS).

Software and hardware can be developed simultaneously by using the macro assembler/linker, C compiler, and simulator for software development, the XDS for hardware development, and the Software Development System for both software development and limited hardware development.

Many third-party vendors offer additional development support for the second-generation TMS320s, including assembler/linkers, simulators, high-level languages, applications software, algorithm development tools, applications boards, software development boards, and in-circuit emulators. Refer to the *TMS320 Family Development Support Reference Guide* (SPRU011A) for further information about TMS320 development support products offered by both Texas Instruments and its third-party suppliers.

Additional support for the TMS320 products consists of an extensive library of product and applications documentation. Three-day DSP design workshops are offered by the TI Regional Technology Centers (RTCs). These workshops provide insight into the architecture and the instruction set of the second-generation TMS320s as well as hands-on training with the TMS320 development tools. When technical questions arise regarding the TMS320 family, contact the Texas Instruments TMS320 Hotline at (713) 274–2320. Or, keep informed on the latest TI and third-party development support tools by accessing the DSP Bulletin Board Service (BBS) at (713) 274–2323. The BBS serves 2400-, 1200-, and 300-bps modems. Also, TMS320 application source code may be downloaded from the BBS.

Table 3 gives a complete list of SMJ320C26 software and hardware development tools.

development support (continued)

Table 3. Software and Hardware Support

MACRO ASSEMBLER/LINKER		
HOST COMPUTER	**OPERATING SYSTEMS**	**PART NUMBER**
DEC VAX	VMS	TMDS3242250-08
IBM PC	MS/PS DOS	TMDS3242850-02
VAX	ULTRIX	TMDS3242260-08
SUN 3	UNIX	TMDS3242550-08
C COMPILER AND MACRO ASSEMBLER/LINKER		
HOST COMPUTER	**OPERATING SYSTEMS**	**PART NUMBER**
DEC VAX	VMS	TMDS3242255-08
IBM PC	MS/PC DOS	TMDS3242855-02
VAX	ULTRIX	TMDS3242265-08
SUN 3	UNIX	TMDS3242555-08
SIMULATOR		
HOST COMPUTER	**OPERATING SYSTEMS**	**PART NUMBER**
DEC VAX	VMS	TMDS3242251-08
IBM PC	MS/PC DOS	TMDS3242851-02
EMULATOR		
MODEL	**POWER SUPPLY**	**PART NUMBER**
XDS/22	INCLUDED	TMDS3262292
SOFTWARE DEVELOPMENT SYSTEM ON PC		
HOST COMPUTER	**OPERATING SYSTEMS**	**PART NUMBER**
IBM PC	MS/PC DOS	TMDX3268828
IBM PC	MS/PC DOS	TMDX3268821†

† Includes assembler/linker

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}‡ . . . . . – 0.3 V to 7 V
Input voltage range . . . . . – 0.3 V to 7 V
Output voltage range . . . . . – 0.3 V to 7 V
Continuous power dissipation . . . . . 1.0 W
Storage temperature range . . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to V_{SS}.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	D15–D0, FSX	2.2			V
		CLKIN, CLKR, CLKX	3.50			
		All others	3.00			
V_{IL}	Low-level input voltage	D15–D0, FSX, CLKIN, CLKR, CLKX			0.8	µA
		All others			0.7	
I_{OH}	High-level output current				300	µA
I_{OL}	Low-level output current				2	mA
T_A	Minimum operating free-air temperature		–55			°C
T_C	Maximum operating case temperature				125	°C

electrical characteristics over specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4	3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX		0.3	0.6	V
I_{OZ}	High-impedance-state output leakage current		V_{CC} = MAX			± 20	µA
I_I	Input current		V_I = V_{SS} to V_{CC}			± 10	µA
I_{CC}	Supply current	Normal	V_{CC} = MAX, f_x = MAX			185	mA
		Idle/$\overline{\text{HOLD}}$				100	
C_I	Input capacitance				15		pF
C_O	Output capacitance				15		pF

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

CLOCK CHARACTERISTICS AND TIMING

The SMJ320C26 can use either its internal oscillator or an external frequency source for a clock.

internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 2). The frequency of CLKOUT1 is one-fourth the crystal fundamental frequency. The crystal should be either fundamental or overtone mode, and parallel resonant, with an effective series resistance of 30 Ω, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF. Note that overtone crystals require an additional tuned LC circuit (see the application report, *Hardware Interfacing to the TMS320C25*).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_X Input clock frequency†	T_A = –55°C MIN	6.7		40.0	MHz
C1, C2	T_C = 125°C MAX		10		pF

† This parameter is not production tested.

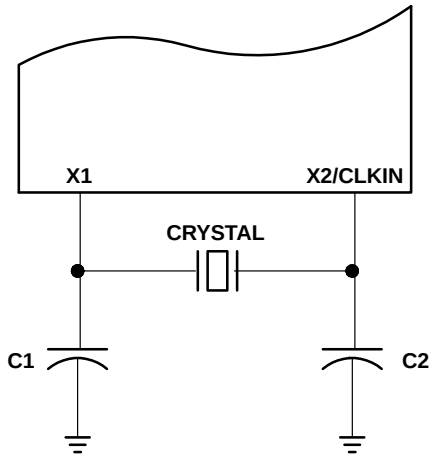


Figure 1. Internal Clock Option

external clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(C)}$	CLKOUT1/CLKOUT2 cycle time	100		600	ns
$t_{d(CIH-C)}$	CLKIN high to CLKOUT1/CLKOUT2/$\overline{STRB}$ high/low	5		32	ns
$t_{f(C)}$	CLKOUT1/CLKOUT2/$\overline{STRB}$ fall time			5	ns
$t_{r(C)}$	CLKOUT1/CLKOUT2/$\overline{STRB}$ rise time			5	ns
$t_{w(CL)}$	CLKOUT1/CLKOUT2 low pulse duration	2Q–8	2Q	2Q+8	ns
$t_{w(CH)}$	CLKOUT1/CLKOUT2 high pulse duration	2Q–8	2Q	2Q+8	ns
$t_{d(C1-C2)}$	CLKOUT1 high to CLKOUT2 low, CLKOUT2 high to CLKOUT1 high, etc.	Q–6	Q	Q+6	ns

† This parameter is not production tested.

NOTE 1: $Q = 1/4t_{c(C)}$

timing requirements over recommended operating conditions (see Note 1)

		MIN	MAX	UNIT
$t_{c(CI)}$	CLKIN cycle time	25	150	ns
$t_{w(CIL)}$	CLKIN low pulse duration, $t_{c(C)}$ = 25 ns (see Note 2)	10	15	ns
$t_{w(CIH)}$	CLKIN high pulse duration, $t_{c(CI)}$ = 25 ns (see Note 2)	10	15	ns
$t_{su(S)}$	$\overline{\text{SYNC}}$ setup time before CLKIN low	5	Q–5	ns
$t_{h(S)}$	$\overline{\text{SYNC}}$ hold time from CLKIN low	8		ns

NOTES: 1. $Q = 1/4t_{c(C)}$
2. CLKIN duty cycle $[t_{r(CI)} + t_{w(CIH)}]/t_{c(CI)}$ must be within 40-60%. CLKIN rise and fall times must be less than 5 ns.

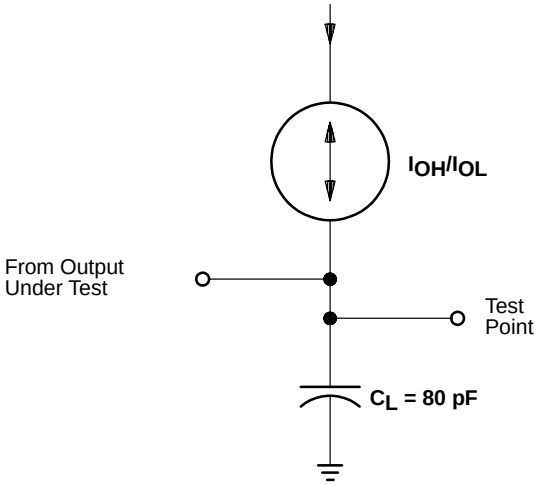
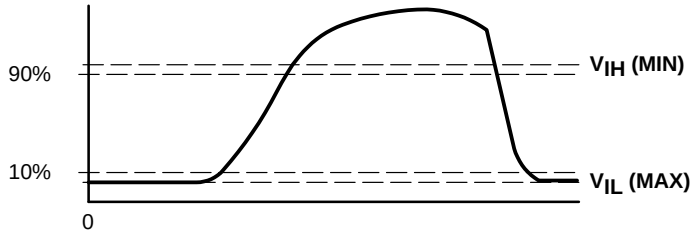
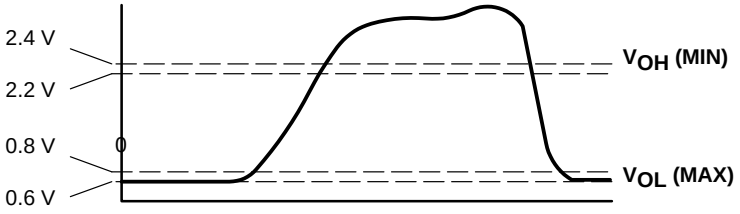


Figure 2. Test Load Circuit



(a) Input



(b) Outputs

Figure 3. Voltage Reference Levels

MEMORY AND PERIPHERAL INTERFACE TIMING

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(C1-S)}$	$\overline{STRB}$ from CLKOUT1 (if $\overline{STRB}$ is present)	Q–6	Q	Q+6	ns
$t_{d(C2-S)}$	CLKOUT2 to $\overline{STRB}$ (if $\overline{STRB}$ is present)	–6	0	6	ns
$t_{su(A)}$	Address setup time before $\overline{STRB}$ low (see Note 3)	Q–12			ns
$t_{h(A)}$	Address hold time after $\overline{STRB}$ high (see Note 3)	Q–8			ns
$t_{w(SL)}$	$\overline{STRB}$ low pulse duration (no wait states, see Note 4)	2Q–5	2Q	2Q+5	ns
$t_{w(SH)}$	$\overline{STRB}$ high pulse duration (between consecutive cycles, see Note 4)		2Q		ns
$t_{su(D)W}$	Data write setup time before $\overline{STRB}$ high (no wait states)	2Q–20			ns
$t_{h(D)W}$	Data write hold time from $\overline{STRB}$ high	Q–10	Q		ns
$t_{en(D)}$	Data bus starts being driven after $\overline{STRB}$ low (write cycle)	0†			ns
$t_{dis(D)}$	Data bus three-state after $\overline{STRB}$ high (write cycle)		Q	Q+15†	ns
$t_{d(MSC)}$	$\overline{MSC}$ valid from CLKOUT1	– 10†	0	10	ns

† This parameter is not production tested.

timing requirements over recommended operating conditions (see Note 1)

		MIN	MAX	UNIT
$t_{a(A)}$	Read data access time from address time (read cycle) (see Notes 3 and 5)		3Q–40	ns
$t_{su(D)R}$	Data read setup time before $\overline{STRB}$ high	23		ns
$t_{h(D)R}$	Data read hold time from $\overline{STRB}$ high	0		ns
$t_{d(SL-R)}$	READY valid after $\overline{STRB}$ low (no wait states)		Q–22	ns
$t_{d(C2H-R)}$	READY valid after CLKOUT2 high		Q – 22†	ns
$t_{h(SL-R)}$	READY hold time after $\overline{STRB}$ low (no wait states)	Q+3		ns
$t_{h(C2H-R)}$	READY hold after CLKOUT2 high	Q + 3†		ns
$t_{d(M-R)}$	READY valid after $\overline{MSC}$ valid		2Q –25†	ns
$t_{h(M-R)}$	READY hold time after $\overline{MSC}$ valid	0†		ns

† This parameter is not production tested.

$\overline{RS}$, $\overline{INT}$, $\overline{BIO}$, AND XF TIMING

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(RS)}$	CLKOUT1 low to reset state entered			22†	ns
$t_{d(IACK)}$	CLKOUT1 to $\overline{IACK}$ valid	– 8†	0	8	ns
$t_{d(XF)}$	XF valid before falling edge of $\overline{STRB}$	Q–12			ns

timing requirements over recommended operating conditions (see Note 1)

		MIN	MAX	UNIT
$t_{su(IN)}$	$\overline{INT}/\overline{BIO}/\overline{RS}$ setup before CLKOUT1 high (see Note 6)	32		ns
$t_{h(IN)}$	$\overline{INT}/\overline{BIO}/\overline{RS}$ hold after CLKOUT1 high (see Note 6)	0		ns
$t_{w(IN)}$	$\overline{NT}/\overline{BIO}$ low pulse duration	$t_{c(C)}$		ns
$t_{w(RS)}$	$\overline{RS}$ low pulse duration	$3t_{c(C)}$		ns

NOTES: 1. $Q = 1/4t_{c(C)}$

3. A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as “address.”
4. Delays between CLKOUT1/CLKOUT2 edges and $\overline{STRB}$ edges track each other, resulting in $t_{w(SL)}$ and $t_{w(SH)}$ being 2Q with no wait states.
5. Read data access time is defined as $t_{a(A)} = t_{su(A)} + t_{w(SL)} - t_{su(D)R}$.
6. $\overline{RS}$, $\overline{INT}$, and $\overline{BIO}$ are asynchronous inputs and can occur at any time during a clock cycle. However, if the specified setup time is met, the exact sequence shown in the timing diagram will occur. $\overline{INT}/\overline{BIO}$ fall time must be less than 8 ns.

$\overline{\text{HOLD}}$ TIMING

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(C1L-AL)}$	$\overline{\text{HOLDA}}$ low after CLKOUT1 low	–1†		10	ns
$t_{dis(AL-A)}$	$\overline{\text{HOLDA}}$ low to address three-state		0		ns
$t_{dis(C1L-A)}$	Address three-state after CLKOUT1 low ($\overline{\text{HOLD}}$ mode) (see Note 7)			20†	ns
$t_{d(HH-AH)}$	$\overline{\text{HOLD}}$ high to $\overline{\text{HOLDA}}$ high			25	ns
$t_{en(A-C1L)}$	Address driven before CLKOUT1 low ($\overline{\text{HOLD}}$ mode) (see Note 7)			8†	ns

† This parameter is not production tested.

timing requirements over recommended operating conditions (see Note 1)

		MIN	MAX	UNIT
$t_{d(C2H-H)}$	$\overline{\text{HOLD}}$ valid after CLKOUT2 high		Q–24	ns

NOTES: 1. $Q = 1/4t_{c(C)}$

7. A15–A0, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ timings are all included in timings referenced as “address.”

SERIAL PORT TIMING

switching characteristics over recommended operating conditions (see Note 1)

PARAMETER		MIN	MAX	UNIT
$t_{d(CH-DX)}$	DX valid after CLKX rising edge (see Note 8)		80	ns
$t_{d(FL-DX)}$	DX valid after FSX falling edge (TXM = 0) (see Note 8)		45	ns
$t_{d(CH-FS)}$	FSX valid after CLKX rising edge (TXM = 1)		45	ns

timing requirements over recommended operating conditions (see Note 1)

		MIN	MAX	UNIT
f_{sx}	Serial port frequency	1.25	5,000	kHz
$t_{c(SCK)}$	Serial port clock (CLKX/CLKR) cycle time	200	800,000	ns
$t_{w(SCK)}$	Serial port clock (CLKX/CLKR) low pulse duration (see Note 9)	80		ns
$t_{w(SCK)}$	Serial port clock (CLKX/CLKR) high pulse duration (see Note 9)	80		ns
$t_{su(FS)}$	FSX/FSR setup time before CLKX/CLKR falling edge (TXM = 0)	18		ns
$t_{h(FS)}$	FSX/FSR hold time after CLKX/CLKR falling edge (TXM = 0)	20		ns
$t_{su(DR)}$	DR setup time before CLKR falling edge	10		ns
$t_{h(DR)}$	DR hold time after CLKR falling edge	20		ns

NOTES: 1. $Q = 1/4t_{c(C)}$
8. The last occurrence of FSX falling and CLKX rising.
9. The duty cycle of the serial port clock must be within 40–60%. Serial port clock (CLKX/CLKR) rise and fall times must be less than 25 ns.

PARAMETER MEASUREMENT INFORMATION

Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.2 volts unless otherwise noted.

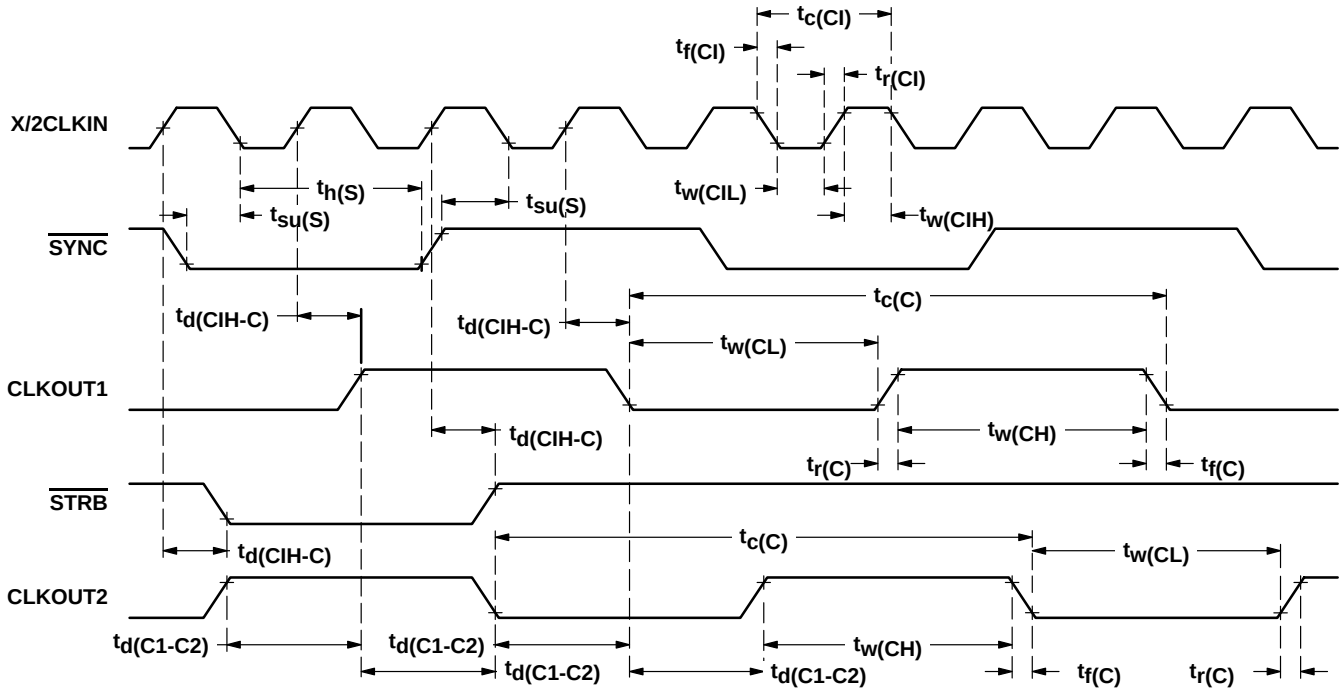


Figure 4. Clock Timing

PARAMETER MEASUREMENT INFORMATION

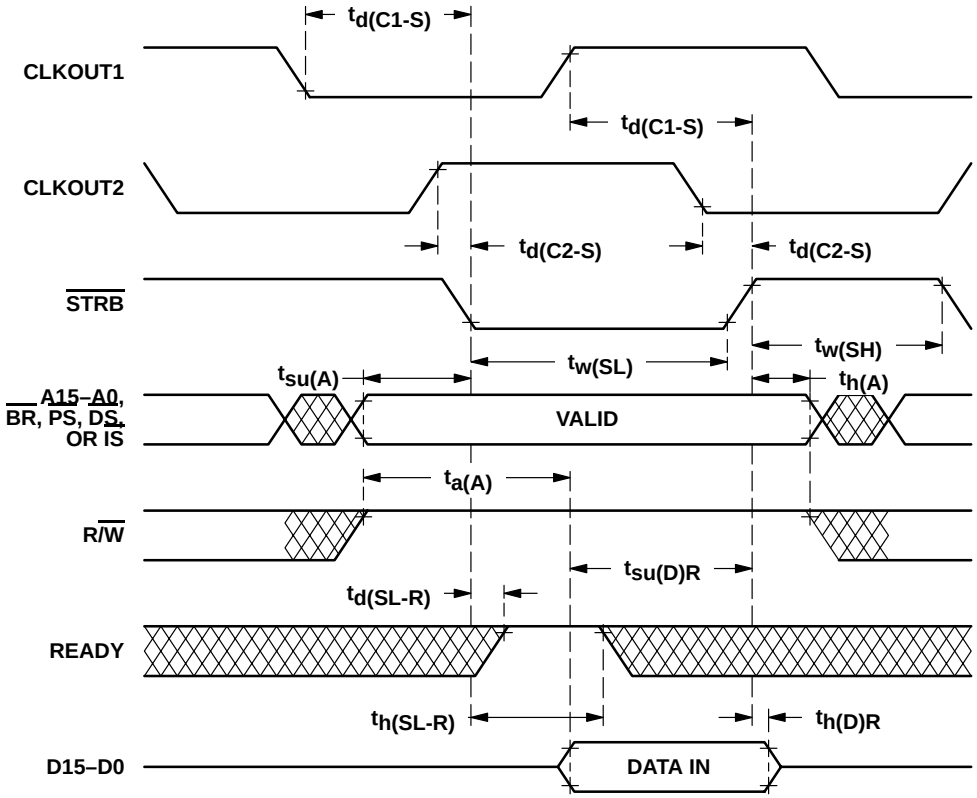


Figure 5. Memory Read Timing

PARAMETER MEASUREMENT INFORMATION

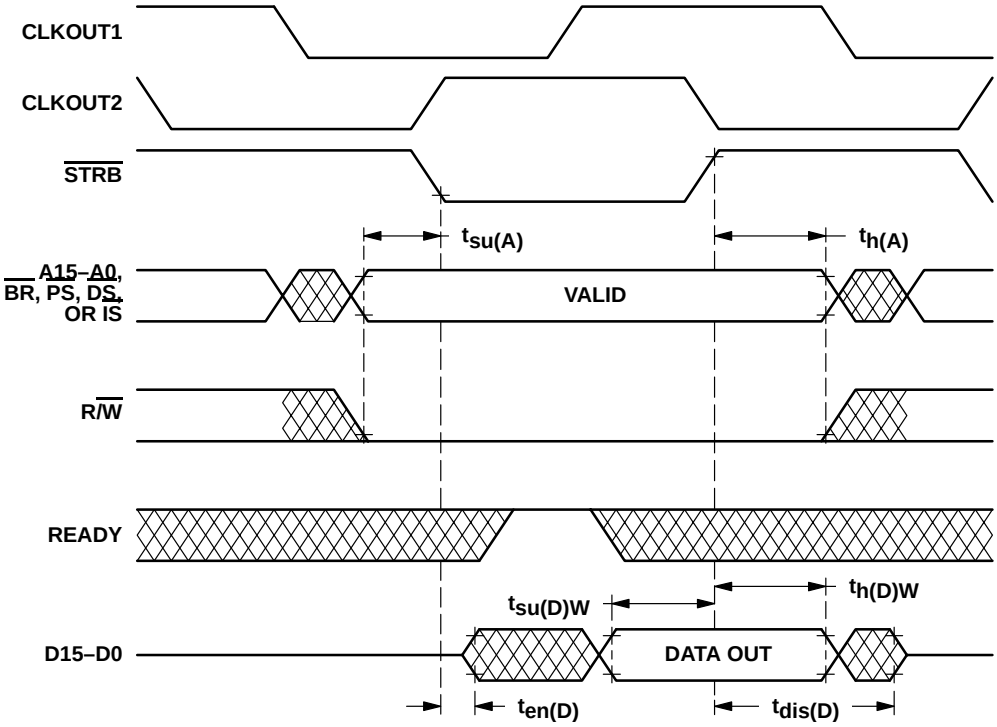


Figure 6. Memory Write Timing

PARAMETER MEASUREMENT INFORMATION

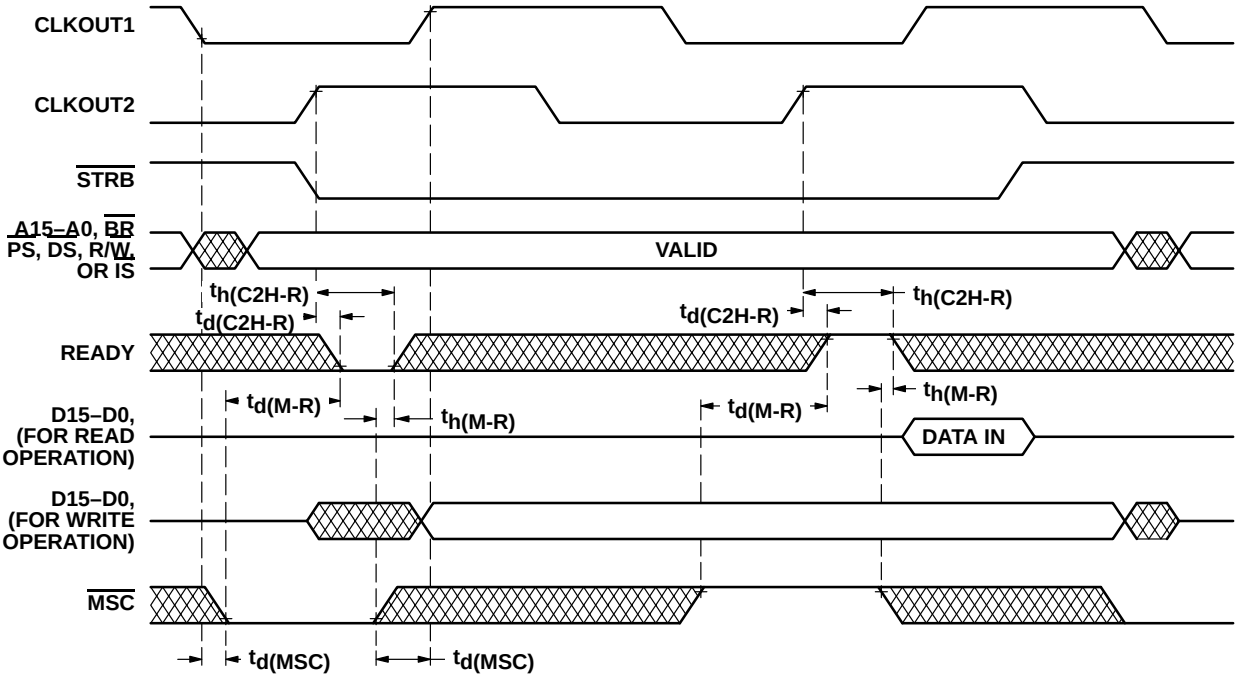
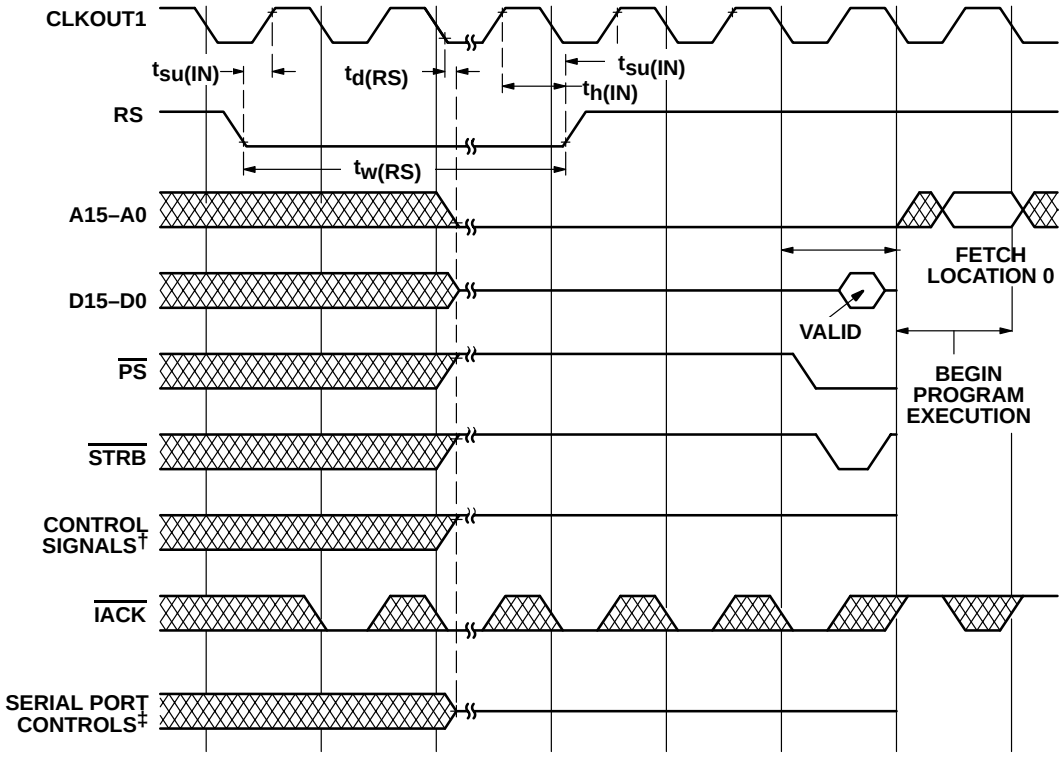


Figure 7. One Wait-State Memory Access Timing

PARAMETER MEASUREMENT INFORMATION



† Control signals are $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and XF.
‡ Serial port controls are DX and FSX.

Figure 8. Reset Timing

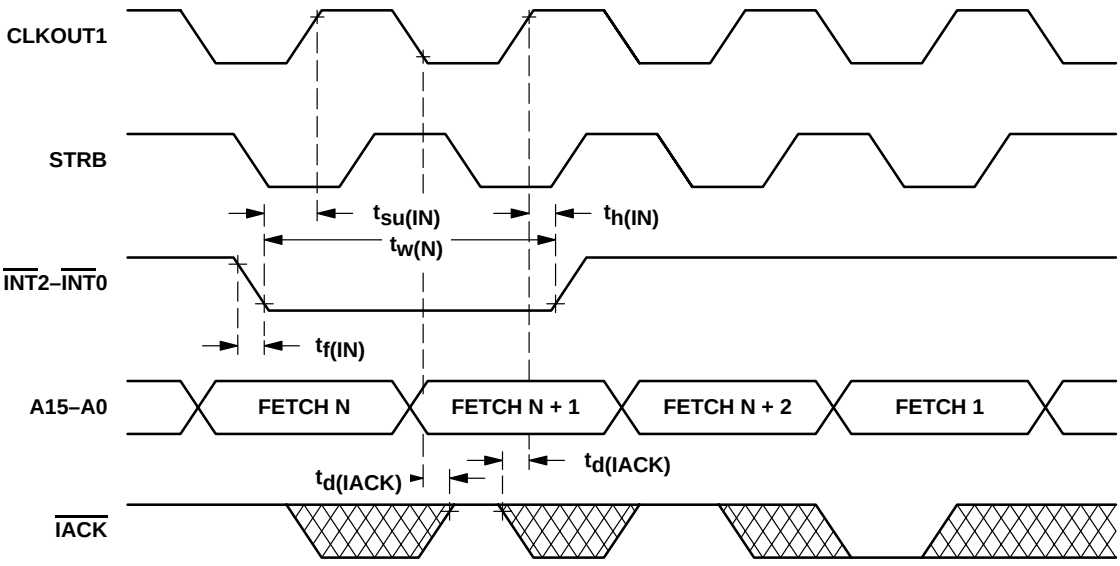


Figure 9. Interrupt Timing

PARAMETER MEASUREMENT INFORMATION

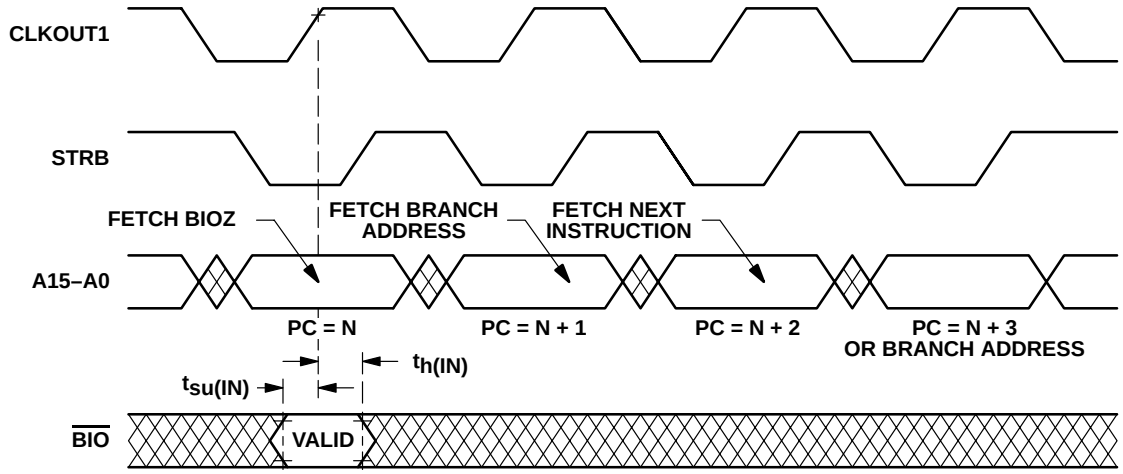


Figure 10. $\overline{\text{BIO}}$ Timing

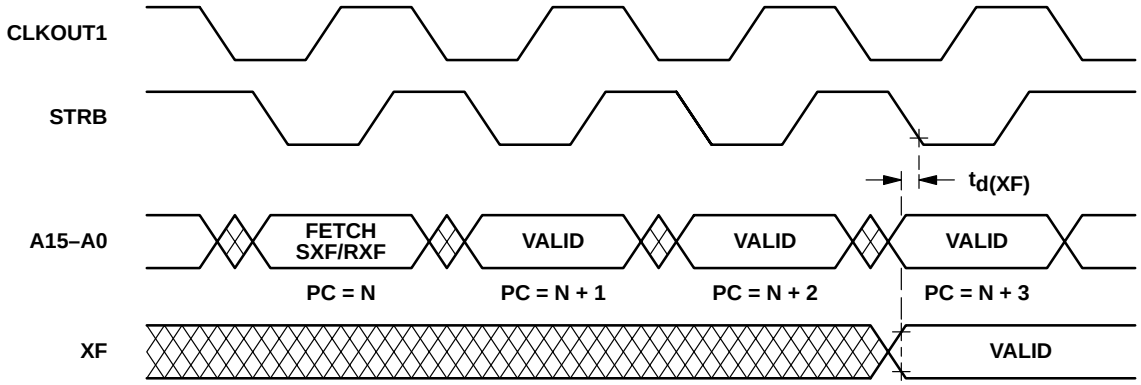
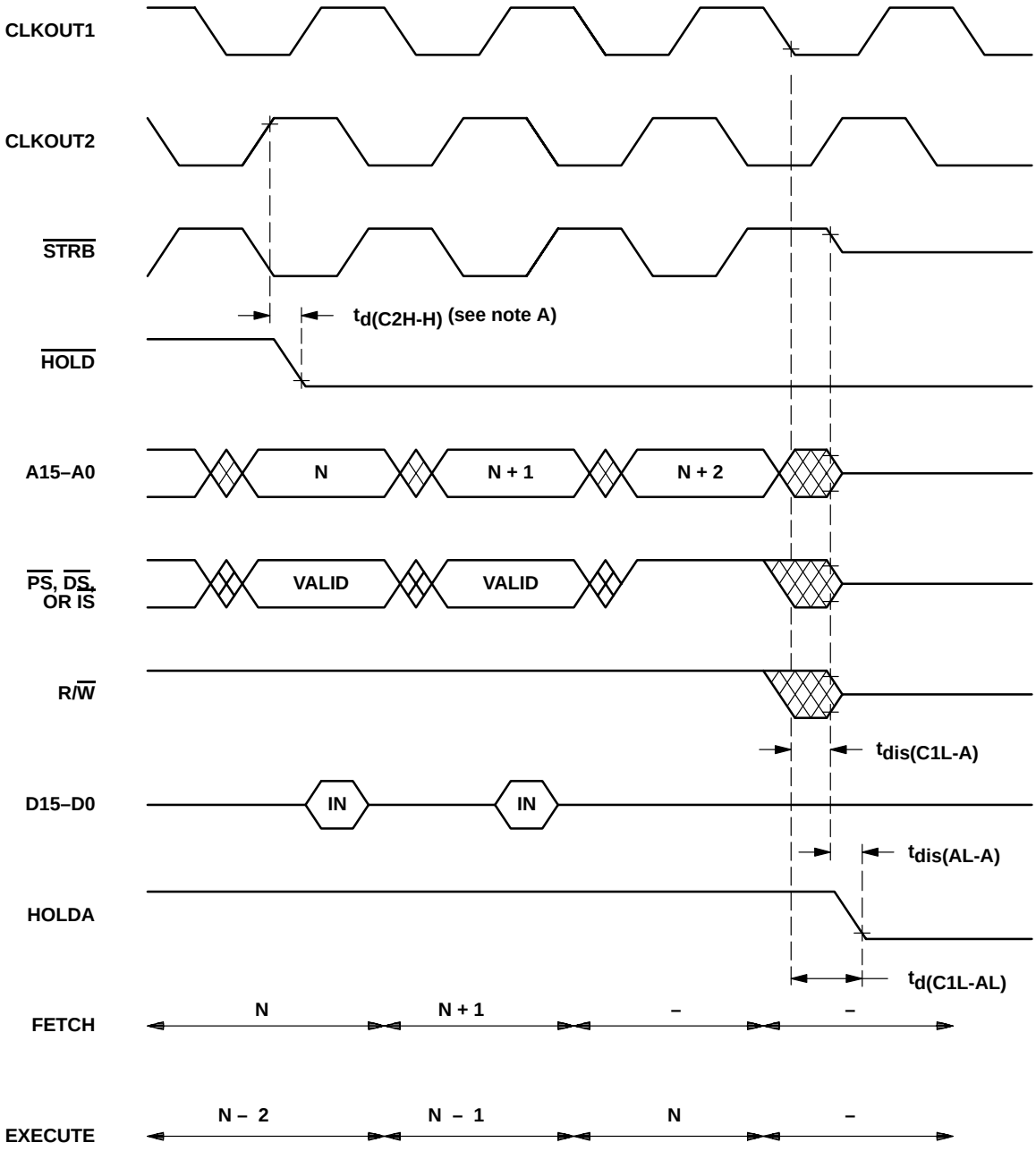


Figure 11. External Flag Timing

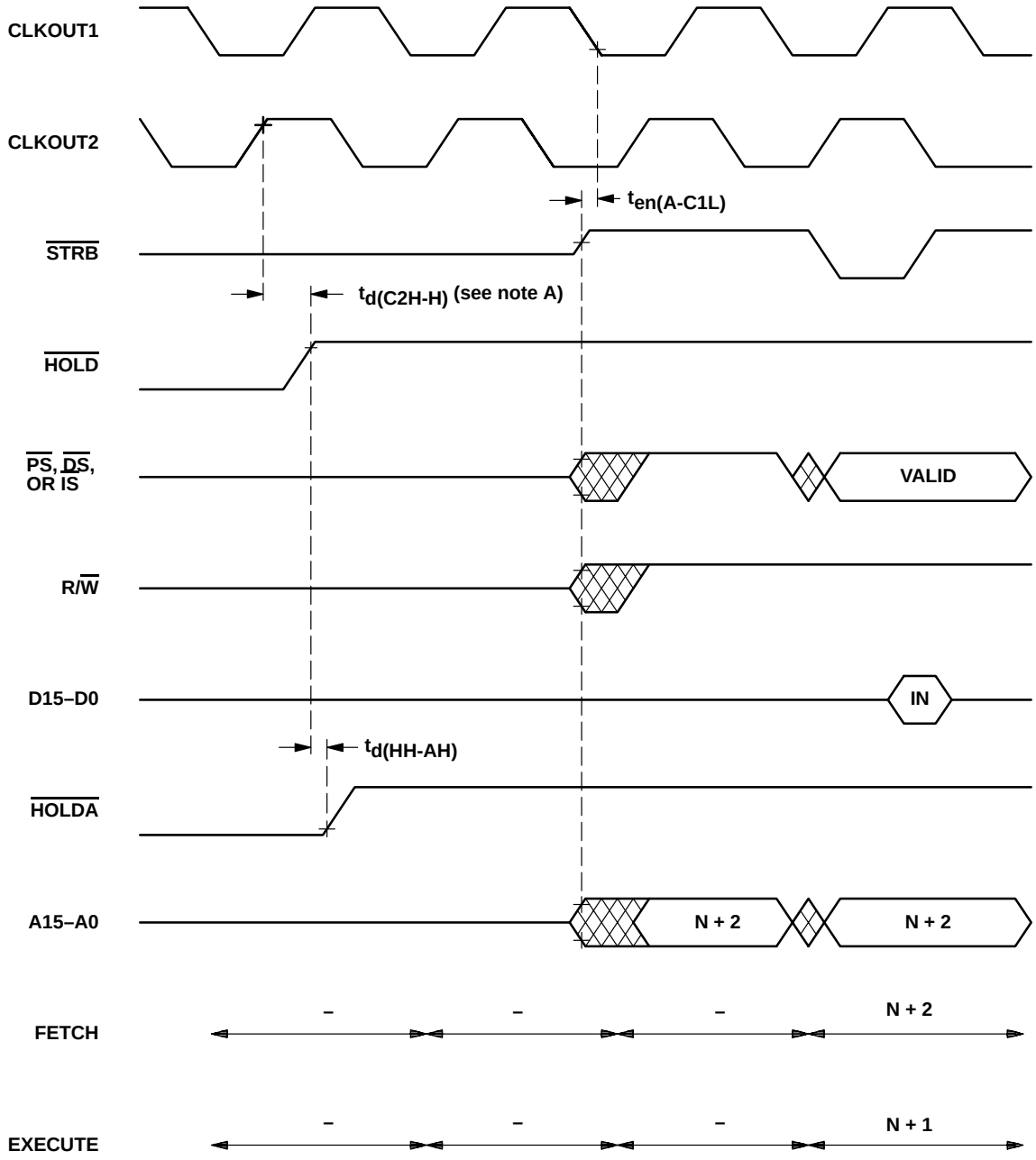
PARAMETER MEASUREMENT INFORMATION



NOTE A: $\overline{\text{HOLD}}$ is an asynchronous input that can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLKOUT2 cycle will occur.

Figure 12. $\overline{\text{HOLD}}$ Timing (Part A)

PARAMETER MEASUREMENT INFORMATION



NOTE A: HOLD is an asynchronous input that can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLKOUT2 cycle will occur.

Figure 13. HOLD Timing (Part B)

PARAMETER MEASUREMENT INFORMATION

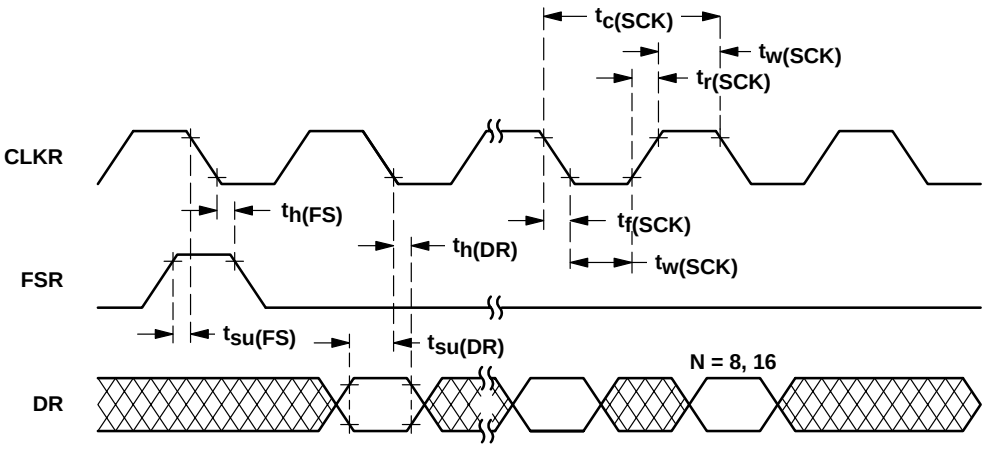


Figure 14. Serial Port Receive Timing

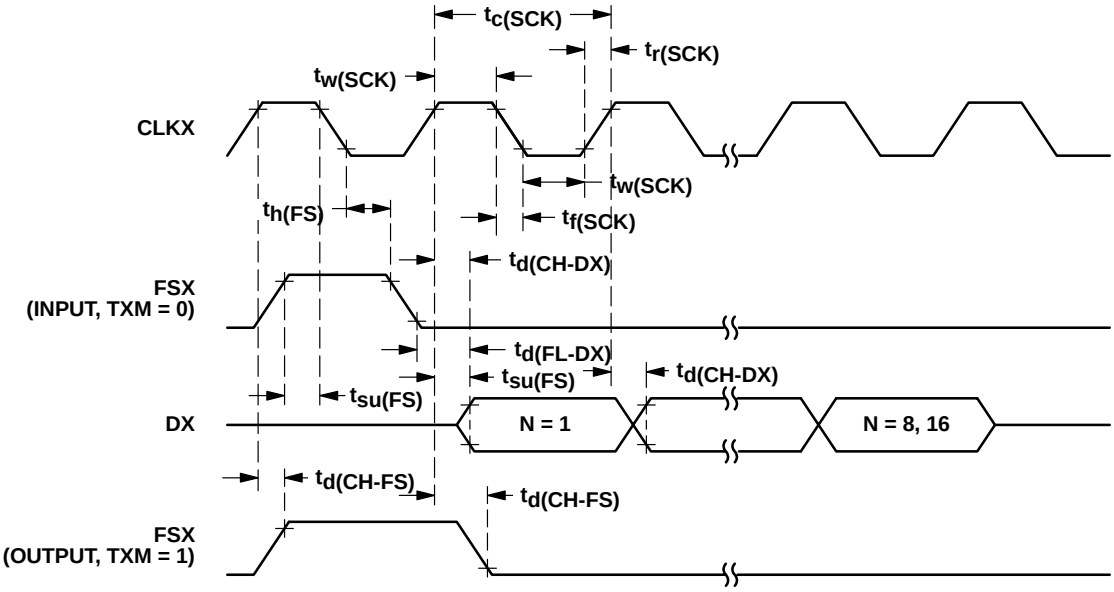


Figure 15. Serial Port Transmit Timing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-8861903XA	OBSOLETE	CPGA	GB	68		TBD	Call TI	Call TI	
5962-8861903YA	OBSOLETE	LCCC	FD	68		TBD	Call TI	Call TI	
SMJ320C26BFDM	OBSOLETE	LCCC	FD	68		TBD	Call TI	Call TI	
SMJ320C26BGBM	OBSOLETE	CPGA	GB	68		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF SMJ320C26B :

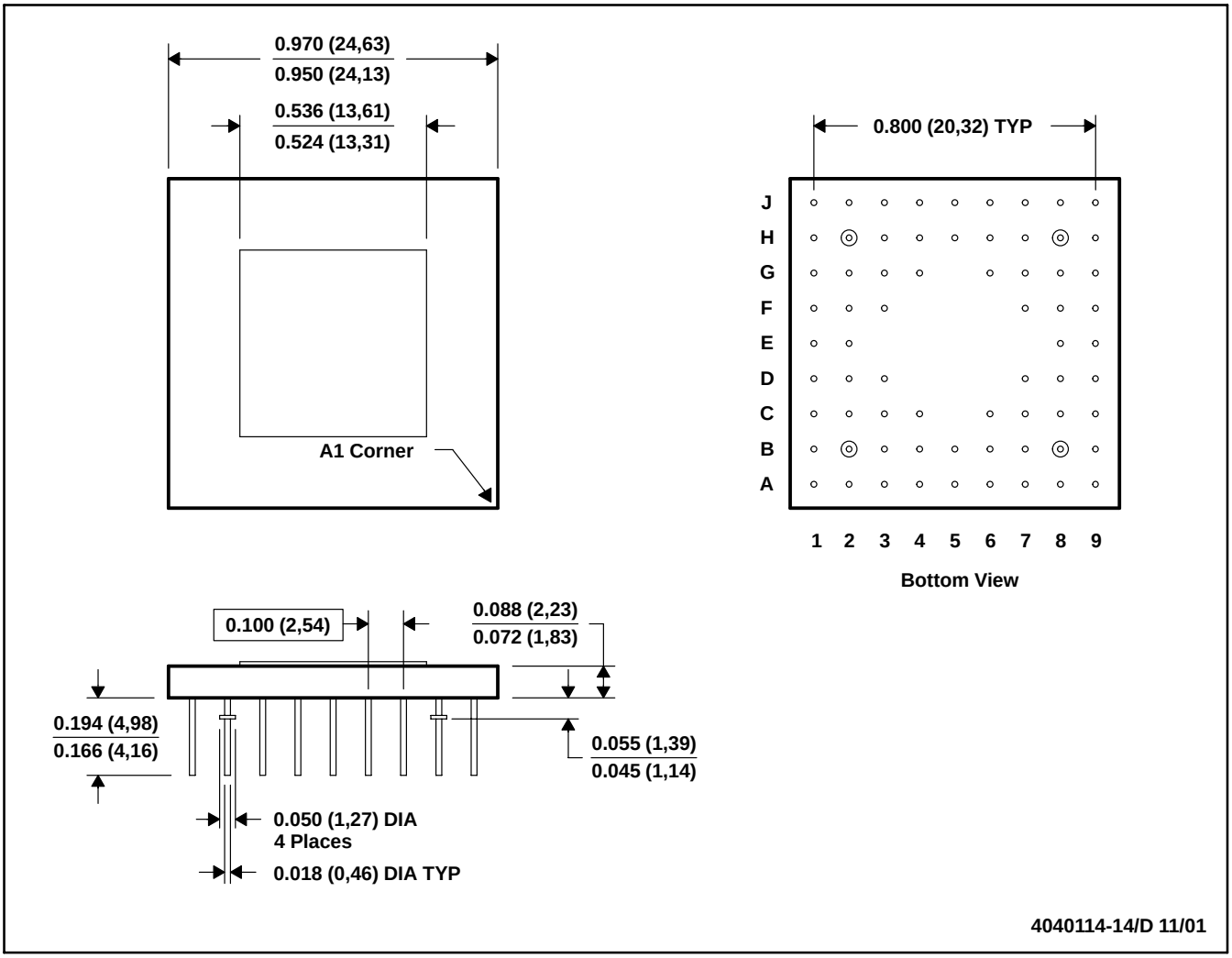
- Catalog: TMS320C26B

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

MCPG023A – OCTOBER 1997 – REVISED DECEMBER 2001

GB (S-CPGA-P68) **CERAMIC PIN GRID ARRAY**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending vendor.
D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edges of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold plated or solder dipped.
G. Falls within MIL STD 1835 CMGA1-PN, CMGA13-PN and JEDEC MO-067 AA, MO-066 AA respectively

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