

## features

- Low Dropout Voltage Regulator, 1.2-V
- 150-mA Load Current Capability
- Power Okay (POK) Function
- Load Independent, Low Ground Current, 150- $\mu$ A
- Current Limiting
- Thermal Shutdown
- Low Sleep State Current (Off Mode)
- Fast Transient Response
- Low Variation Due to Load and Line Regulation
- Output Stable With Low ESR Capacitors
- TTL Logic Controlled Enable Input

## applications

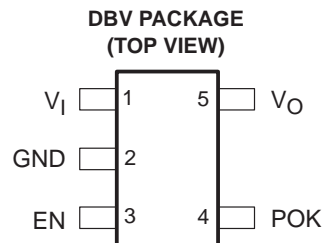
- Processor Powerup Sequencing
- Palmtop Computers, Laptops, and Notebooks

## description

The SN105125 is a low dropout voltage regulator with an output tolerance of  $\pm 2\%$  over the operating range. The device is optimized for low noise applications and has a low quiescent current (enable  $< 0.8$  V). The device has a low dropout voltage at full load (150 mA). The power okay function monitors the output voltage and indicates when an error occurs in the system (active low). In the event of an output fault such as overcurrent, thermal shutdown, or dropout, the power okay output is pulled low (open drain).

The SN105125 has a fast transient response recovery capability in the event of load transition from heavy load to light load. The device also minimizes overshoot during this condition. During power down, the output capacitor and load are de-energized through the internal active shutdown clamp, which is turned on when the device is disabled.

The SN105125 requires a small output capacitor for stability with low ESR. An input capacitor is not required unless the bulk ac capacitor is placed away from the device or the power supply is a battery. In this situation, a 1- $\mu$ F capacitor is recommended for the application. Low ESR ceramic capacitors may be used with the device to reduce board space in power applications, a key concern in hand-held wireless devices.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

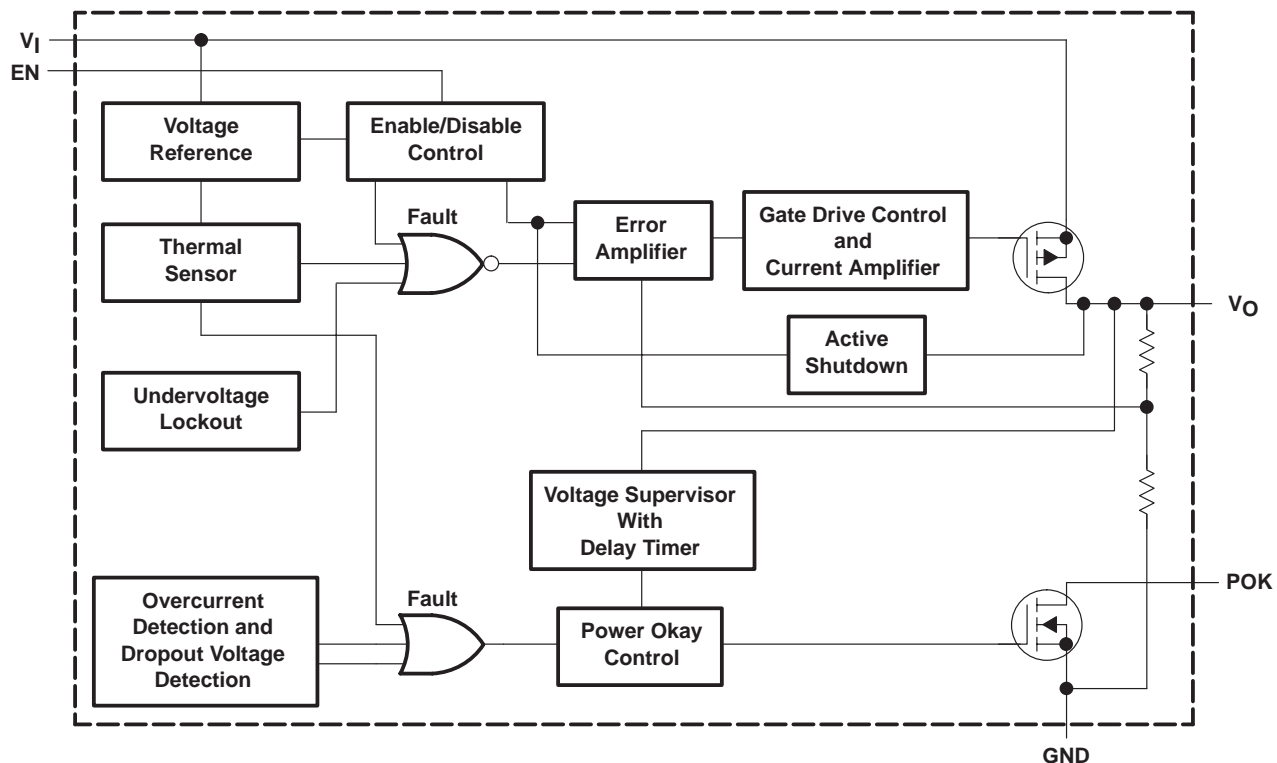
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# SN105125 150-mA LOW DROPOUT REGULATOR WITH POK

SLVS418 – JANUARY 2002

## functional block diagram



## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	3	I	Enable/shutdown input (active high)
GND	2	I	Ground
POK	4	I	Power okay indicator
V <sub>I</sub>	1	I	Input supply voltage
V <sub>O</sub>	5	O	Output voltage

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Main input voltage range, $V_I$ (see Notes 1 and 2) .....	0 V to 7 V
Enable input voltage range, $V_{(EN)}$ (see Notes 1 and 2) .....	0 V – $V_I$
Power okay output voltage range $V_{(POK)}$ , (see Notes 1 and 2) .....	0 V – $V_I$
Regulated output current limit, $I_O$ .....	400 mA
Continuous power dissipation, $P_D$ , $T_A = 25^\circ\text{C}$ .....	0.5 W
Electrostatic discharge susceptibility, $V_{(HBMESD)}$ , (see Note 3) .....	2 kV
Junction temperature, $T_J$ , .....	150°C
Storage temperature range, $T_{Stg}$ .....	–55°C to 150°C
Lead temperature (soldering, 10 sec) .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.  
 2. Absolute negative voltage on these terminals should not go below –0.5 V.  
 3. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal. Devices are ESD sensitive. Handling precautions are recommended.

**recommended operating conditions**

	MIN	TYP	MAX	UNIT
Main input voltage, $V_I$ (see Notes 1 and 2)	3		5.25	V
Enable input voltage, $V_{(EN)}$ (see Notes 1 and 2)	0		$V_I$	V
Power okay voltage, $V_{(POK)}$ (see Notes 1 and 2)	0		$V_I$	V
Operating ambient temperature, $T_A$	0		70	°C

- NOTES: 1. All voltage values are with respect to GND.  
 2. Absolute negative voltage on these terminals should not go below –0.5 V.

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electrical characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_I = 5\text{ V}$ ,  $V_{(EN)} = V_I$ ,  $I_O = 100\ \mu\text{A}$ ,  $C_L = 1\ \mu\text{F}$  (unless otherwise noted)

### regulator $V_O$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_O$	Output voltage	$I_O = 25\ \text{mA}$		1.2		V
	Output voltage accuracy	$I_O = 0$	-1%		1%	
		$I_O = 50\ \text{mA}$ , $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ (see Note 4)	-2%		2%	
$I_Q$	Quiescent supply current	$V_{(EN)} \leq 0.8\ \text{V}$		1		$\mu\text{A}$
$I_{(GND)}$	Ground terminal current (see Note 5)	$I_O = 0$		150		$\mu\text{A}$
		$I_O = 150\ \text{mA}$		150		
$I_L$	Output load current		150			mA
$I_{(Limit)}$	Output current limit	$V_O = 0$	160	300		mA
$\Delta V_{(LNR)}$	Line regulation	$V_I = 3\ \text{V}$ to $5.25\ \text{V}$		10		mV
$\Delta V_{(LDR)}$	Load regulation	$I_O = 0.1\ \text{mA}$ to $150\ \text{mA}$ , See Note 6		2%	3%	
$V_I - V_O$	Dropout voltage	$I_O = 100\ \mu\text{A}$		1		V
		$I_O = 150\ \text{mA}$		1		
$C_L$	Load capacitance	ESR and capacitance tradeoffs		1		$\mu\text{F}$
$I_{(REV)}$	Reverse output current on $V_I$	$V_I = \text{GND}$ , $V_O = \text{regulated voltage}$			50	$\mu\text{A}$

- NOTES: 4. Assured by design, not tested in production.  
 5. Ground terminal current is the regulator quiescent current drawn from the supply to support the load current.  
 6. Regulation is measured at constant junction temperature using low duty cycle pulse testing. Devices are tested for load regulation in the load range from 0.1 mA to 150 mA.

### enable input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IL}$	Regulated shutdown	$V_I = 3\ \text{V}$ to $5.25\ \text{V}$ regulated shutdown			0.8	V
$V_{IH}$	Regulated enabled	$V_I = 3\ \text{V}$ to $5.25\ \text{V}$ regulated enabled	2			V
$I_{(EN)}$	Enable input current	Shutdown, $V_{IL} \leq 0.8\ \text{V}$		0.01		$\mu\text{A}$
		Enabled, $V_{IH} \geq 2\ \text{V}$		0.01		
	Resistance discharge	$V_{(EN)} \leq 0.8\ \text{V}$		500		$\Omega$

### thermal protection (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$T_{(SD)}$	Thermal shutdown			165		$^\circ\text{C}$
$T_{(SDHYS)}$	Hysteresis			15		$^\circ\text{C}$

NOTE 4: Assured by design, not tested in production.

### power okay (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(POKLO)}$	Low threshold	Output falls % of $V_O$ (power NOT okay)	85%			
$V_{(POKTH)}$	High threshold	Output reaches % of $V_O$ , starts delay timer (power okay)			90%	
$V_{OL}$	$V_O$ out of regulation	Fault condition, $I_{OL} = 100\ \mu\text{A}$			0.4	V
$I_{lkg}$	Leakage current	$V_I = 5\ \text{V}$			1	$\mu\text{A}$

NOTE 7: Power okay is a function of the output voltage being 5% lower than the specified range. The function is a detection of one of the following: over current, over temperature, or dropout.



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**switching characteristics (see Note 4),  $T_A = 25^\circ\text{C}$ ,  $V_I = 5\text{ V}$ ,  $V_{(\text{EN})} = V_I$ ,  $I_O = 100\ \mu\text{A}$ ,  $C_L = 1\ \mu\text{F}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power up overshoot	Maximum voltage overshoot allowed on output during powerup		1%		
$t_{(\text{STEP})}$	Output transient time limit	Time for output to return within specified regulation range		5		$\mu\text{s}$
	Output transient voltage limit	Voltage that load step can affect the nominal output voltage		1%		
$I_{(\text{SR})}$	Load step current slew rate	$I_L = 0.1\ \text{mA}$ to 150 mA		10		$\text{mA}/\mu\text{s}$
$t_r$	Power up rise time			50		$\mu\text{s}$
$t_f$	Power down fall time	Discharge resistance = 500 $\Omega$ , $V_O < 1.08\ \text{V}$		60		$\mu\text{s}$
$t_d(\text{POK})$	Power okay delay time	$V_I > V_{(\text{POKTH})}$ until $\text{POK}\uparrow$		2.5		ms

NOTE 4: Assured by design, not tested in production.

### thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta\text{JC}}$	Thermal impedance, junction-to-case			145		$^\circ\text{C}/\text{W}$
$R_{\theta\text{JA}}$	Thermal impedance, junction-to-ambient			235		$^\circ\text{C}/\text{W}$

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## PARAMETER MEASUREMENT INFORMATION

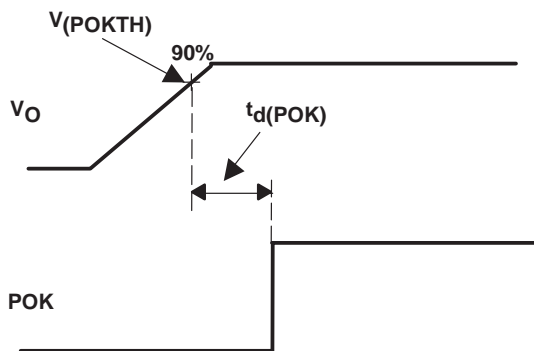


Figure 1. Power Okay Timing During Power Up

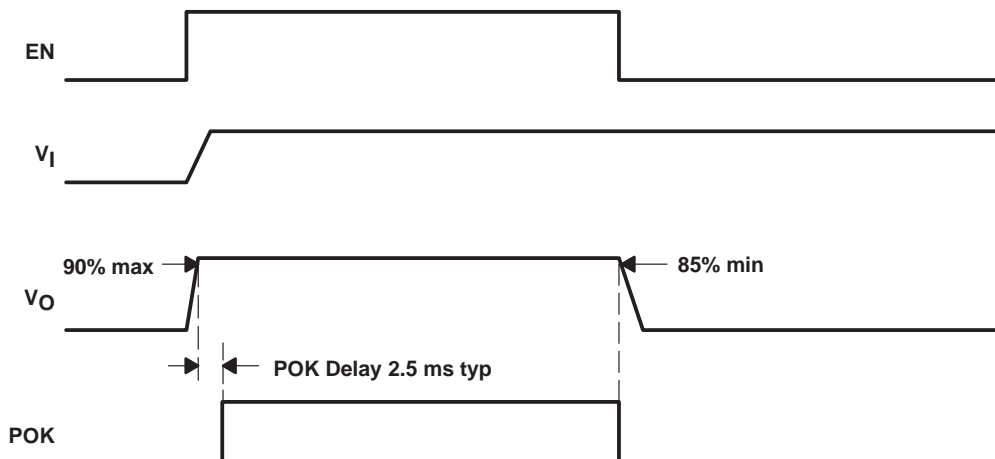


Figure 2. Power Okay Delay Timing and Output Voltage Supervisory

TYPICAL CHARACTERISTICS

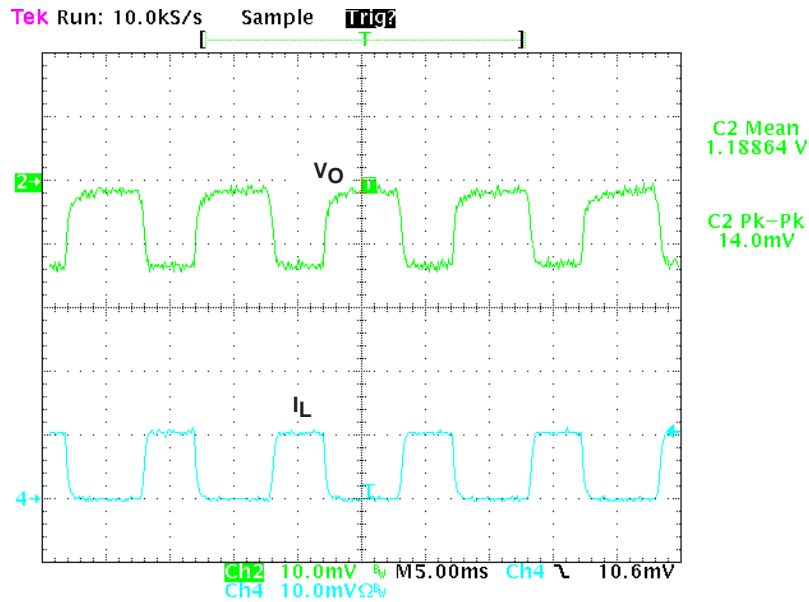


Figure 3. Load Regulation, 50-mA Dynamic Load Step ( $V_I = 3\text{ V}$ )

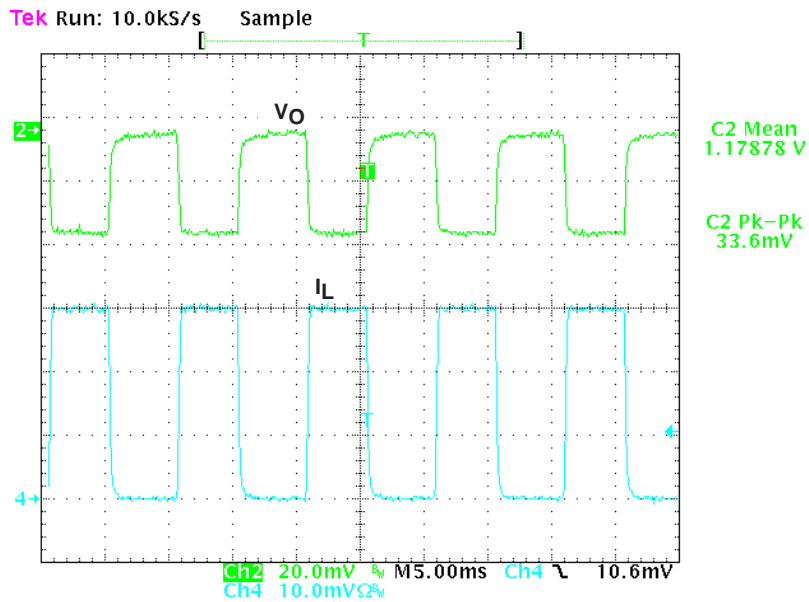


Figure 4. Load Regulation, 150-mA Dynamic Load Step ( $V_I = 3\text{ V}$ )

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## TYPICAL CHARACTERISTICS

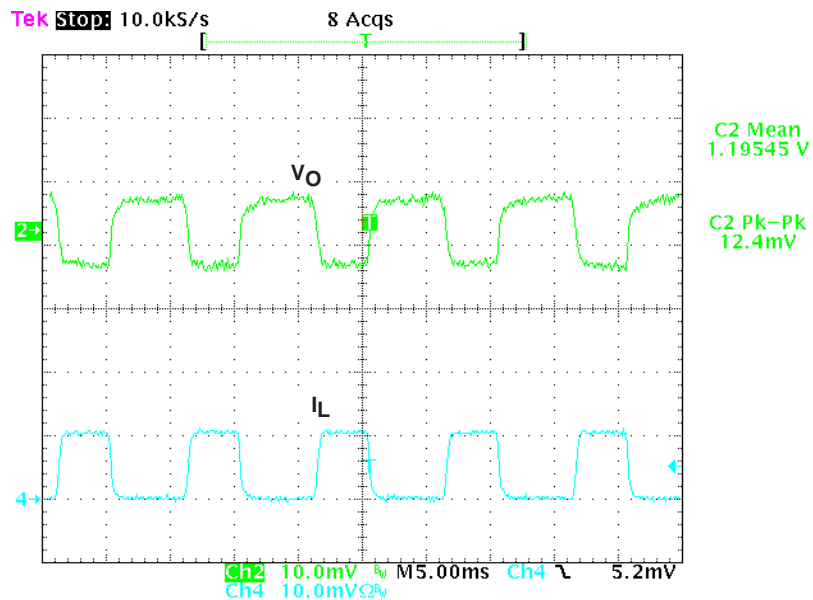


Figure 5. Load Regulation, 50-mA Dynamic Load Step ( $V_I = 5\text{ V}$ )

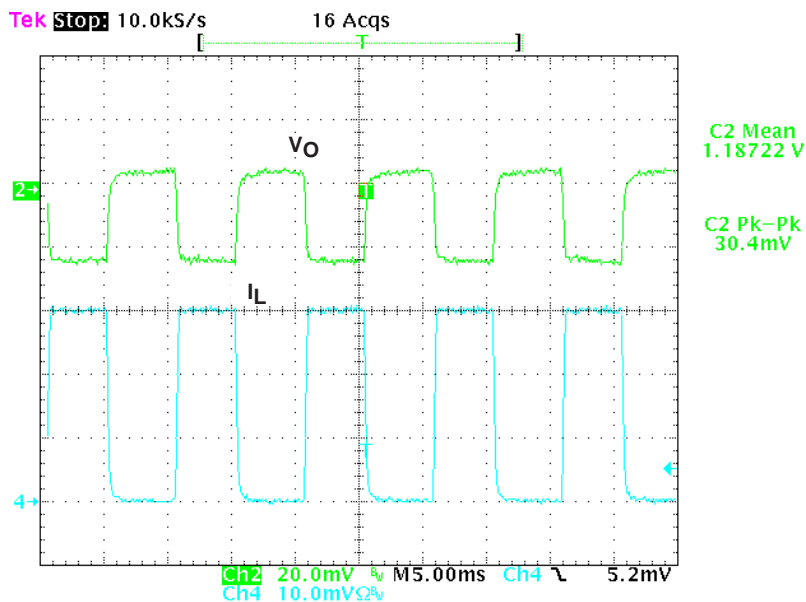


Figure 6. Load Regulation, 150-mA Dynamic Load Step ( $V_I = 5\text{ V}$ )



TYPICAL CHARACTERISTICS

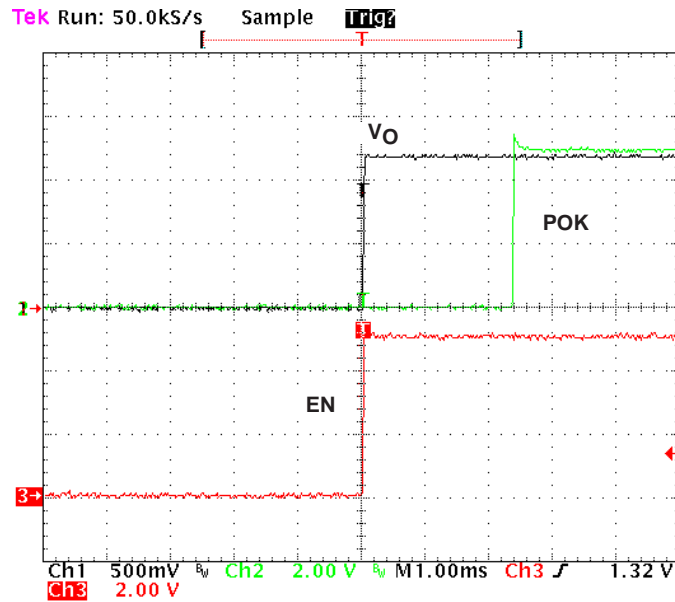


Figure 7. Power Okay Delay During Power Up Condition

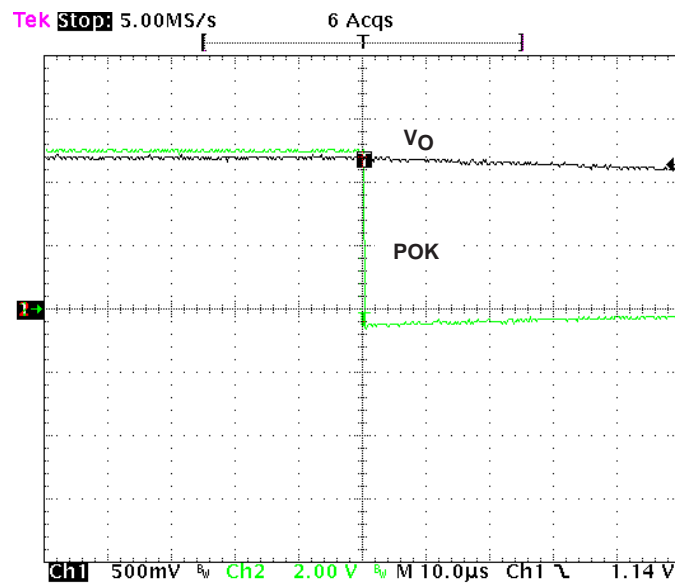


Figure 8. Power Okay Delay During Power Down Condition

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### THERMAL INFORMATION

The SN105125 is designed to provide a continuous load current of 150 mA when the maximum power dissipation of the package is not exceeded in the application. To determine the maximum power dissipation of the package, use the junction-to-ambient thermal resistance of the device. The basic equation is as follows:

Maximum power dissipation (W)

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA} \text{ (maximum power dissipation limit)}$$

Where:

$T_{J(MAX)}$  is the maximum junction temperature of the die (less than 150°C, minimum thermal shutdown)

$T_A$  is the operating ambient temperature

$R_{\theta JA}$  is the thermal resistance and is layout dependent

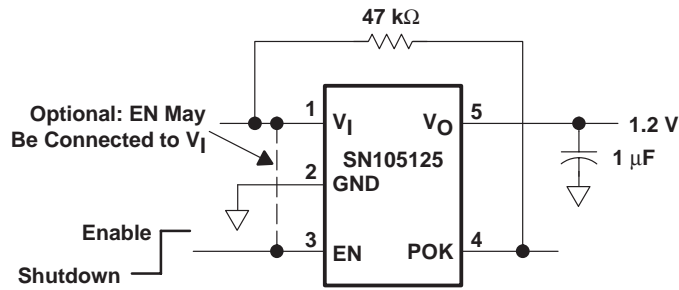
The recommended minimum footprint offers a  $R_{\theta JA}$  of 235°C/W.

To determine the actual power dissipation of the regulator, use the following equation:

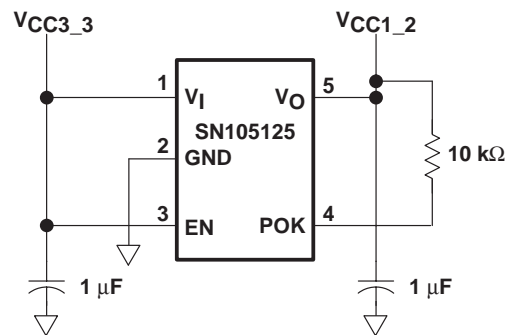
$$P_D = (V_I - V_O) I_O + V_I I_{(GND)} \text{ (Watts)}$$

Power dissipation resulting from quiescent current is negligible. When the power dissipation is excessive, the thermal protection circuit is triggered.

**APPLICATION INFORMATION**



**Figure 9. Typical Application Schematic**



**Figure 10. Typical Application For Processor VID Code Power Sequencing Schematic**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN105125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN105125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN105125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN105125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

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