



Flip Flops, Series 54/74

DM5472/DM7472

DM5472 / DM7472 (SN5472/SN7472)

J-K master slave flip flop

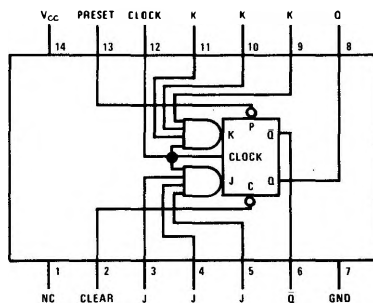
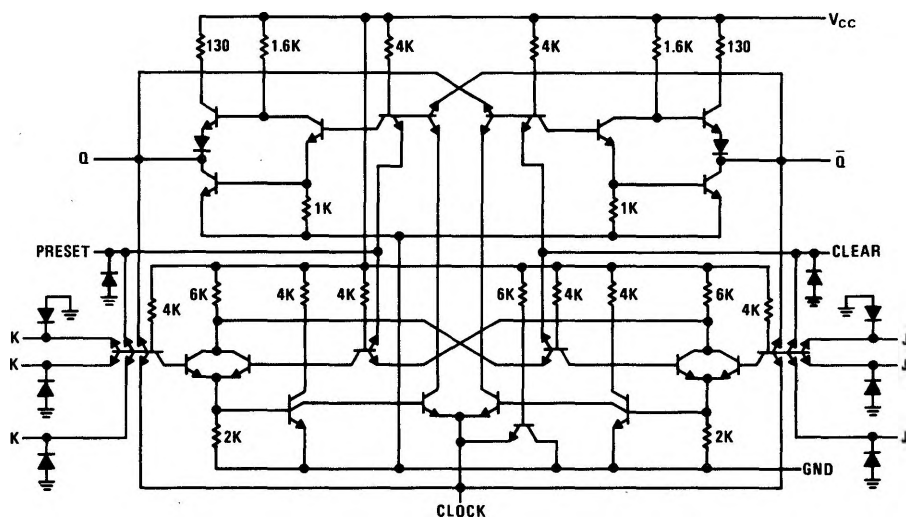
general description

The DM5472/DM7472 is a single flip flop with gating used to perform logic on the J and K inputs. Separate PRESET and CLEAR inputs override the clock and permit the flip flop to be directly set to either state. The flip flop is termed Master-Slave since the J and K information is load-

ed into the Master section when the clock voltage rises, and is transferred to the Slave section and outputs when the clock voltage falls.

The device also features a special clock line clamp to reduce ringing and prevent false clocking.

schematic and connection diagrams



absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7472	0°C to 70°C
DM5472	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

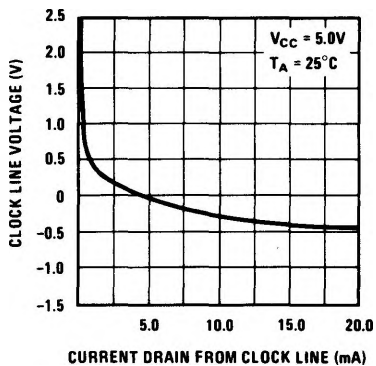
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	$V_{CC} = 5.0V$ $T_A = 25^\circ C$ $I_{IN} = -12 \text{ mA}$			-1.5	V
Clock Line Clamp Voltage	DM5472 $V_{CC} = 5.5V$ DM7472 $V_{CC} = 5.25V$ $I_{CLOCK} = -10 \text{ mA}$			-0.5	V
Logical "1" Input Voltage	DM5472 $V_{CC} = 4.5V$ DM7472 $V_{CC} = 4.75V$	2.0			V
Logical "0" Input Voltage	DM5472 $V_{CC} = 4.5V$ DM7472 $V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage	DM5472 $V_{CC} = 4.5V$ DM7472 $V_{CC} = 4.75V$ $I_{OUT} = -400 \mu A$	2.4			V
Logical "0" Output Voltage	DM5472 $V_{CC} = 4.5V$ DM7472 $V_{CC} = 4.75V$ $I_{OUT} = 16 \text{ mA}$			0.4	V
Logical "1" Input Current	DM5472 $V_{CC} = 5.5V$ DM7472 $V_{CC} = 5.25V$ $V_{IN} = 2.4V$				
J or K CLEAR or PRESET CLOCK			10 20 <0	40 80 80	μA μA μA
Logical "1" Input Current	DM5472 $V_{CC} = 5.5V$ DM7472 $V_{CC} = 5.25V$ $V_{IN} = 5.5V$			1	mA
Logical "0" Input Current	DM5472 $V_{CC} = 5.5V$ DM7472 $V_{CC} = 5.25V$ $V_{IN} = 0.4V$				
J or K CLEAR, PRESET, or CLOCK				-1.6 -3.2	mA mA
Output Short Circuit Current	DM5472 $V_{CC} = 5.5V$ DM7472 $V_{CC} = 5.25V$ $V_{OUT} = 0$	-20 -18		-55	mA
Supply Current	DM5472 $V_{CC} = 5.5V$ DM7472 $V_{CC} = 5.25V$		9	17	mA
Minimum Allowable Clock Pulse Width	$V_{CC} = 5.0V$ $T_A = 25^\circ C$			20	ns
Toggle Frequency	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	15	27		MHz
Propagation Delay Time to a Logical "0" from Clock, t_{pd0}	$V_{CC} = 5.0V$ $T_A = 25^\circ C$ N = 10 C = 50 pF	15	26	45	ns
Propagation Delay Time to a Logical "1" from Clock, t_{pd1}	$V_{CC} = 5.0V$ $T_A = 25^\circ C$ N = 10 C = 50 pF	10	17	30	ns
Propagation Delay Time to a Logical "0" from CLEAR or PRESET	$V_{CC} = 5.0V$ $T_A = 25^\circ C$ N = 10 C = 50 pF			40	ns
Propagation Delay Time to a Logical "1" from CLEAR or PRESET	$V_{CC} = 5.0V$ $T_A = 25^\circ C$ N = 10 C = 50 pF			25	ns
Time after negative-going clock transition that J or K information must be held, t_{hold}	$V_{CC} = 5.0V$ $T_A = 25^\circ C$			-5	ns
Time prior to negative-going clock transition that J or K information must be set, t_{setup}	$V_{CC} = 5.0V$ $T_A = 25^\circ C$		Clock pulse width		ns
Clock Voltage Fall Time	$V_{CC} = 5.0V$ $T_A = 25^\circ C$			150	ns
Clock Skew ($t_{pd \min} - t_{hold \max}$)	$V_{CC} = 5.0V$ $T_A = 25^\circ C$	15			ns

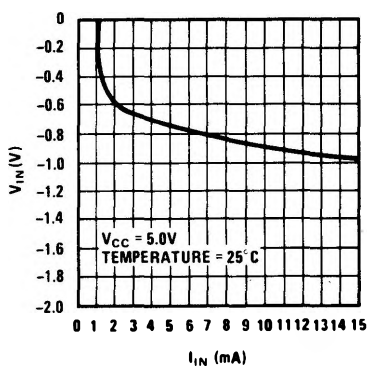
Note 1: Min/max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7472 and -55°C to +125°C for the DM5472 unless otherwise specified. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

typical performance characteristics

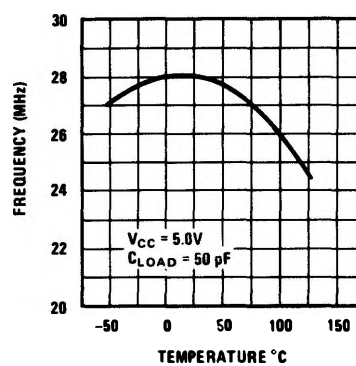
Clock Line Voltage vs Clock Line Current



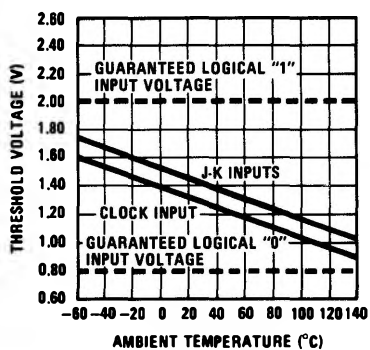
Input Clamp Diode Characteristics Inputs J1, J2, J3, K1, K2, K3



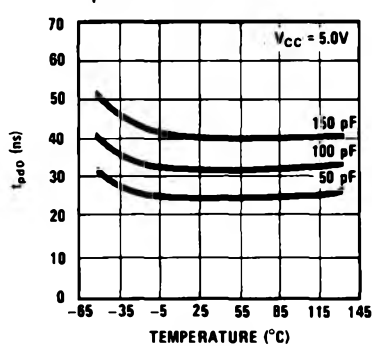
Maximum Toggle Frequency vs Temperature



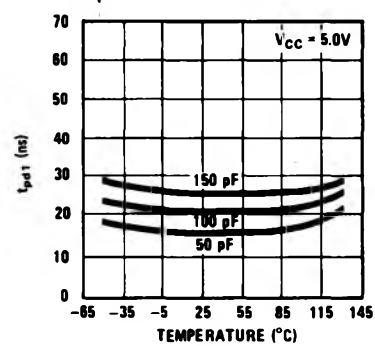
Threshold Voltage vs Temperature



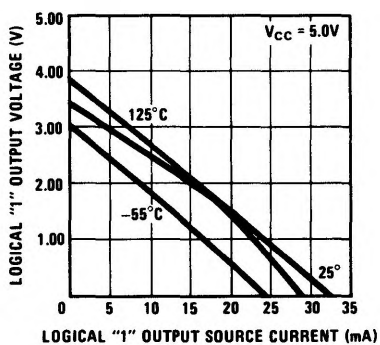
Transition Time to Logical "0" (tpd0) vs Temperature



Transition Time to Logical "1" (tpd1) vs Temperature



Logical "1" Output Voltage vs Source Current



Logical "0" Output Voltage vs Sink Current

