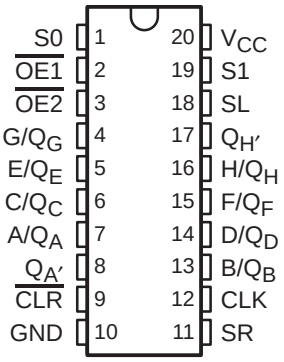
The SN54F299 is obsolete and no longer supplied.

SN54F299, SN74F299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

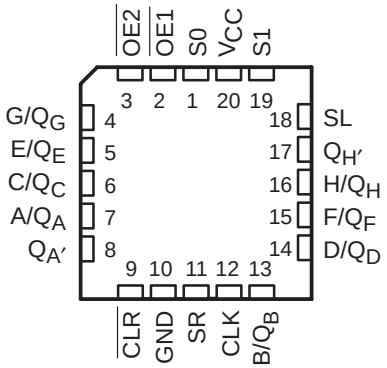
SDFS071B − MARCH 1987 − REVISED APRIL 2004

- **Four Modes of Operation:**
  - **Hold (Store)**
  - **Shift Right**
  - **Shift Left**
  - **Load Data**
- **Operates With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - **Stacked or Pushdown Registers**
  - **Buffer Storage**
  - **Accumulator Registers**

SN54F299 . . . J PACKAGE
SN74F299 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54F299 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) inputs and two output-enable ($\overline{OE1}$, $\overline{OE2}$) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when the clear ($\overline{CLR}$) input is low. Taking either $\overline{OE1}$ or $\overline{OE2}$ high disables the outputs but has no effect on clearing, shifting, or storage of data.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP − N	Tube of 20	SN74F299N	SN74F299N
	SOIC − DW	Tube of 25	SN74F299DW	F299
		Reel of 2000	SN74F299DWR	
	SOP − NS	Reel of 2000	SN74F299NSR	74F299

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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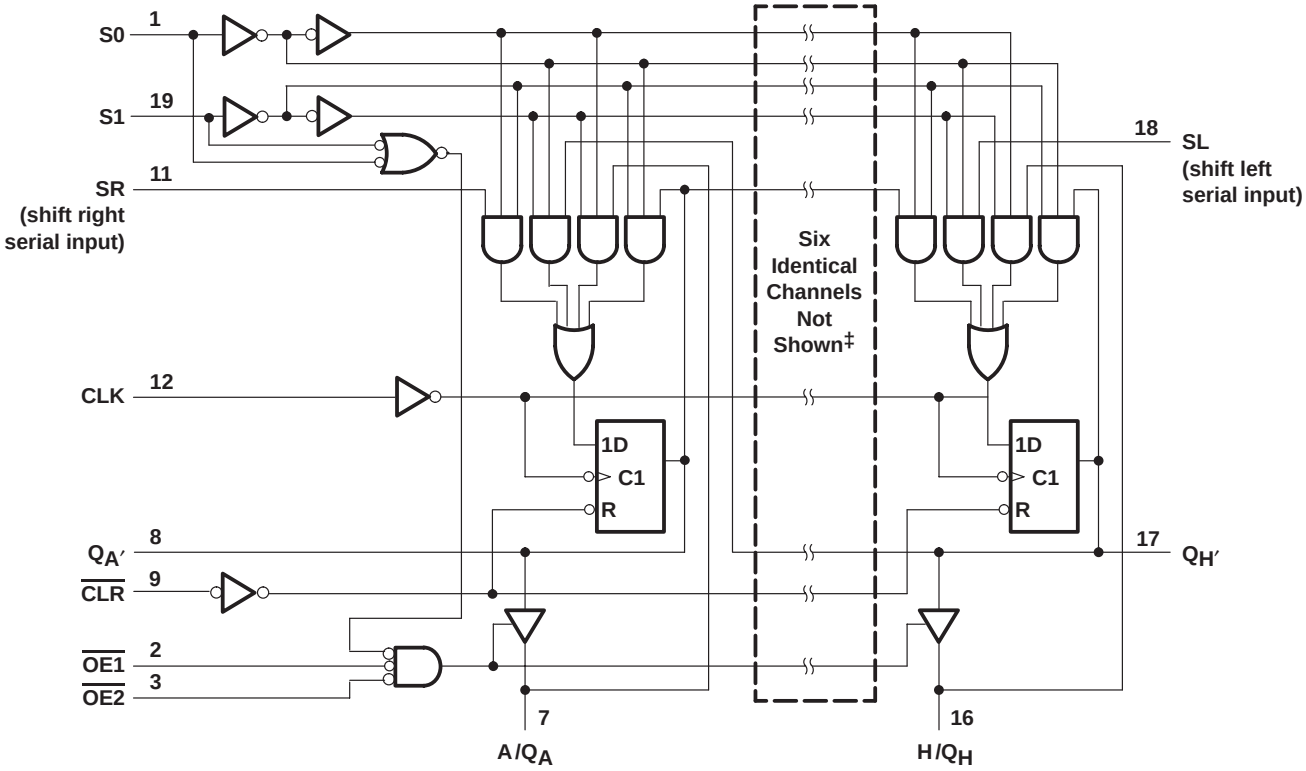
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	$\overline{OE1}$†	$\overline{OE2}$†	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic diagram (positive logic)



‡ I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −1.2 V to 7 V
Input current range . . . . . −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: $Q_{A'}$ or $Q_{H'}$ . . . . . 40 mA
SN54F299 (Q_A thru Q_H) . . . . . 40 mA
SN74F299 (Q_A thru Q_H) . . . . . 48 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54F299			SN74F299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	$Q_{A'}$ or $Q_{H'}$			−1			−1	mA
		Q_A thru Q_H			−3			−3	
I_{OL}	Low-level output current	$Q_{A'}$ or $Q_{H'}$			20			20	mA
		Q_A thru Q_H			20			24	
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

The SN54F299 is obsolete and no longer supplied.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F299			SN74F299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V	I_{OH} = − 1 mA	2.5	3.4		2.5	3.4		V
	Q_A thru Q_H		I_{OH} = − 1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = − 3 mA	2.4	3.3		2.4	3.3		
	Any output	V_{CC} = 4.75 V,	I_{OH} = − 1 mA to −3 mA				2.7			
V_{OL}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	Q_A thru Q_H		I_{OL} = 20 mA		0.3	0.5				
			I_{OL} = 24 mA					0.35	0.5	
I_I	A thru H	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	mA
	Any other		V_I = 7 V			0.1			0.1	
I_{IH}‡	A thru H	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	µA
	Any other					20			20	
I_{IL}‡	A thru H	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	S0 or S1					−1.2			−1.2	
	Any other					−0.6			−0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 4		68	95		68	95	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 4: I_{CC} is measured with $\overline{OE1}$, $\overline{OE2}$, and CLK at 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V_{CC} = 5 V, T_A = 25°C ′F299		SN54F299		SN74F299		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				70		65		70	MHz
t_w	Pulse duration	CLK high or low		7		8		7		ns
		$\overline{CLR}$ low		7		8		7		
t_{su}	Setup time before CLK↑	S0 or S1	High or low	8.5		9.5		8.5		ns
		A/Q_A thru H/Q_H, SR, or SL	High or low	5.5		6.5		5.5		
	Inactive-state setup time before CLK↑¶	$\overline{CLR}$	High	7		13		7		
t_h	Hold time after CLK↑	S0 or S1	High or low	0		0		0		ns
		A/Q_A thru H/Q_H, SR, or SL	High or low	2		2		2		

¶ Inactive-state setup time also is referred to as recovery time.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			′F299			SN54F299		SN74F299		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			70	100		65		70		MHz
t_{PLH}	CLK	$Q_{A'}$ or $Q_{H'}$	3.2	6.6	9	2.7	10.5	3.2	10	ns
t_{PHL}			2.7	6.1	8.5	2.2	10	2.7	9.5	
t_{PLH}	CLK	Q_A thru Q_H	3.2	6.6	9	2.7	11	3.2	10	ns
t_{PHL}			4.2	8.1	11	3.7	12.5	4.2	12	
t_{PHL}	$\overline{CLR}$	$Q_{A'}$ or $Q_{H'}$	3.7	7.1	9.5	3.2	11.5	3.7	10.5	ns
		Q_A thru Q_H	5.7	10.6	14	5	15.5	5.7	15	
t_{PZH}	$\overline{OE1}$ or $\overline{OE2}$	Q_A thru Q_H	2.7	5.6	8	2.2	10.5	2.7	9	ns
t_{PZL}			3.2	6.6	10	2.7	12	3.2	11	
t_{PHZ}	$\overline{OE1}$ or $\overline{OE2}$	Q_A thru Q_H	1.7	4.1	6	1.7	9	1.7	7	ns
t_{PLZ}			1.2	3.6	5.5	1.2	7.5	1.2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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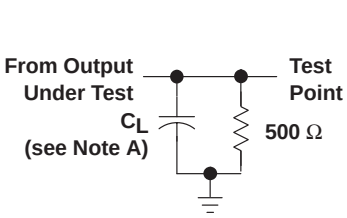
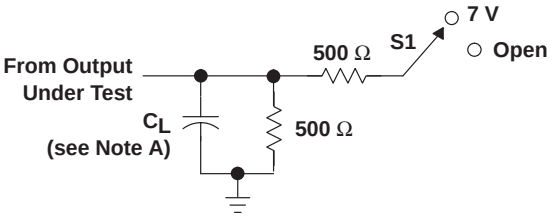
PARAMETER MEASUREMENT INFORMATION

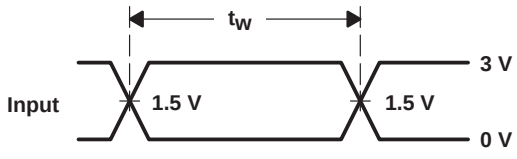


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

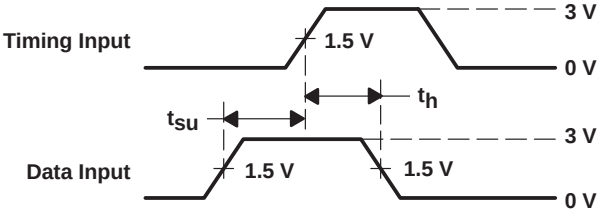


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

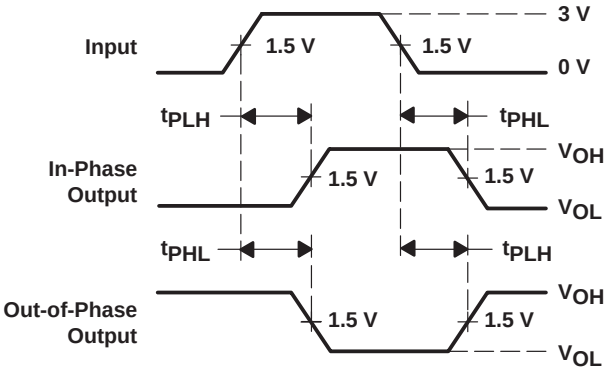
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
Open Collector	7 V



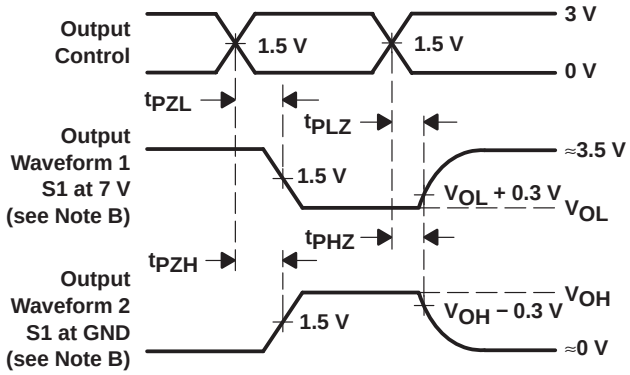
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns, duty cycle = 50%.
D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74F299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	Samples
SN74F299DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	Samples
SN74F299DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	Samples
SN74F299DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	Samples
SN74F299DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	Samples
SN74F299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74F299N	Samples
SN74F299N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74F299NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74F299N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

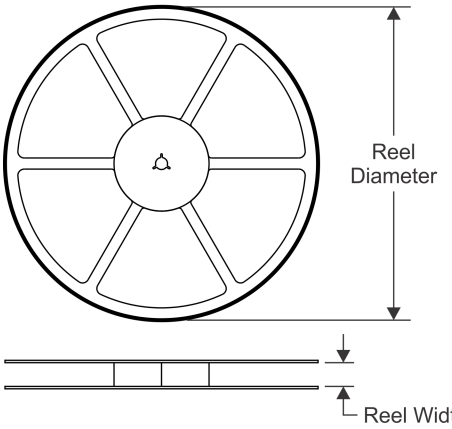
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

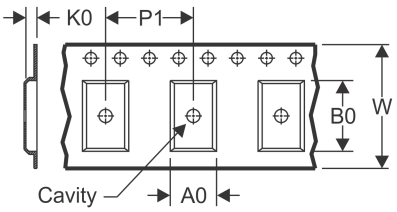
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

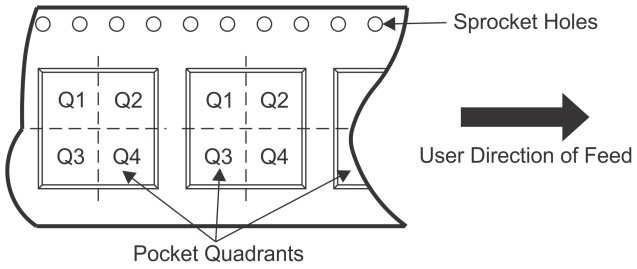


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

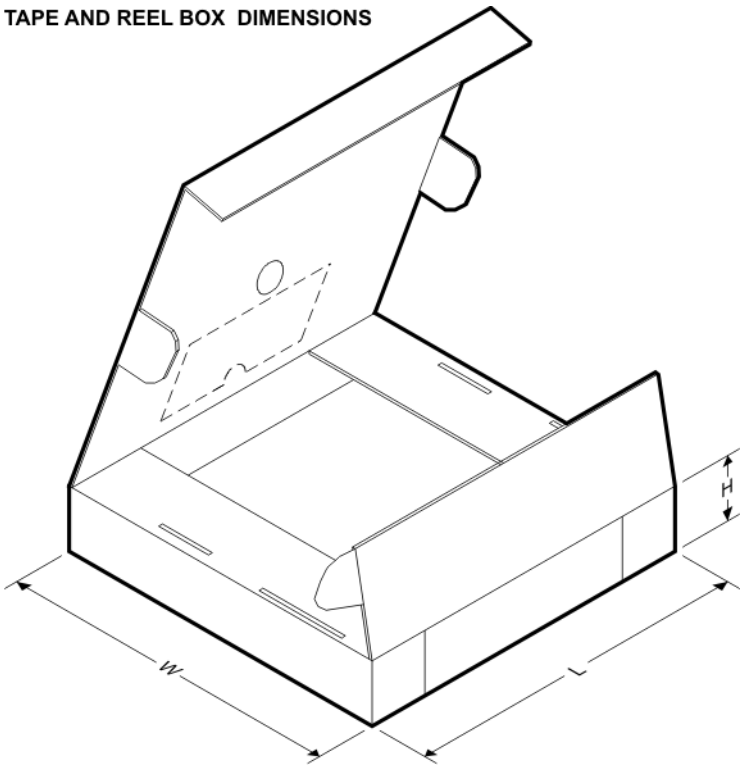
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F299DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



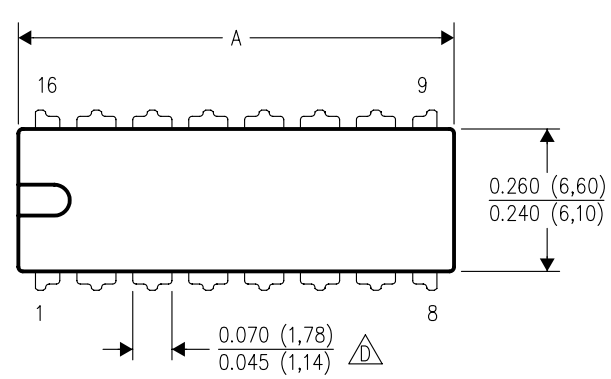
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F299DWR	SOIC	DW	20	2000	367.0	367.0	45.0

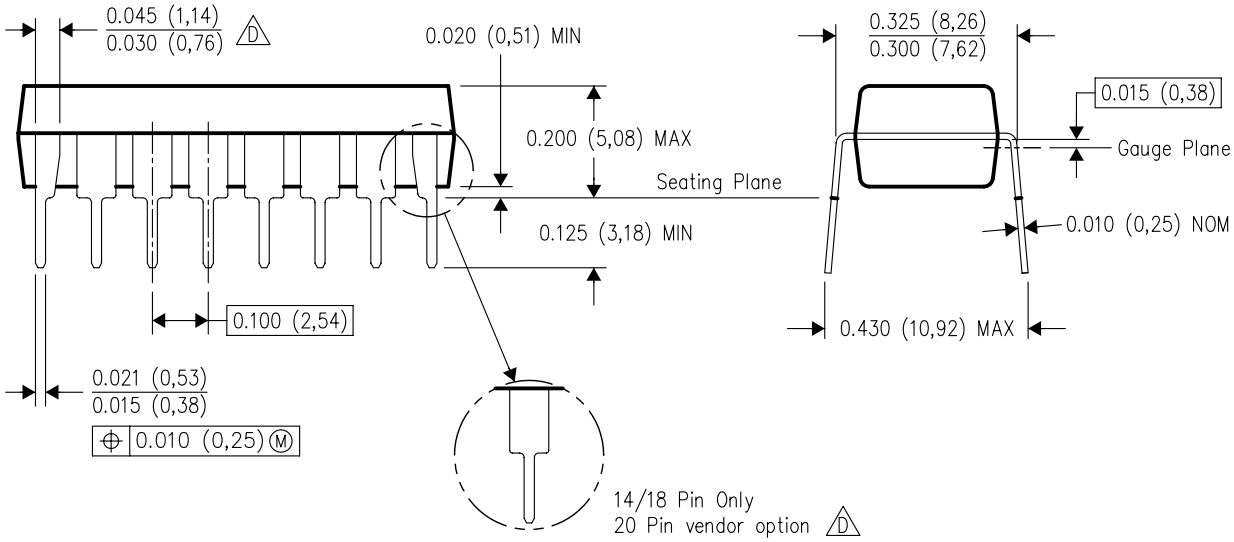
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



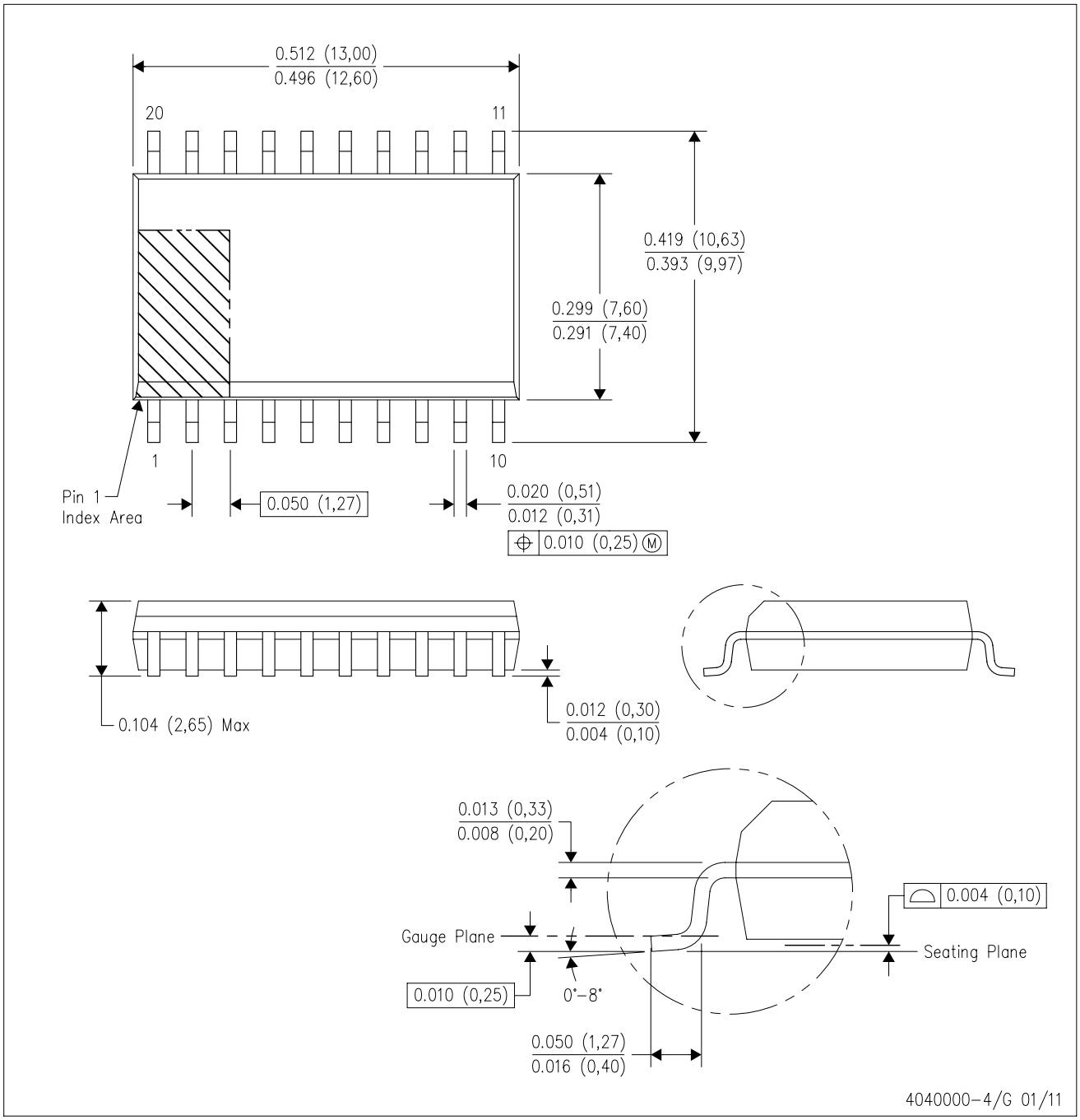
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

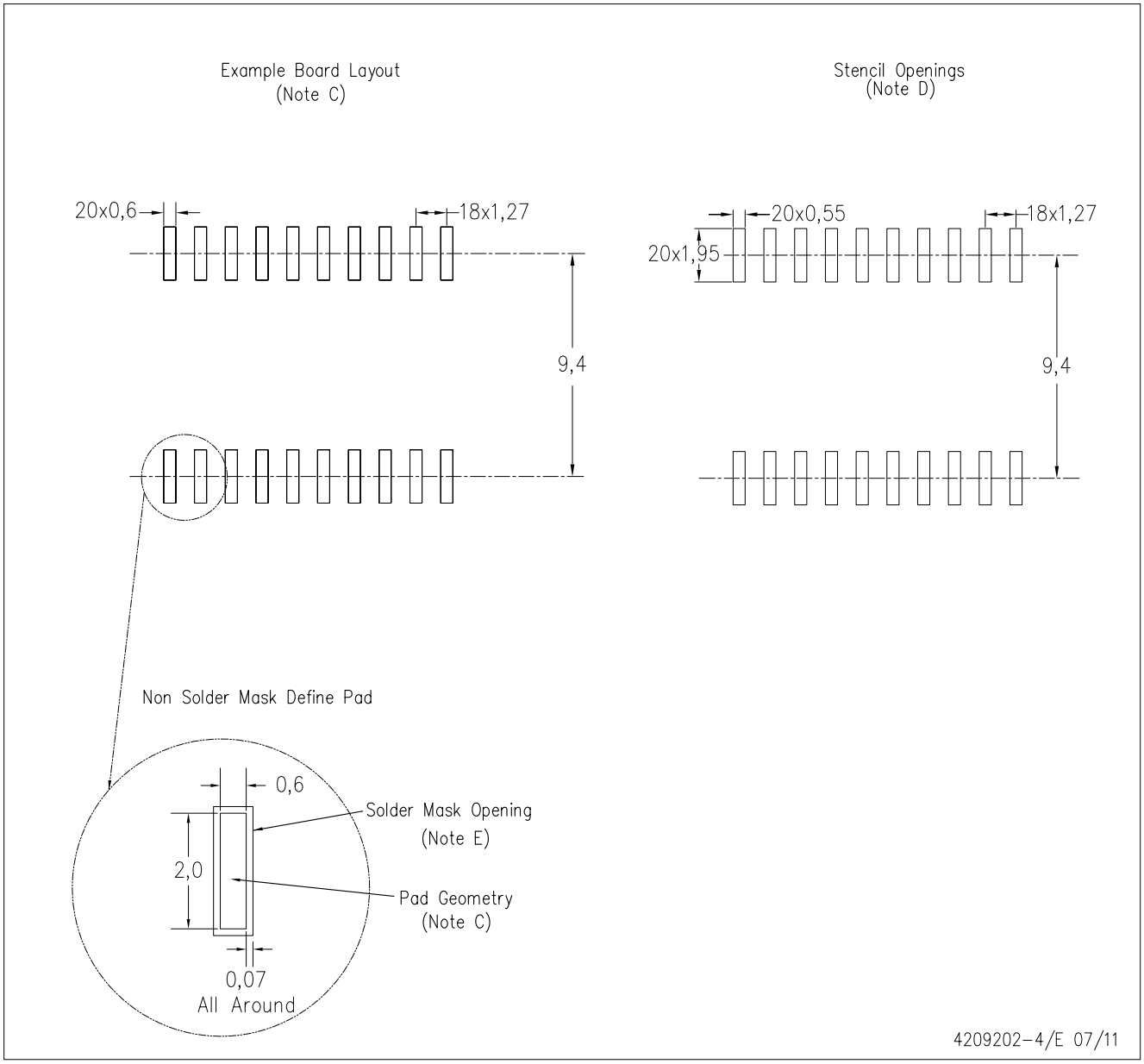
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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