

SN54HC4724, SN74HC4724 8-BIT ADDRESSABLE LATCHES

SCLS166

D2684, DECEMBER 1982—REVISED JUNE 1989

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable Input Simplifies Expansion
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

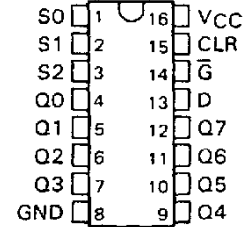
These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear (CLR) and enable (\bar{G}) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable \bar{G} should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54HC4724 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC4724 is characterized for operation from -40°C to 85°C .

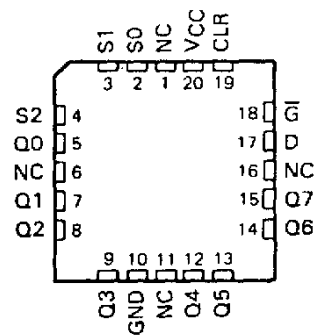
SN54HC4724 . . . J PACKAGE
SN74HC4724 . . . N PACKAGE

(TOP VIEW)



SN54HC4724 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLR	\bar{G}			
L	L	D	Q_iO	Addressable Latch
L	H	Q_iO	Q_iO	Memory
H	L	D	L	8-Line Demultiplexer
H	H	L	L	Clear

LATCH SELECTION TABLE

SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

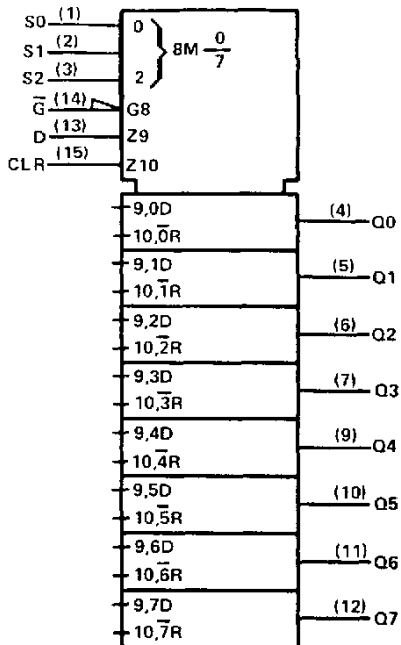
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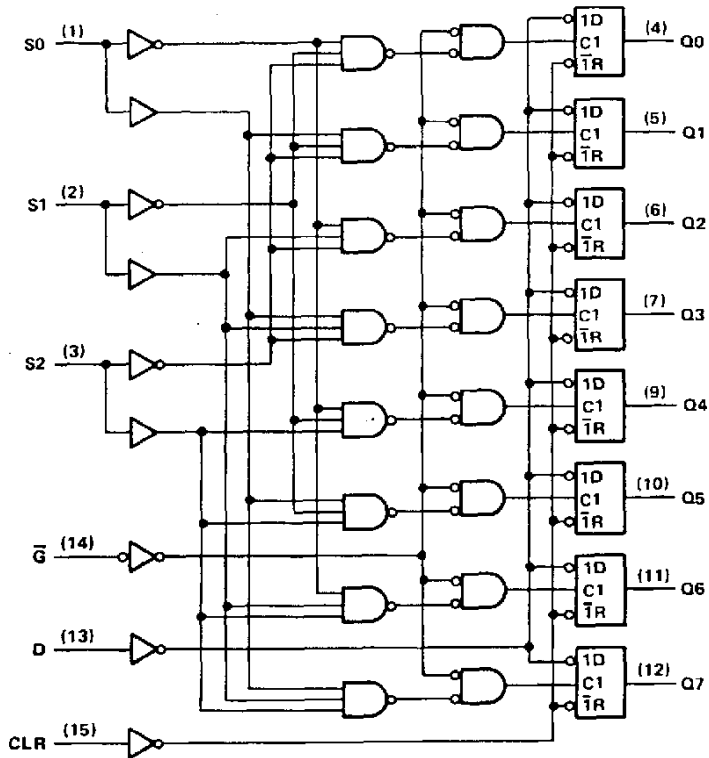
logic symbol†



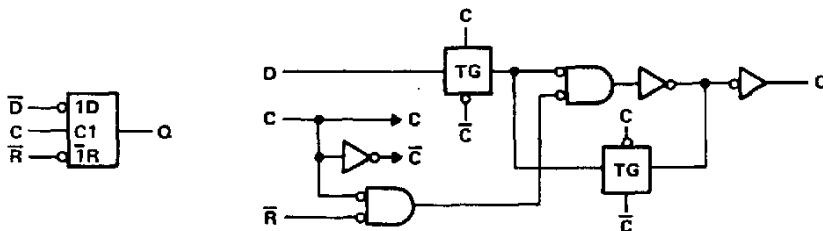
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

logic diagram (positive logic)



logic symbol and logic diagram, each internal latch (positive logic)



SN54HC4724, SN74HC4724
8-BIT ADDRESSABLE LATCHES

absolute maximum ratings over operating free-air temperature†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC4724			SN74HC4724			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5			V
		$V_{CC} = 4.5$ V	3.15		3.15			
		$V_{CC} = 6$ V	4.2		4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0	0.3	0	0.3	V	
		$V_{CC} = 4.5$ V	0	0.9	0	0.9		
		$V_{CC} = 6$ V	0	1.2	0	1.2		
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000	0	1000	ns	
		$V_{CC} = 4.5$ V	0	500	0	500		
		$V_{CC} = 6$ V	0	400	0	400		
T_A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC4724		SN74HC4724		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -4 \text{ mA}$	2 V		0.002	0.1			0.1	V	
		4.5 V		0.001	0.1			0.1		
		6 V		0.001	0.1			0.1		
	4.5 V		0.17	0.26			0.4	0.33		
$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26			0.4	0.33		
	6 V		± 0.1	± 100			± 1000	± 1000	nA	
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V					160	80	μA	
C_i		2 to 6 V		3	10		10	10	pF	



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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C			SN54HC4724		SN74HC4724		UNIT
			MIN		MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	2 V	80			120			ns	
		4.5 V	16			24		20		
		6 V	14			20		17		
	$\overline{\text{G}}$ low	2 V	80			120		100		
		4.5 V	16			24		20		
		6 V	14			20		17		
t _{su}	Setup time, data or address before $\overline{\text{G}}\uparrow$	2 V	75			115		95	ns	
		4.5 V	15			23		19		
		6 V	13			20		16		
t _h	Hold time, data or address after $\overline{\text{G}}\uparrow$	2 V	5			5		5	ns	
		4.5 V	5			5		5		
		6 V	5			5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC4724		SN74HC4724		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PHL}	CLR	Any Q	2 V		60	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		14	26		38		32	
t _{pd}	Data	Any Q	2 V		56	130		195		165	ns
			4.5 V		17	26		39		33	
			6 V		13	22		33		28	
t _{pd}	Address	Any Q	2 V		74	200		300		250	ns
			4.5 V		21	40		60		50	
			6 V		17	34		51		43	
t _{pd}	$\overline{\text{G}}$	Any Q	2 V		66	170		255		215	ns
			4.5 V		20	34		51		43	
			6 V		16	29		43		37	
t _t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C _{pd}	Power dissipation capacitance per latch	No load, T _A = 25°C	33 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.



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