

- High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads
- Bus-Structured Pinout
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

An output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

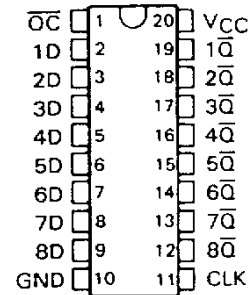
An output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HC564 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC564 is characterized for operation from -40°C to 85°C .

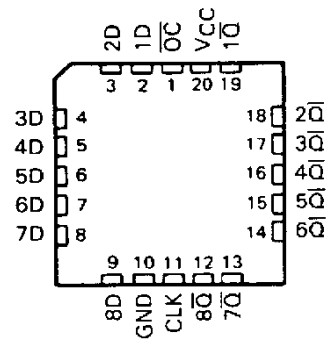
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
\overline{OC}	CLK	D	\overline{Q}
L	↑	H	L
L	↑	L	H
L	L	X	\overline{Q}_0
H	X	X	Z

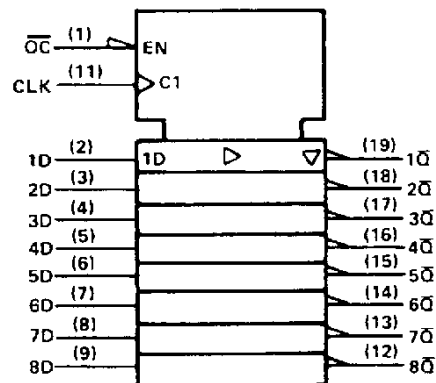
SN54HC564 . . . J PACKAGE
SN74HC564 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC564 . . . FK PACKAGE
(TOP VIEW)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

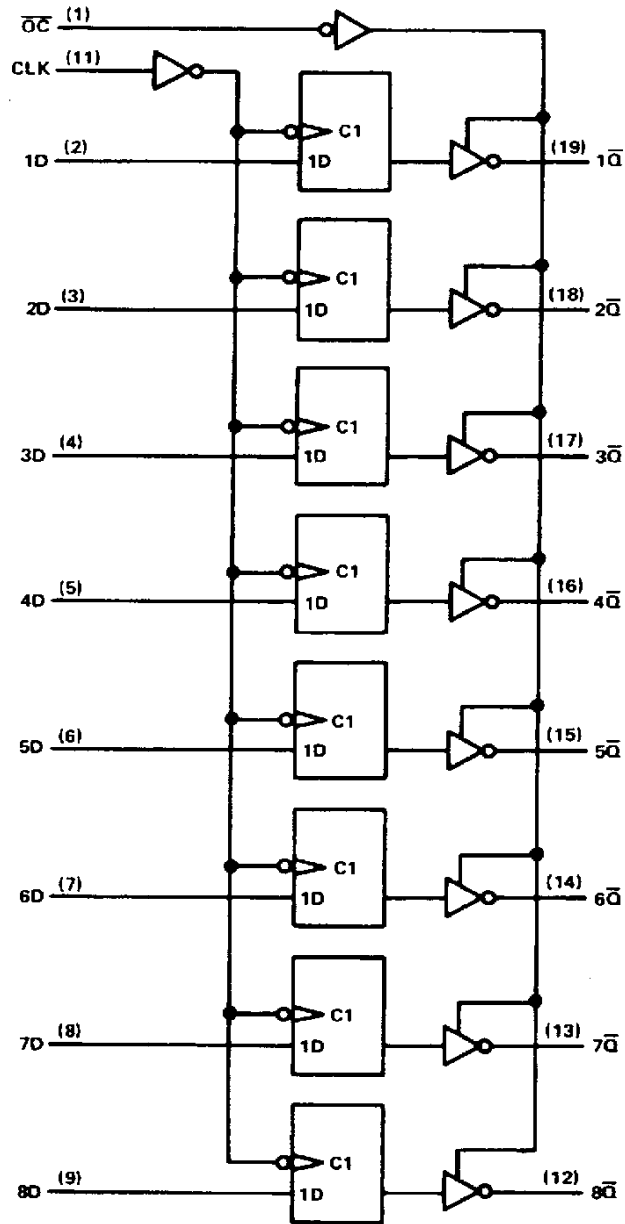


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5-154HC564, SN74HC564
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

logic diagram (positive logic)



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SN54HC564, SN74HC564
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC564			SN74HC564			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	$V_{CC} = 2$ V		1.5	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 6$ V		4.2	$V_{CC} = 6$ V		4.2	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0	$V_{CC} = 2$ V		0.3	V
		$V_{CC} = 4.5$ V		0	$V_{CC} = 4.5$ V		0.9	
		$V_{CC} = 6$ V		0	$V_{CC} = 6$ V		1.2	
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) times	$V_{CC} = 2$ V		0	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		0	$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		0	$V_{CC} = 6$ V		400	
T_A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC564		SN74HC564		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = -6 \text{ mA}$	4.5 V	5.48	5.80		5.2		5.34	V	
		6 V								
		2 V		0.002	0.1		0.1			0.1
	4.5 V		0.001	0.1		0.1		0.1		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20 \mu\text{A}$	6 V		0.001	0.1		0.1		0.1	
		4.5 V		0.17	0.26		0.4		0.33	
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 6 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
		4.5 V								
I_I	$V_I = V_{CC}$ or 0	6 V	± 0.1	± 100		± 1000		± 1000	nA	
I_{OZ}	$V_O = V_{CC}$ or 0	6 V	± 0.01	± 0.5		± 10		± 5	μA	
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V		8		160		80	μA	
C_I		2 to 6 V		3	10		10		pF	



SN54HC564, SN74HC564
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HC564		SN74HC564		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency	2 V	0	6	0	4.2	0	5	MHz
	4.5 V	0	31	0	21	0	25	
	6 V	0	36	0	25	0	29	
t _w Pulse duration, CLK high or low	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t _{su} Setup time, data before CLK†	2 V	100		150		125		ns
	4.5 V	20		30		25		
	6 V	17		26		21		
t _h Hold time, data after CLK†	2 V	5		5		5		ns
	4.5 V	5		5		5		
	6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC564		SN74HC564		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6	11		4.2		5	MHz	
			4.5 V	31	36		21		25		
			6 V	36	40		25		29		
t _{pd}	CLK	Any \bar{Q}	2 V		54	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		15	31		46		38	
t _{en}	\overline{OC}	Any \bar{Q}	2 V		45	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t _{dis}	\overline{OC}	Any \bar{Q}	2 V		45	150		225		190	ns
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t _t		Any \bar{Q}	2 V		28	60		90		75	ns
	4.5 V			8	12		18		15		
	6 V			6	10		15		13		

C _{pd}	Power dissipation capacitance per flip-flop	No load, T _A = 25°C	100 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.



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SN54HC564, SN74HC564
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 150 \text{ pF}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC564		SN74HC564		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Any \bar{Q}	2 V		75	230		345		290	ns
			4.5 V		24	46		69		58	
			6 V		21	34		58		49	
t_{en}	\bar{OC}	Any \bar{Q}	2 V		57	200		300		250	ns
			4.5 V		19	40		60		50	
			6 V		17	34		51		43	
t_t		Any \bar{Q}	2 V		60	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		14	36		53		45	

Note 1: Load circuits and voltage waveforms are shown in Section 1.

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