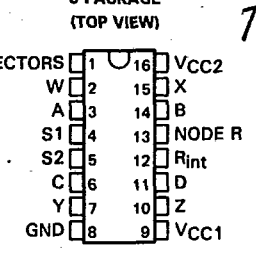
SN55325
MEMORY CORE DRIVER

D969, MARCH 1971—REVISED SEPTEMBER 1986

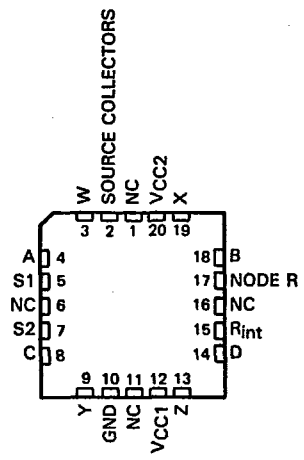
T-52-15

- 600-mA Output Capability
- Fast Switching Times
- Output Transient-Voltage Protection
- Dual Sink and Dual Source Outputs
- Minimum Time Skew Between Address and Output Current Rise
- 24-Volt Output Capability
- Source Base Drive Externally Adjustable
- TTL Compatibility
- Input Clamping Diodes
- Transformer Coupling Eliminated
- Reliability Increased
- Drive-Line Lengths Reduced
- Use of External Components Minimized

J PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN55325 monolithic integrated circuit memory driver is designed for use with magnetic memories.

The device contains two 600-milliampere source switches and two 600-milliampere sink switches. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

When R_{int} and node R are connected together, the amount of base drive available for the source-1 or source-2 output transistor is set internally by a 575-ohm resistor. This method provides adequate base drive for source currents up to 375 mA with a V_{CC2} voltage of 15 volts or 600 mA with a V_{CC2} voltage of 24 volts.

When source currents greater than 375 mA are required, it is recommended that a resistor of the appropriate value be connected between V_{CC2} and node R and R_{int} must remain open. By using this method the source base current may usually be regulated within ±5%. An advantage of this method of setting the base drive is that the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher source currents for a given junction temperature.

Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This arrangement provides protection from voltage surges associated with switching inductive loads.

The SN55325 is characterized for operation over the full military temperature range of −55°C to 125°C.

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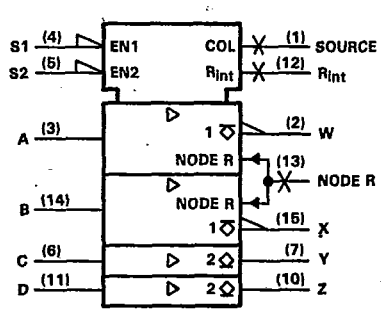
logic symbol†



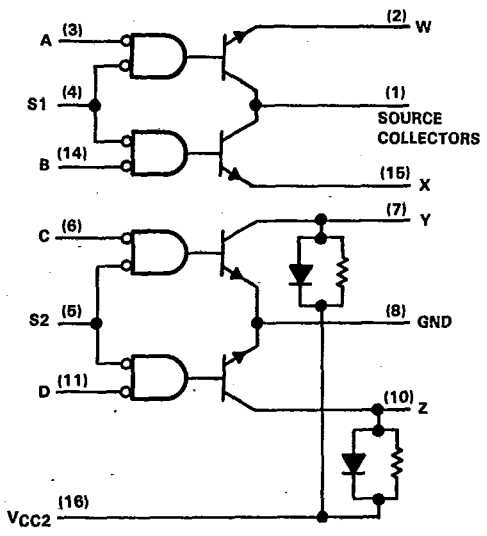
†This symbol is in accordance with ANSI/EEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J package.

FUNCTION TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC1} (see Note 1) . . . . . 7 V
Supply voltage V_{CC2} (see Note 1) . . . . . 25 V
Input voltage (any address or strobe input) . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range . . . . . −55 to 125°C
Storage temperature range . . . . . −65 to 150°C
Case temperature for 10 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 11.0 mW/°C for both packages.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.5	5	5.5	V
Supply voltage, V_{CC2}	4.5		24	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperatuare, T_A	−55		125	°C

electrical characteristics over rated operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC1} = 4.5 V, I_I = −10 mA,	V_{CC2} = 24 V, T_A = 25°C		−1.3	−1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		V_{CC1} = 4.5 V, V_{CC2} = 24 V	T_A = −55°C to 125°C			500	μA
				T_A = 25°C		3	150	
V_{OH}	High-level sink output voltage		V_{CC1} = 4.5 V, I_O = 0	V_{CC2} = 24 V,	19	23		V
$V_{(sat)}$	Saturation voltage	Source outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω to V_{CC2}, $I_{(source)}$ ≈ −600 mA‡, See Note 3	T_A = −55°C to 125°C			0.9	V
				T_A = 25°C		0.43	0.7	
		Sink outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω to V_{CC2}, $I_{(sink)}$ ≈ 600 mA‡, See Note 3	T_A = −55°C to 125°C			0.9	
				T_A = 25°C		0.43	0.7	
I_I	Input current at maximum input voltage	Address inputs	V_{CC1} = 5.5 V, V_I = 5.5 V	V_{CC2} = 24 V,			1	mA
		Strobe inputs					2	
I_{IH}	High-level input current	Address inputs	V_{CC1} = 5.5 V, V_I = 2.4 V	V_{CC2} = 24 V,		3	40	μA
		Strobe inputs				6	80	
I_{IL}	Low-level input current	Address inputs	V_{CC1} = 5.5 V, V_I = 0.4 V	V_{CC2} = 24 V,		−1	−1.6	mA
		Strobe inputs				−2	−3.2	
$I_{CC(off)}$	Supply current, all sources and sinks off	From V_{CC1}	V_{CC1} = 5.5 V, T_A = 25°C	V_{CC2} = 24 V,		14	22	mA
		From V_{CC2}				7.5	20	
I_{CC1}	Supply current from V_{CC1} either sink on		V_{CC1} = 5.5 V, $I_{(sink)}$ = 50 mA,	V_{CC2} = 24 V, T_A = 25°C		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		V_{CC1} = 5.5 V, $I_{(source)}$ = −50 mA, See Note 3	V_{CC2} = 24 V, T_A = 25°C,		32	60	mA

†All typical values are at T_A = 25°C.
‡Under these conditions, not more than one output is to be on at any one time.
NOTE 3: These parameters must be measured using pulse techniques, t_w = 200 μs, duty cycle ≤2%.

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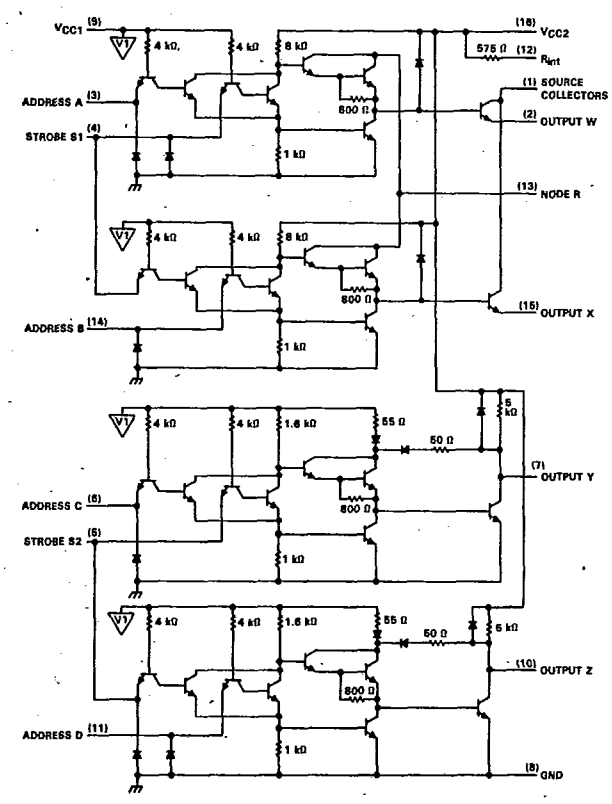
switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER†	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Source collectors	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		45	60	ns
t_{PHL}				45	60	
t_{TLH}	Source outputs	V_{CC2} = 20 V, R_L = 1 kΩ, C_L = 25 pF		55		ns
t_{THL}				7		
t_{PLH}	Sink outputs	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		25	45	ns
t_{PHL}				25	45	
t_{TLH}	Sink outputs	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		10	15	ns
t_{THL}				15	20	
t_S	Sink outputs	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		20	30	ns

†t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_S = storage time

schematic



Component values shown are nominal. Pin numbers shown are for the J package.

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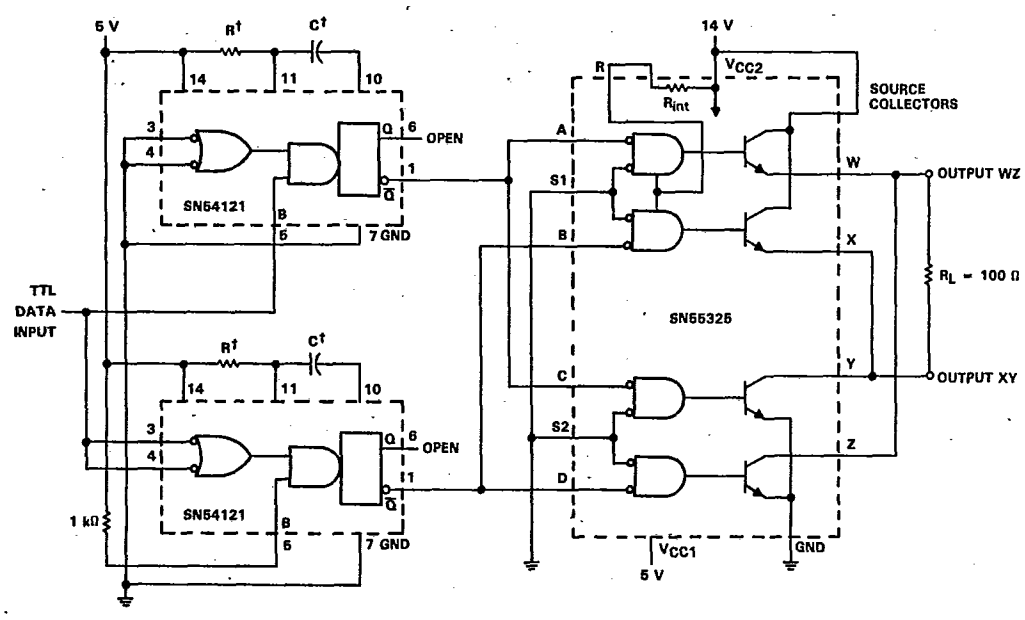
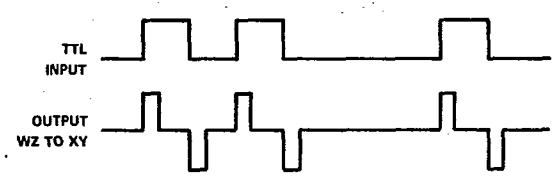
TYPICAL APPLICATION DATA

balanced bipolar logic-line driver

The circuit shown in Figure 1 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5-volt supply; however, the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a three-state output that is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several thousand feet in length or low-impedance coaxial lines.



TEST CIRCUIT



VOLTAGE WAVEFORMS

†R and C are adjusted to give the desired bipolar output pulse width.

FIGURE 1. BALANCED BIPOLAR LOGIC-LINE DRIVER

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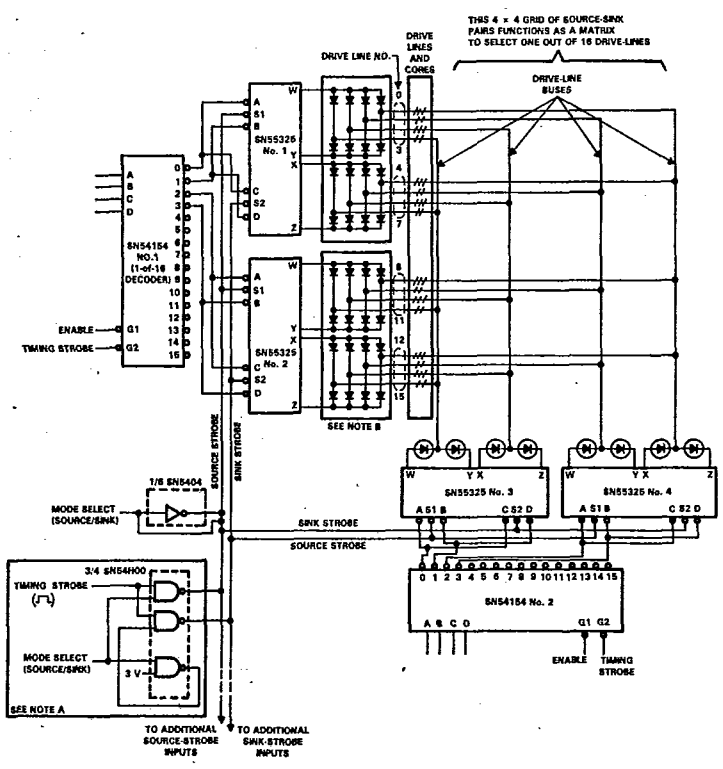
TYPICAL APPLICATION DATA

balanced bipolar logic-line driver

In memory-drive applications, the SN55325 can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 2. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, SN54154 No. 1 must be set to 3 (with mode select high), enabling source X of SN55325 No. 2 to drive lines 12 through 15, and SN54154 No. 2 must be set to 2, providing a sink at Y of SN55325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 3. These 256 drive-lines are sufficient to serve $(256/2)^2 = 16{,}384$ individual cores.



NOTE A: This optional mode-select and timing-strobe technique can be used in place of the SN5404 mode-select and SN54154 timing-strobe when minimum time skew is desired.
B. All diodes are IN4607.

FIGURE 2. SN55325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

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TYPICAL APPLICATION DATA

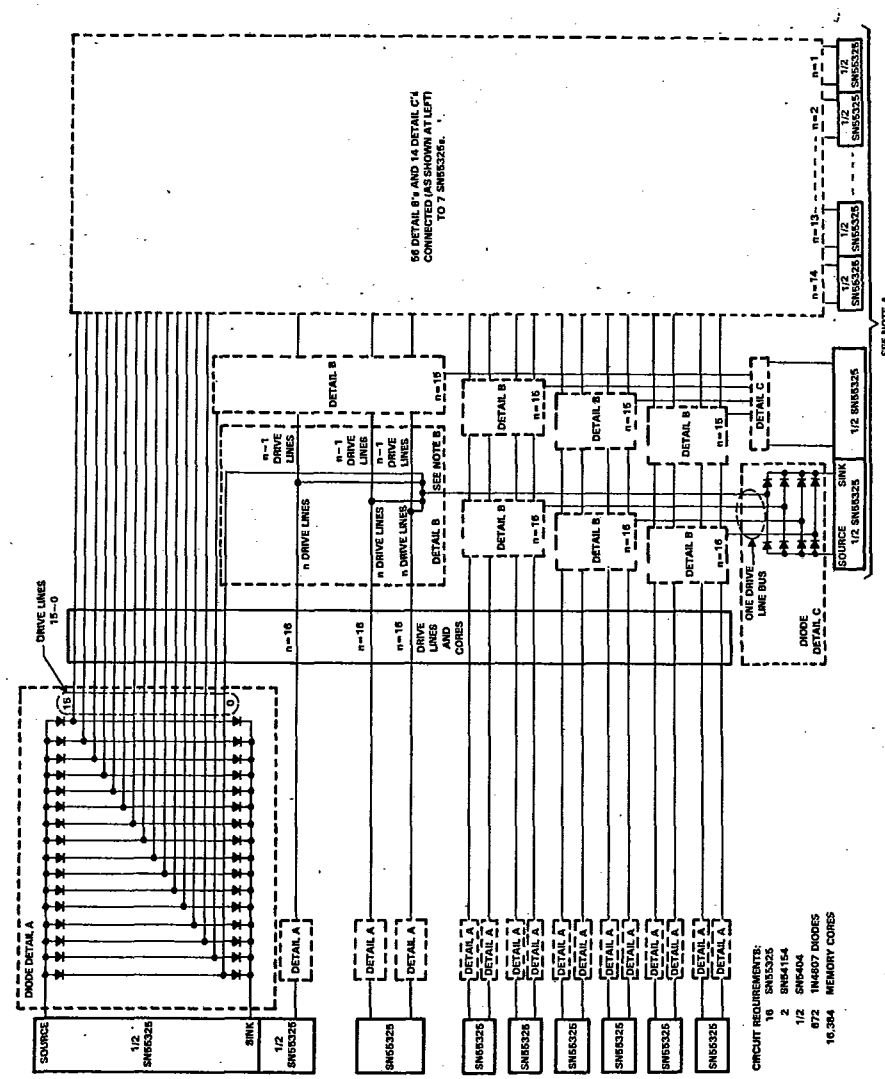

FIGURE 3. SN55325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY

NOTES: A. Outputs from one SN54154 decoder are connected to each SN55325 as shown in Figure 2. Source strobe and sink strobe from an SN5404 are connected to each SN55325 as shown in Figure 2.
B. The division of the drive-line bus into four segments reduces the capacitive load on the SN55325 driver.
C. All diodes are IN4607.

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TYPICAL APPLICATION DATA

external resistor calculation

A typical magnetic-memory word-drive requirement is shown in Figure 4. A source-output transistor of one SN55325 delivers load current (I_L). The sink-output transistor of another SN55325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \quad (1)$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2,

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3,

$$I_{CS} \approx 0.94\ I_L \quad (3)$$

where: I_{CS} in in mA.

As an example, let $V_{CC2(min)} = 20$ V and $V_L = 3$ V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ mA$$

In this example, the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

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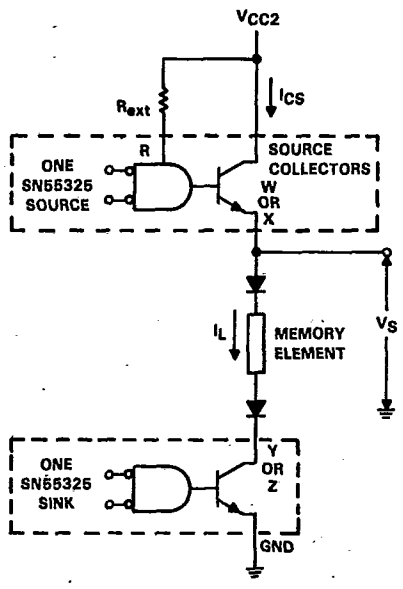
TYPICAL APPLICATION DATA

external resistor calculation (continued)



NOTES: A. For clarity, partial logic diagrams of two SN55325s are shown.
B. Source and sink shown are in different packages.

FIGURE 4