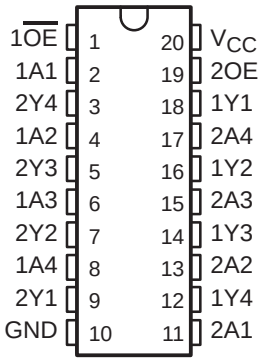
- **State-of-the-Art BiCMOS Design Substantially Reduces Standby Current**
- **3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883 Method 3015**
- **High-Impedance State During Power Up and Power Down**
- **Package Options Include Small-Outline (DW) and Standard Plastic DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



description

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. With the SN64BCT240 and SN64BCT244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs.

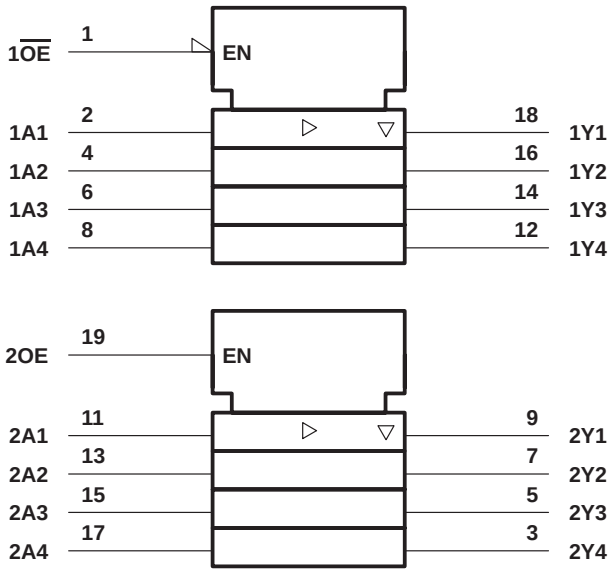
The SN64BCT241 is characterized for operation from –40°C to 85°C and 0°C to 70°C.

FUNCTION TABLES

INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

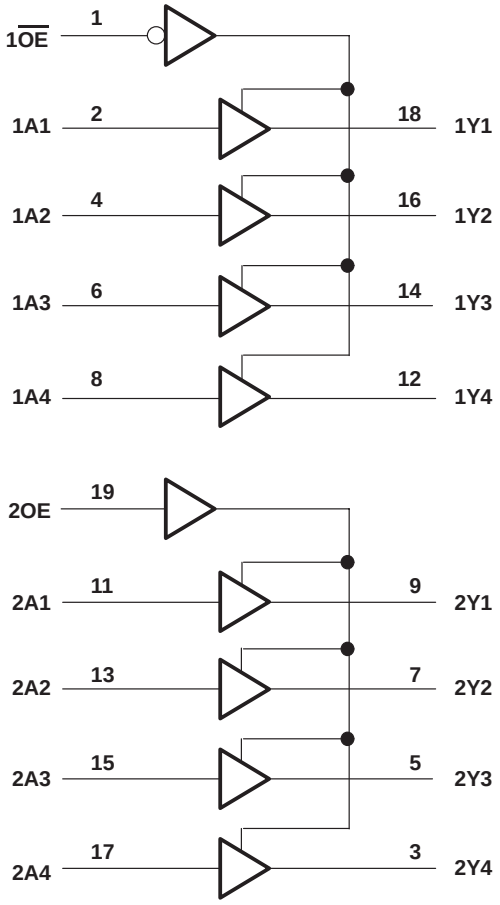
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . – 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . – 0.5 V to V_{CC}
Current into any output in the low state, I_O . . . . . 128 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 97°C/W
N package . . . . . 67°C/W
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative voltage rating may be exceeded if the input clamp current rating is observed.
2. The package thermal impedance is calculated in acordane with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

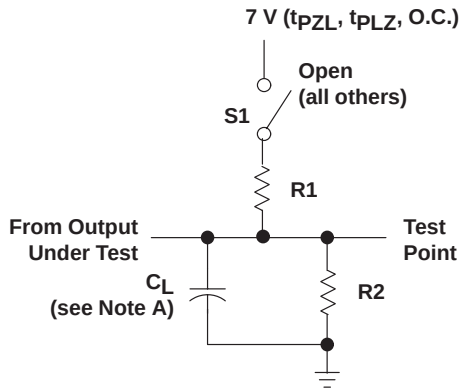
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.3		V
			I_{OH} = –15 mA	2	3.1		
		V_{CC} = 4.75 V,	I_{OH} = –3 mA	2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OH} = 64 mA		0.42	0.55	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OZ}	$1\overline{OE}$ at 0.8 V, 2OE at 2 V	V_{CC} = 0 to 2.3 V (power up)	V_O = 2.7 V or 0.5 V,			± 50	µA
		V_{CC} = 1.8 V to 0 (power down)				± 50	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	$1\overline{OE}$ or $2\overline{OE}$	V_{CC} = 5.5 V,	V_I = 0.5 V			–1	mA
	Any A input					–1.6	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0	–100		–225	mA
I_{CCL}		V_{CC} = 5.5 V,	Output open		23	43	mA
I_{CCH}		V_{CC} = 5.5 V,	Output open		53	85	mA
I_{CCZ}		V_{CC} = 5.5 V,	Output open		4	10	mA
C_i		V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6		pF
C_o		V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		11		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

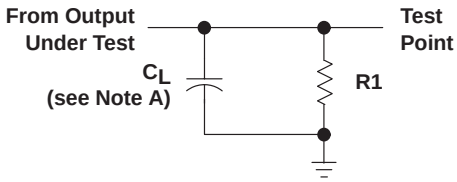
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
					T_A = –40°C to 85°C		T_A = 0°C to 70°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	4.5	0.5	5.2	0.5	4.9	ns
t_{PHL}			1	5.4	1	6.3	1	5.9	
t_{PZH}	1OE or 2$\overline{OE}$	Y	1	7.8	1	9.1	1	8.7	ns
t_{PZL}			1	8.6	1	10	1	9.4	
t_{PHZ}	1OE or 2$\overline{OE}$	Y	1	6.8	1	8.4	1	8.1	ns
t_{PLZ}			1	8.1	1	11	1	9.9	

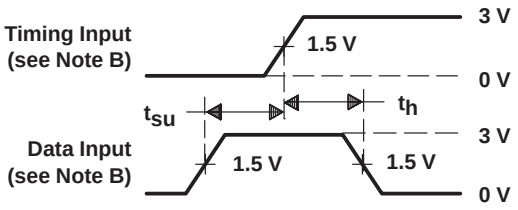
PARAMETER MEASUREMENT INFORMATION



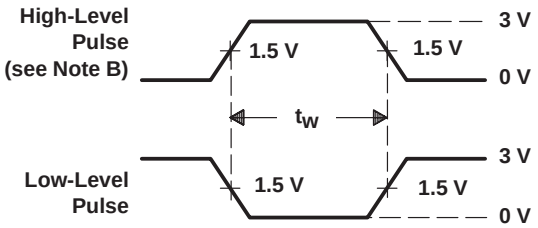
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



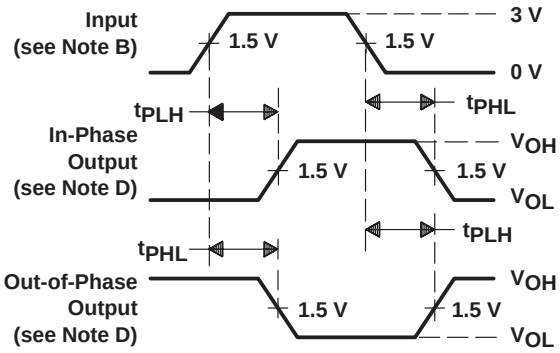
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



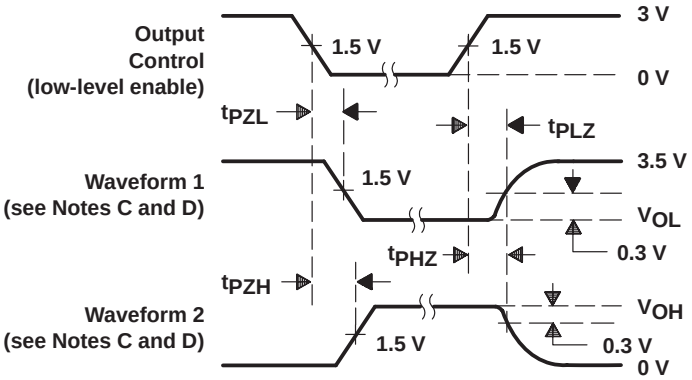
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN64BCT241DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN64BCT241N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265