

## 9-CHANNEL RS-422 / RS-485 TRANSCEIVER

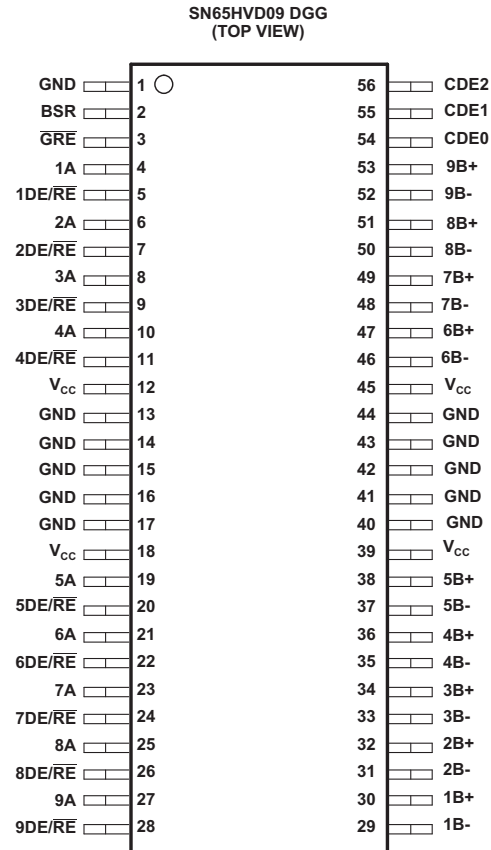
 Check for Samples: [SN65HVD09-EP](#)

### FEATURES

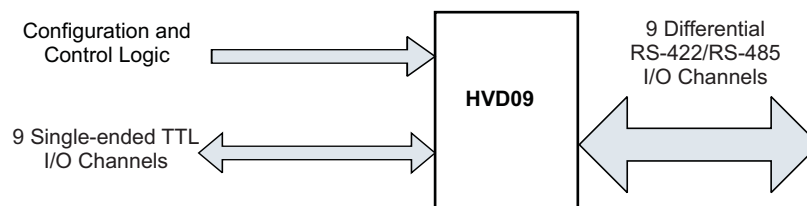
- Designed to Operate at up to 20 Million Data Transfers per Second on Each RS-422/RS-485 Channel
- SN65HVD09 Packaged in Thin Shrink Small-Outline Package with 0.5-mm Pin Pitch
- ESD Protection on Bus Pins Exceeds 12kV
- Low Disabled Supply Current 8 mA Typ
- Thermal Shutdown Protection
- Positive- and Negative-Current Limiting
- Power-Up/Down Glitch Protection

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



Terminals 13 through 17, and 40 through 44 are connected together to the package lead frame and signal ground.



### DESCRIPTION

The SN65HVD09 is a 9-channel RS-422 / RS-485 transceiver suitable for industrial applications. It offers improved switching performance, a small package, and high ESD protection. The precise skew limits ensures that the propagation delay times, not only from channel-to-channel but from device-to-device, are closely matched for the tight skew budgets associated with high-speed parallel data buses.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## SN65HVD09-EP

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Patented thermal enhancements are used in the thin shrink, small-outline package (TSSOP), allowing operation over the industrial temperature range. The TSSOP package offers very small board area requirements while reducing the package height to 1 mm. This provides more board area and allows component mounting to both sides of the printed circuit boards for low-profile, space-restricted applications such as small form-factor hard disk drives.

The HVD09 can withstand electrostatic discharges exceeding 12 kV using the human-body model, and 600 V using the machine model on the RS-485 I/O terminals. This provides protection from the noise that can be coupled into external cables. The other terminals of the device can withstand discharges exceeding 4 kV and 400 V respectively.

Each of the nine half-duplex channels of the HVD09 is designed to operate with either RS-422 or RS-485 communication networks.

The SN65HVD09 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 85°C	TSSOP-DGG	SN65HVD09IDGGREP	SN65HVD09EP	V62/12607-01XE

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### PIN FUNCTIONS

NAME	PIN NO.	LOGIC LEVEL	I/O	TERMINATION	DESCRIPTION
1A to 9A	4,6,8,10,19,21,23,25,27	TTL	I/O	Pullup	1A to 9A carry data to and from the communication controller.
1B– to 9B–	29,31,33,35,37,46,48,50,52	RS-485	I/O	Pulldown	1B– to 9B– are the inverted data signals of the balanced pair to/from the bus.
1B+ to 9B+	30,32,34,36,38,47,49,51,53	RS-485	I/O	Pullup	1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus.
BSR	2	TTL	Input	Pullup	BSR is the bit significant response. BSR disables receivers 1 through 8 and enables wired-OR drivers when BSR and DE/RE and CDE1 or CDE2 are high. Channel 9 is placed in a high-impedance state with BSR high.
CDE0	54	TTL	Input	Pulldown	CDE0 is the common driver enable 0. Its input signal enables all drivers when CDE0 and 1DE/RE – 9DE/RE are high.
CDE1	55	TTL	Input	Pulldown	CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when CDE1 is high and BSR is low.
CDE2	56	TTL	Input	Pulldown	CDE2 is the common driver enable 2. When CDE2 is high and BSR is low, drivers 5 to 8 are enabled.
$\overline{\text{CRE}}$	3	TTL	Input	Pullup	$\overline{\text{CRE}}$ is the common receiver enable. When high, CRE disables receiver channels 5 to 9.
1DE/RE to 9DE/RE	5,7,9,11,20,22,24,26,28	TTL	Input	Pullup	1DE/RE–9DE/RE are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when 1DE/RE–9DE/RE and CRE and BSR are low and CDE1 and CDE2 are low.
GND	1,13,14,15,16,17,40,41,42,43,44	NA	Power	NA	GND is the circuit ground. All GND terminals except terminal 1 are physically tied to the die pad for improved thermal conductivity. <sup>(1)</sup>
V <sub>CC</sub>	12,18,39,45	NA	Power	NA	Supply voltage

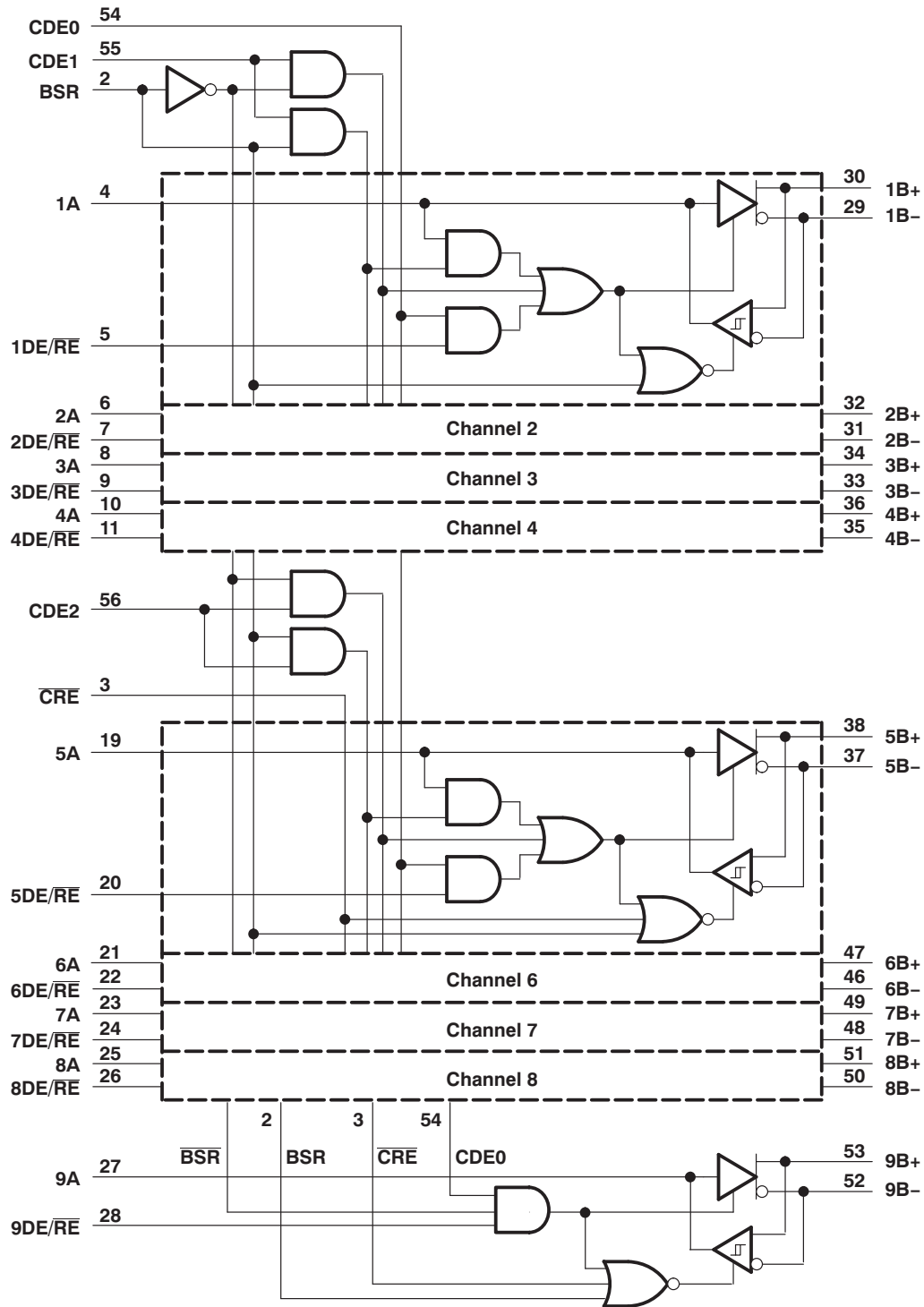
- (1) Terminal 1 must be connected to signal ground for proper operation.

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LOGIC DIAGRAM (POSITIVE LOGIC)



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

		VALUE	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	–0.3 to 6	V
	Bus voltage range	–10 to 15	V
	Data I/O and control (A side) voltage range	–0.3 to V <sub>CC</sub> +0.5	V
I <sub>O</sub>	Receiver output current	±40	mA
Electrostatic discharge	B side and GND, ESD HBM	12	kV
	B side and GND, ESD MM	400	V
	All terminals, ESD HBM	4	kV
	All terminals, ESD MM	400	V
Continuous total power dissipation <sup>(3)</sup>		Internally Limited	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals.
- (3) The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.

**DISSIPATION RATINGS**

PACKAGE	T <sub>A</sub> ≤ 25°C	OPERATING FACTOR <sup>(1)</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
DGG	2500 mW	20 mW/°C	1600 mW	1300 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

**PACKAGE THERMAL CHARACTERISTICS**

		MIN	NOM	MAX	UNIT
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	DGG, board-mounted, no air flow			°C/W
θ <sub>JC</sub>	Junction-to-case thermal resistance	DGG			°C/W
T <sub>SD</sub>	Thermal shutdown temperature				°C

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2		0.8	V
V <sub>IL</sub>	Low-level input voltage				
V <sub>O</sub> , V <sub>I</sub> , or V <sub>IC</sub>	Voltage at any bus terminal (separately or common-mode)	–7		12	V
I <sub>O</sub>	Output current	Driver	–60	60	mA
		Receiver	–8	8	mA
T <sub>A</sub>	Operating free-air temperature	–40		85	°C

- (1) n = 1 - 9

**ELECTRICAL CHARACTERISTICS**

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN65HVD09			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OD</sub>   Driver differential output voltage magnitude	RS-422 load, R <sub>L</sub> = 100 Ω	See Figure 1	0.56	1.6	V	
	RS-485 load, R <sub>L</sub> = 54 Ω			1.4		
	Pull-Up Pull-Down Load	See Figure 2	1	1.5		
V <sub>OH</sub> High-level output voltage	A side, I <sub>OH</sub> = -8 mA, V <sub>ID</sub> = 200 mV,	See Figure 4	4	4.5	V	
	B side,	See Figure 2		3	V	
V <sub>OL</sub> Low-level output voltage	A side, I <sub>OH</sub> = 8 mA, V <sub>ID</sub> = -200 mV,	See Figure 4		0.6	0.8	V
	B side,	See Figure 2		1		V
V <sub>IT+</sub> Receiver positive-going differential input threshold voltages	I <sub>OH</sub> = -8 mA,	See Figure 4			0.2	V
V <sub>IT-</sub> Receiver negativegoing differential input threshold voltage	I <sub>OL</sub> = 8 mA,	See Figure 4	-0.2			V
V <sub>hys</sub> Receiver input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		24	45		mV
I <sub>I</sub> Bus input current	V <sub>IH</sub> = 12 V, V <sub>CC</sub> = 5 V,	Other input at 0 V			1	mA
	V <sub>IH</sub> = 12 V, V <sub>CC</sub> = 0,				1	mA
	V <sub>IH</sub> = -7 V, V <sub>CC</sub> = 5 V,		-0.8	-0.4		mA
	V <sub>IH</sub> = -7 V, V <sub>CC</sub> = 0,		-0.8	-0.3		mA
I <sub>IH</sub> High-level input current	nA, BSR, DE/ $\overline{RE}$ , and $\overline{CRE}$ ,	V <sub>IH</sub> = 2 V	-100			μA
	CDE0, CDE1, and CDE2,	V <sub>IH</sub> = 2V			100	μA
I <sub>IL</sub> Low-level input current	nA, BSR, DE/ $\overline{RE}$ , and $\overline{CRE}$ ,	V <sub>IL</sub> = 0.8 V	-100			μA
	CDE1, CDE1, and CDE2,	V <sub>IL</sub> = 0.8 V			100	μA
I <sub>OS</sub> Short circuit output current	nB+ or nB-				±260	mA
I <sub>OZ</sub> High-impedance-state output current	nA		See I <sub>IH</sub> and I <sub>IL</sub>			
	nB+ or nB-		See I <sub>IH</sub>			
I <sub>CC</sub> Supply current	Disabled				10	mA
	All drivers enabled, no load				60	
	All receivers enabled, no load				45	
C <sub>O</sub> Output capacitance	nB+ or nB- to GND			18		pF
C <sub>pd</sub> Power dissipation capacitance <sup>(2)</sup>	Receiver			40		pF
	Driver			100		

 (1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

 (2) C<sub>pd</sub> determines the no-load dynamic supply current consumption, I<sub>S</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f + I<sub>CC</sub>

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN65HVD09			UNIT
		MIN	TYP <sup>(1)</sup>	MAX	
$t_{pd}$ Propagation delay time, $t_{PHL}$ or $t_{PLH}$ (see <a href="#">Figure 2</a> and <a href="#">Figure 3</a> )		2.5		13.5	ns
$t_{sk(p)}$ Pulse skew, $ t_{PHL} - t_{PLH} $				5	ns
$t_f$ Fall time	S1 to B, See <a href="#">Figure 3</a>		4		ns
$t_r$ Rise time	See <a href="#">Figure 3</a>		8		ns
$t_{en}$ Enable time, control inputs to active output				50	ns
$t_{dis}$ Disable time, control inputs to high-impedance output				225	ns
$t_{PHZ}$ Propagation delay time, high-level to high-impedance output	See <a href="#">Figure 6</a> and <a href="#">Figure 7</a>		17	225	ns
$t_{PLZ}$ Propagation delay time, low-level to high-impedance output			25	225	ns
$t_{PZH}$ Propagation delay time, high-impedance to high-level output			17	50	ns
$t_{PZL}$ Propagation delay time, high-impedance to low-level output			17	50	ns

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN65HVD09			UNIT
		MIN	TYP <sup>(1)</sup>	MAX	
$t_{pd}$ Propagation delay time, $t_{PHL}$ or $t_{PLH}$ (see <a href="#">Figure 2</a> and <a href="#">Figure 3</a> )		8		14.5	ns
$t_{sk(lim)}$ Skew limit, maximum $t_{pd}$ – minimum $t_{pd}$ <sup>(2)</sup>				5	ns
$t_{sk(p)}$ Pulse skew, $ t_{PHL} - t_{PLH} $			0.6	5	ns
$t_t$ Transition time ( $t_r$ or $t_f$ )	See <a href="#">Figure 5</a>		2		ns
$t_{en}$ Enable time, control inputs to active output			31		ns
$t_{dis}$ Disable time, control inputs to high-impedance output			41		ns
$t_{PHZ}$ Propagation delay time, high-level to high-impedance output	See <a href="#">Figure 8</a> and <a href="#">Figure 9</a>		34		ns
$t_{PLZ}$ Propagation delay time, low-level to high-impedance output			14		ns
$t_{PZH}$ Propagation delay time, high-impedance to high-level output			30		ns
$t_{PZL}$ Propagation delay time, high-impedance to low-level output			30		ns

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This parameter is applicable at one  $V_{CC}$  and operating temperature within the recommended operating conditions and to any two devices.

PARAMETER MEASUREMENT INFORMATION

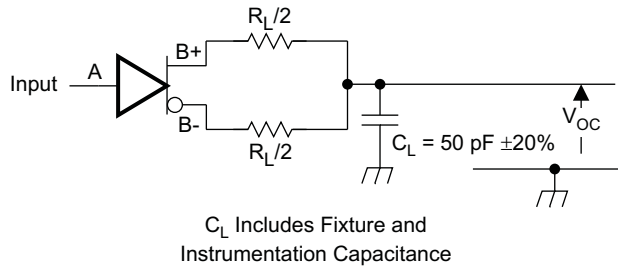
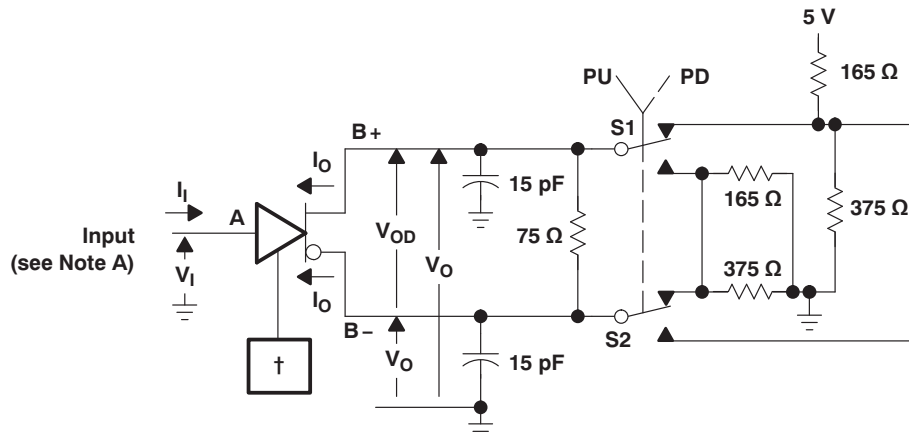


Figure 1. Driver Test Circuit, RS-422 and RS-485 Loading



† CDEO and DE/RE are at 2 V, BSR is at 0.8V, and all others are open.  
‡ All nine drivers are enabled, similarly loaded, and switching.

Figure 2. Driver Test Circuit, Pull-Up and Pull-Down Loading<sup>†</sup>

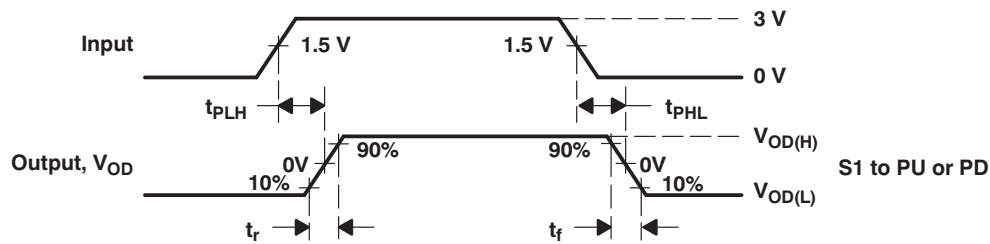
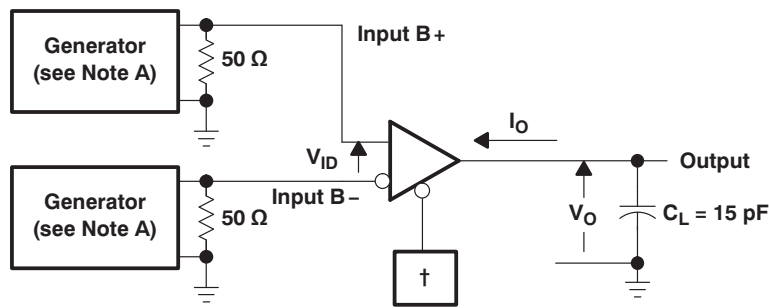


Figure 3. Driver Delay and Transition Time Test Waveforms



PARAMETER MEASUREMENT INFORMATION (continued)



† CDE0, CDE1, CDE2, BSR, CRE, and DE/RE at 0.8 V

‡ All nine receivers are enabled and switching.

Figure 4. Receiver Propagation Delay and Transition Time Test Circuit

- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .
- B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
- C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
- D. All indicated voltages are  $\pm 10$  mV.

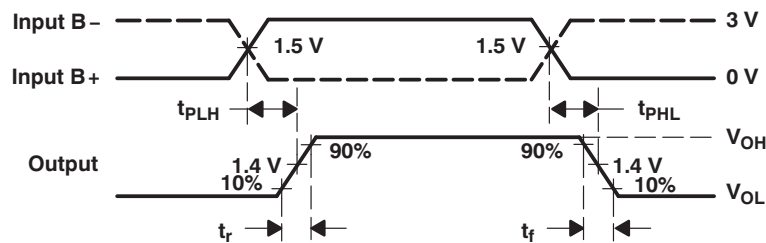
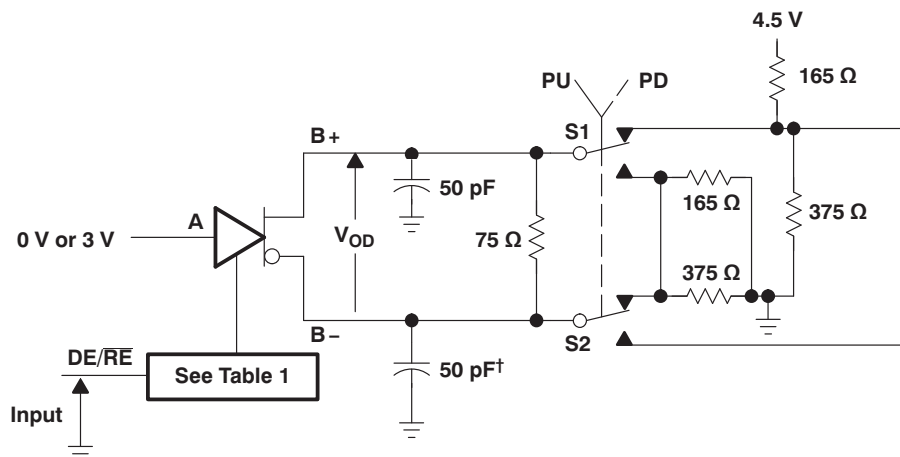


Figure 5. Receiver Delay and Transition Time Waveforms

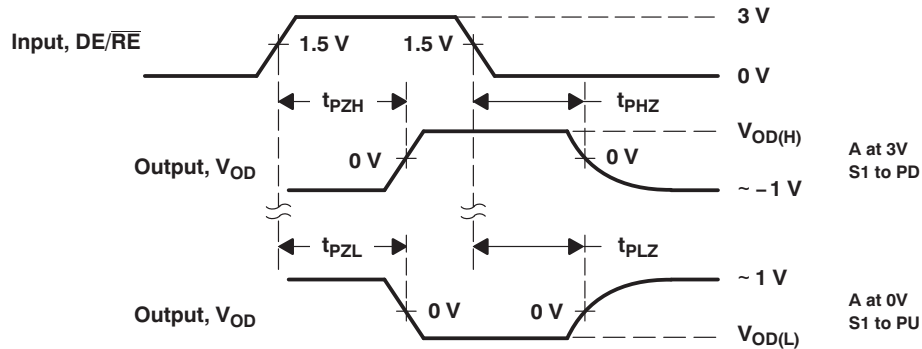


† Includes probe and jig capacitance in two places.

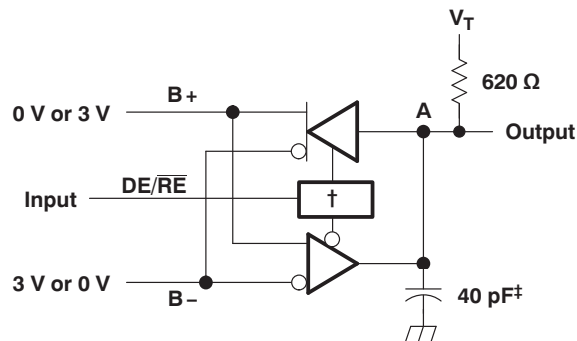
Figure 6. Driver Enable and Disable Time Test Circuit

**Table 1. Enabling for Driver Enable and Disable Time**

DRIVER	BSR	CDE0	CDE1	CDE2	$\overline{\text{CRE}}$
1–8	H	H	L	L	X
9	L	H	H	H	H


**Figure 7. Driver Enable Time Waveforms**

- NOTES:
- A. All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .
  - B. All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
  - C. All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
  - D. All indicated voltages are  $\pm 10$  mV.



† CDE0 is high, CDE1, CDE2, BSR, and  $\overline{\text{CRE}}$  are low, all others are open.

‡ Includes probe and jig capacitance.

**Figure 8. Receiver Enable and Disable Time Test Circuit**

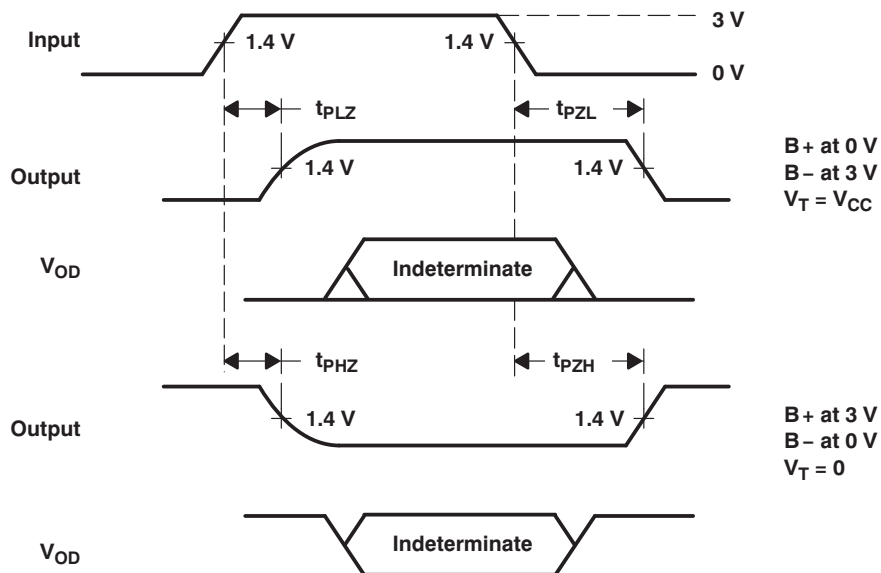


Figure 9. Receiver Enable and Disable Time Waveforms

- NOTES:
- All input pulses are supplied by a generator having the following characteristics:  $t_r \leq 6$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O = 50 \Omega$ .
  - All resistances are in  $\Omega$  and  $\pm 5\%$ , unless otherwise indicated.
  - All capacitances are in pF and  $\pm 10\%$ , unless otherwise indicated.
  - All indicated voltages are  $\pm 10$  mV.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT  
vs  
FREQUENCY

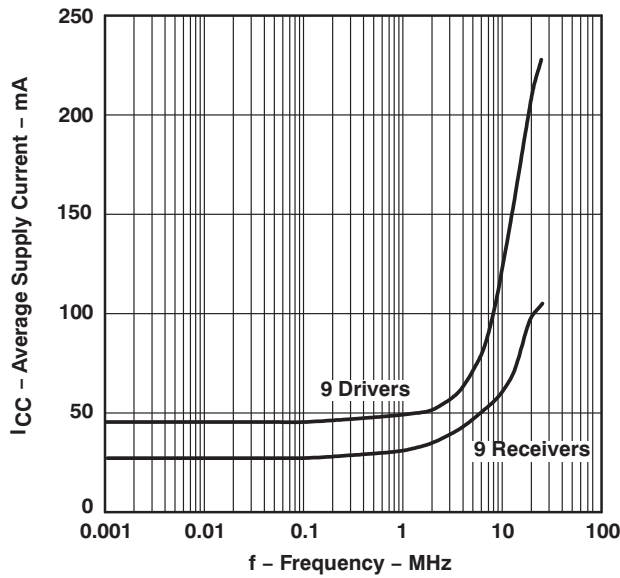


Figure 10.

LOGIC INPUT CURRENT  
vs  
INPUT VOLTAGE

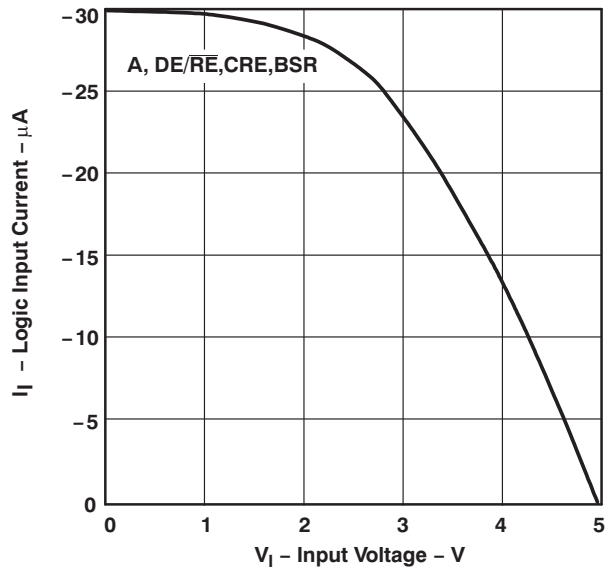


Figure 11.

BUS  
INPUT CURRENT  
vs  
INPUT VOLTAGE

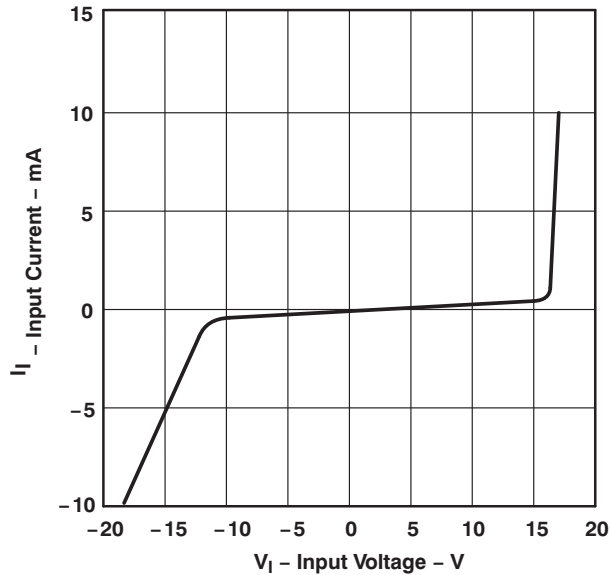


Figure 12.

DRIVER  
LOW-LEVEL OUTPUT VOLTAGE  
vs  
LOW-LEVEL OUTPUT CURRENT

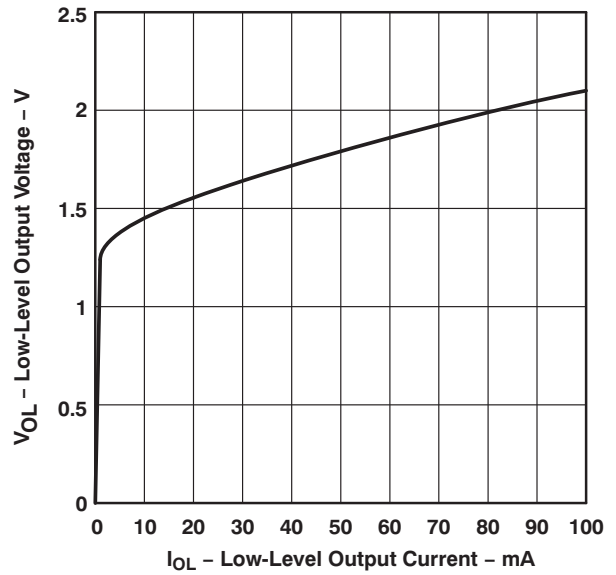


Figure 13.

TYPICAL CHARACTERISTICS (continued)

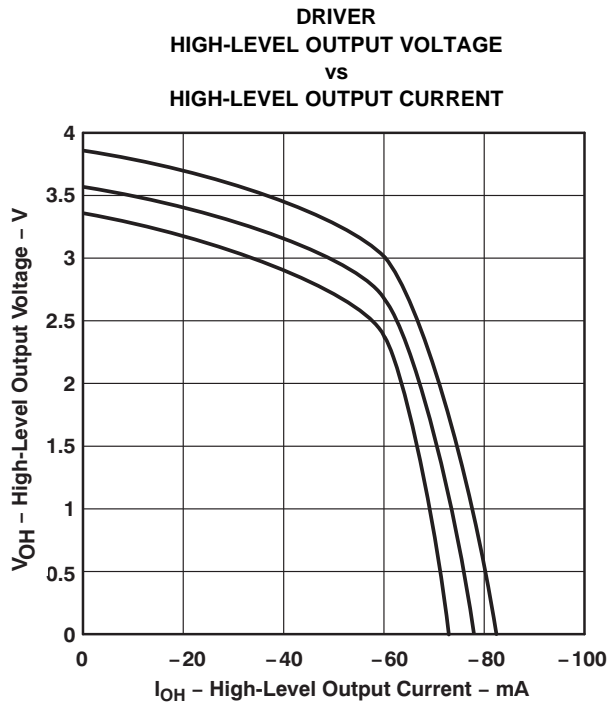


Figure 14.

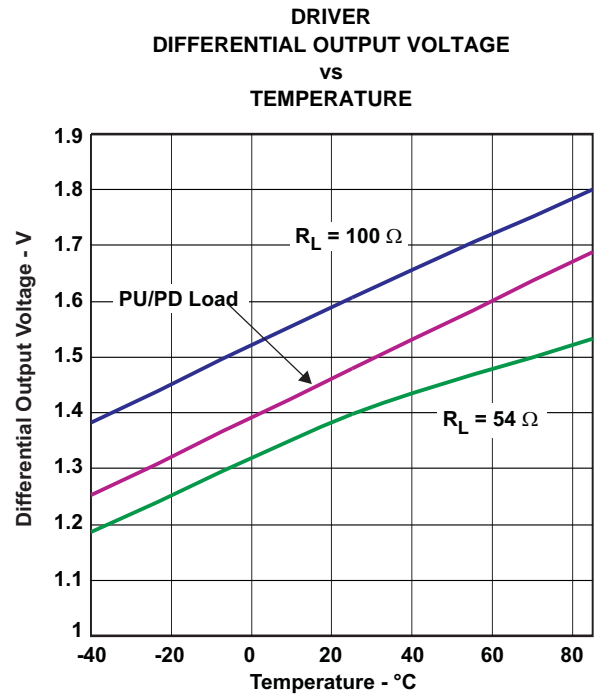


Figure 15.

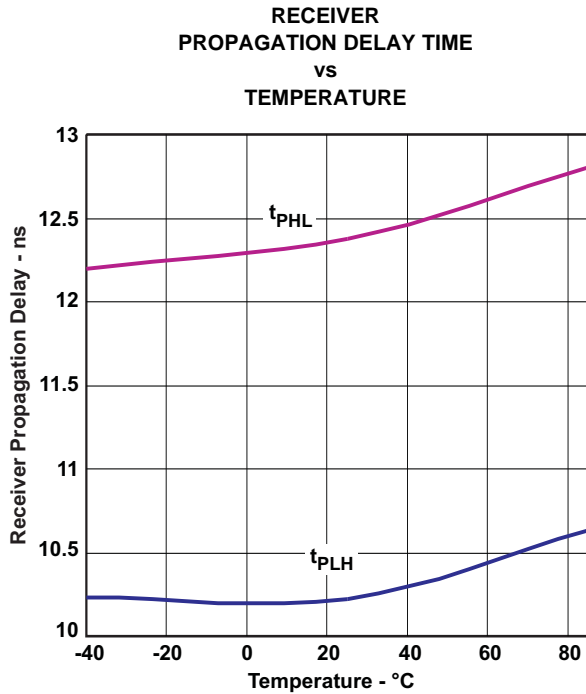


Figure 16.

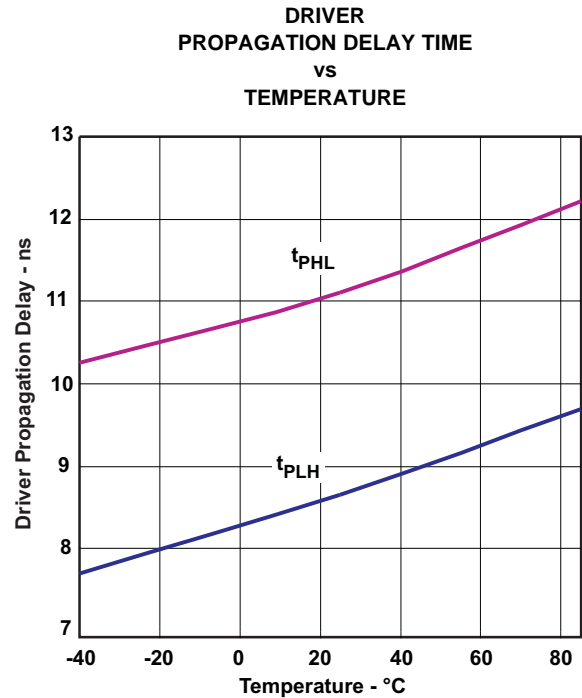


Figure 17.

TYPICAL CHARACTERISTICS (continued)

DRIVER  
OUTPUT CURRENT  
vs  
SUPPLY VOLTAGE

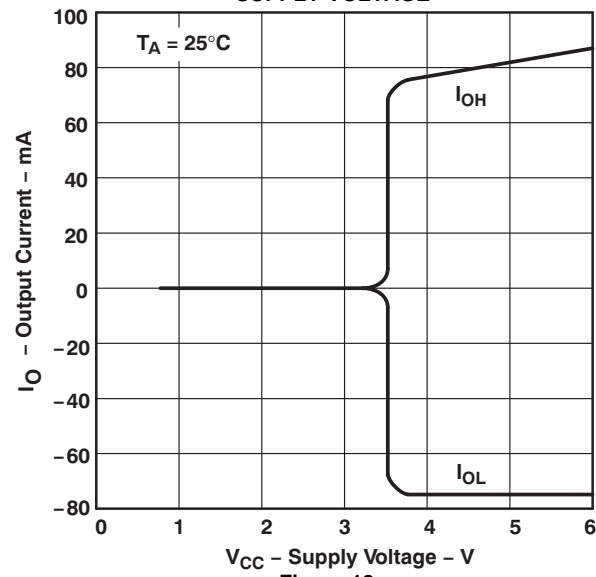
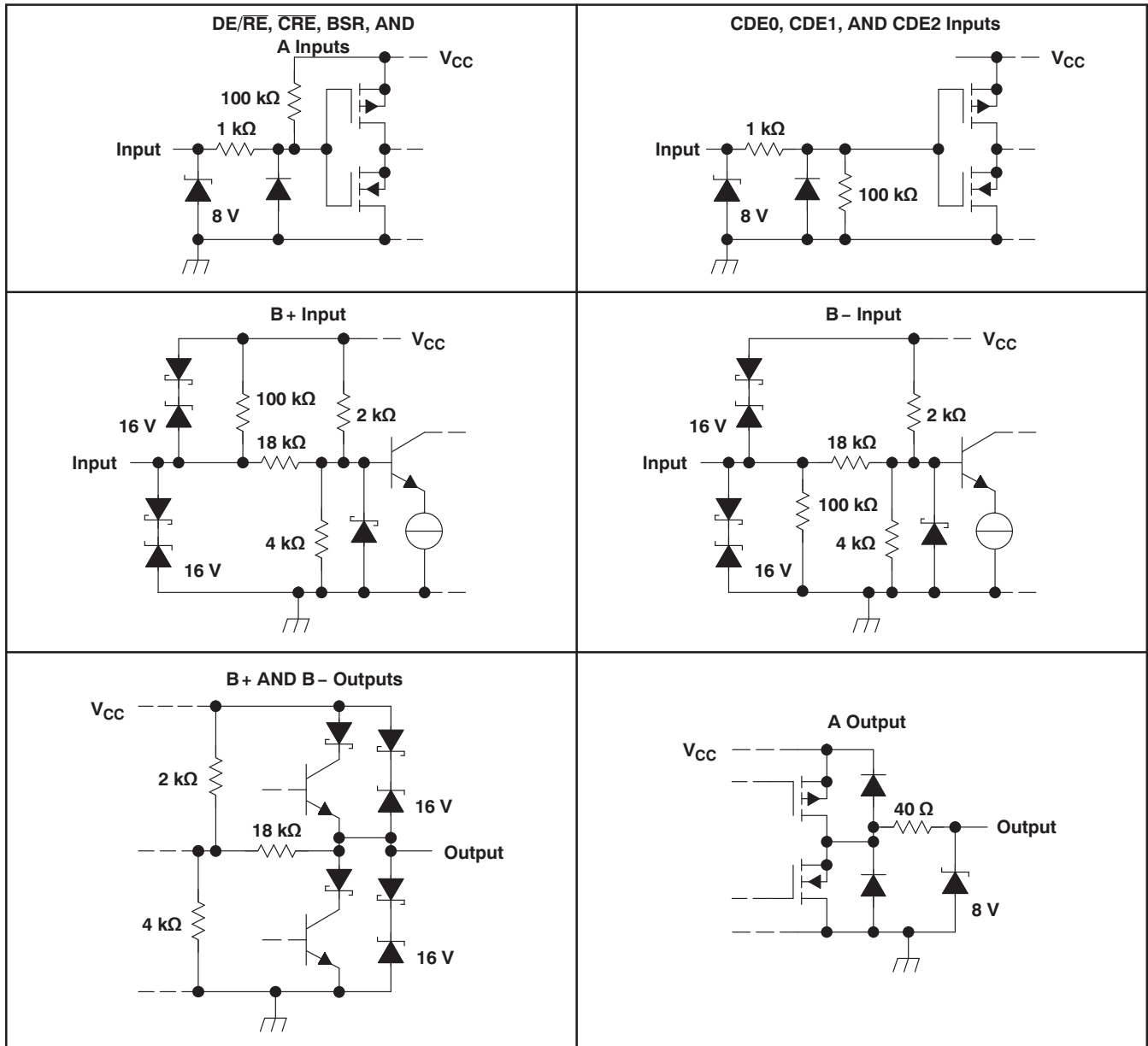
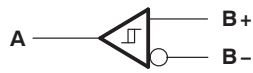


Figure 18.

TYPICAL CHARACTERISTICS (continued)  
SCHEMATICS OF INPUTS AND OUTPUTS

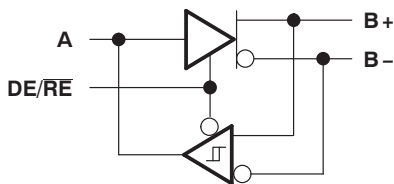


**APPLICATION INFORMATION**
**FUNCTION TABLES**
**RECEIVER**


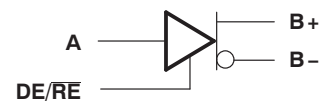
INPUTS		OUTPUT A
B+ <sup>1</sup>	B- <sup>1</sup>	
L	H	L
H	L	H

**DRIVER**

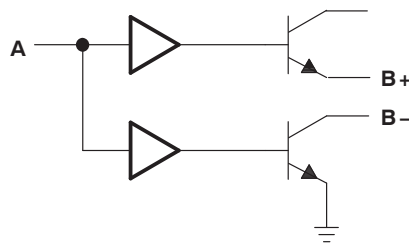

INPUT A	OUTPUTS	
	B+	B-
L	L	H
H	H	L

**TRANSCEIVER**


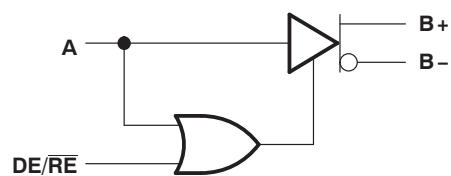
DE/RE	INPUTS			OUTPUTS		
	A	B+ <sup>1</sup>	B- <sup>1</sup>	A	B+	B-
L	-	L	H	L	-	-
L	-	H	L	H	-	-
H	L	-	-	-	L	H
H	H	-	-	-	H	L

**DRIVER WITH ENABLE**


DE/RE	INPUTS		OUTPUTS	
	A	B+ <sup>1</sup>	B+	B-
L	L	-	Z	Z
L	H	-	Z	Z
H	L	-	L	H
H	H	-	H	L

**WIRED-OR DRIVER**


INPUT A	OUTPUTS	
	B+	B-
L	Z	Z
H	H	L

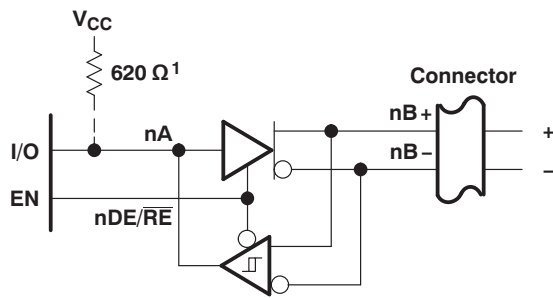
**TWO-ENABLE INPUT DRIVER**


DE/RE	INPUTS		OUTPUTS	
	A	B+ <sup>1</sup>	B+	B-
L	L	-	Z	Z
L	H	-	H	L
H	L	-	L	H
H	H	-	H	L

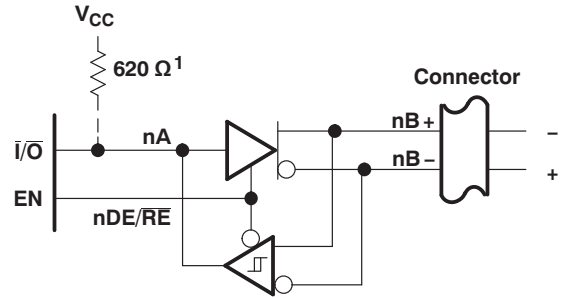
NOTE: H = high level, L = low level, X = irrelevant, Z = high impedance (off)

- (1) An H in this column represents a voltage of 200 mV or higher than the other bus input. An L represents a voltage of 200 mV or lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

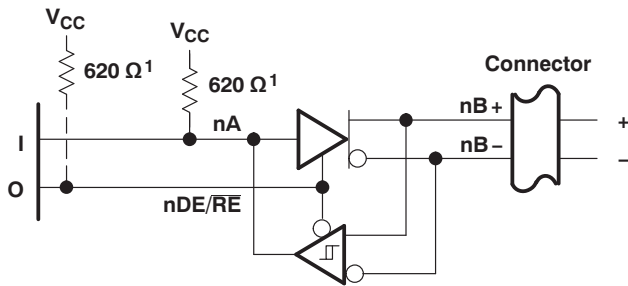




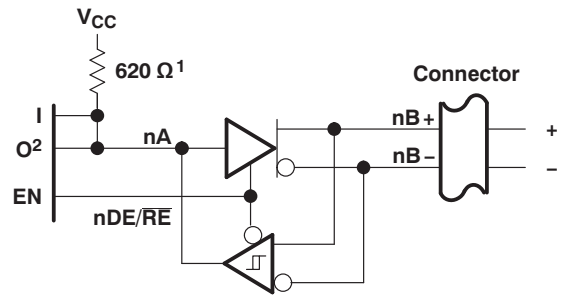
(a) ACTIVE-HIGH BIDIRECTIONAL I/O WITH SEPARATE ENABLE



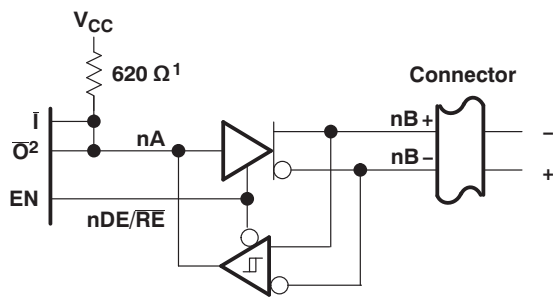
(b) ACTIVE-LOW BIDIRECTIONAL I/O WITH SEPARATE ENABLE



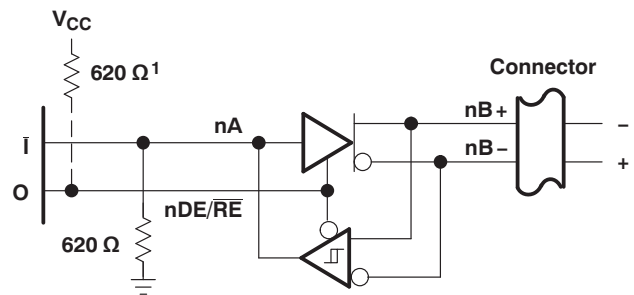
(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT



(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT, AND ENABLE



(e) SEPARATE ACTIVE-LOW INPUT AND OUTPUT AND ACTIVE-HIGH ENABLE



(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

1: When 0 is open drain

2: Must be open-drain or 3-state output

(1) When 0 is open drain

(2) Must be open-drain or 3-state output

NOTE: The BSR,  $\overline{\text{CRE}}$ , A, and  $\text{DE}/\overline{\text{RE}}$  inputs have internal pullup resistors. CDE0, CDE1, and CDE2 have internal pulldown resistors.

Figure 19. Typical Transceiver Connections

**CHANNEL LOGIC CONFIGURATIONS WITH CONTROL INPUT LOGIC**

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; the BSR, CDE0, CDE1, CDE2, and CRE bit values are shown below the diagrams. Channel 1 is at the top of the logic diagrams; channel 9 is at the bottom of the logic diagrams.

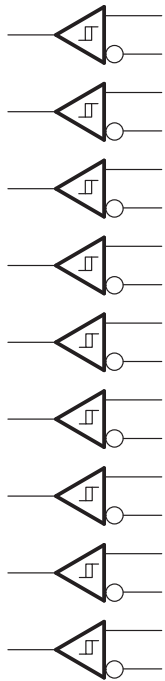


Figure 19. 00000

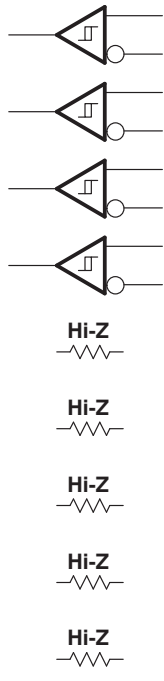


Figure 20. 00001

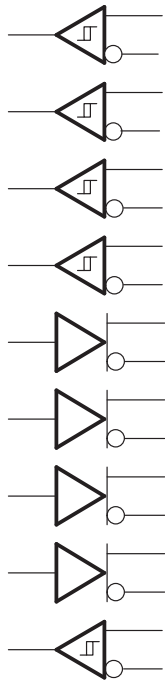


Figure 21. 00010

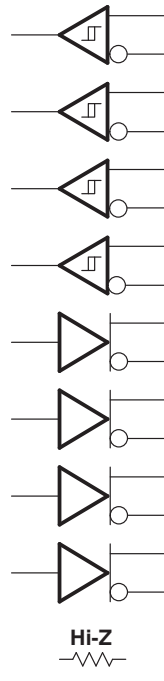


Figure 22. 00011

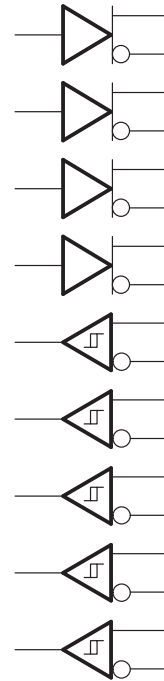


Figure 23. 00100

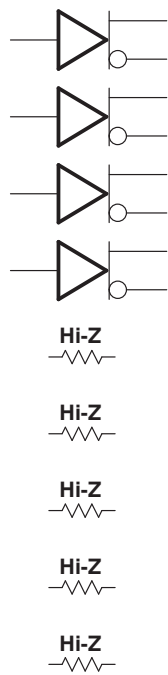


Figure 24. 00101

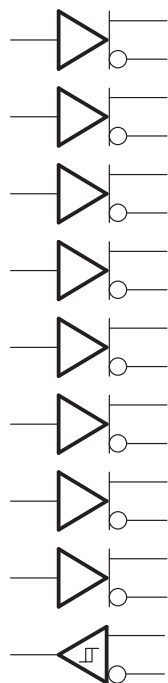


Figure 25. 00110

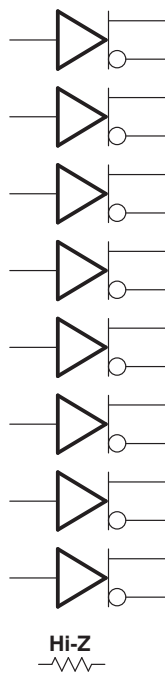


Figure 26. 00111

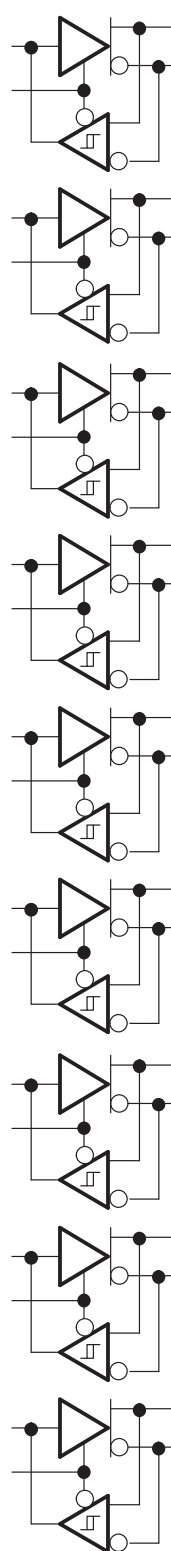


Figure 27. 01000

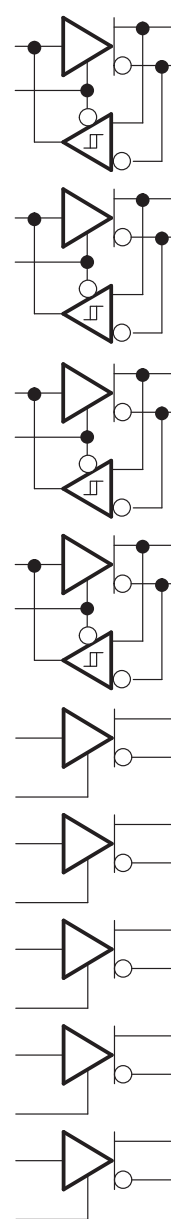
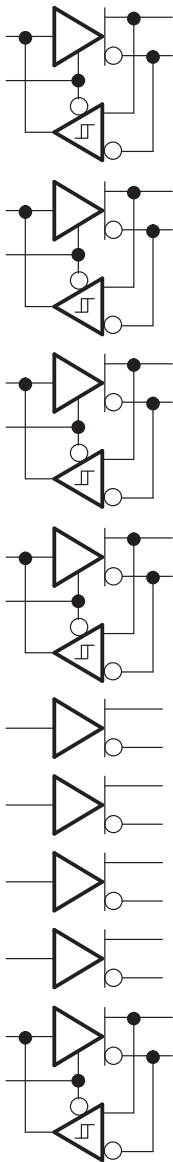
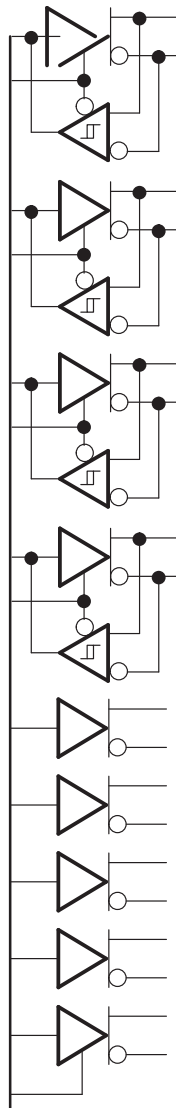


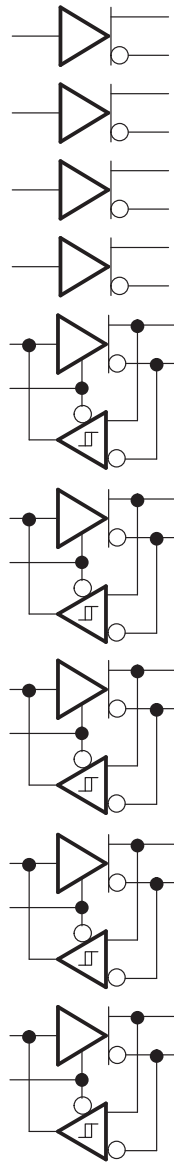
Figure 28. 01001



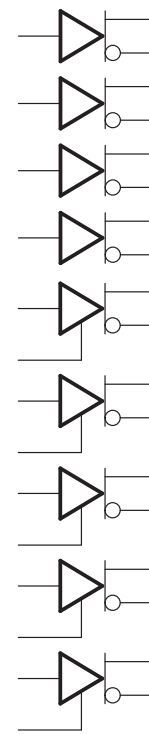
**Figure 29. 01010**



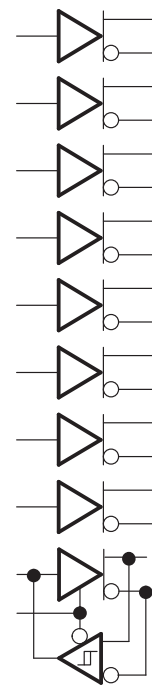
**Figure 30. 01011**



**Figure 31. 01100**



**Figure 32. 01101**



**Figure 33. 01110**

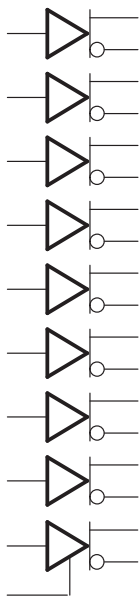


Figure 34. 01111

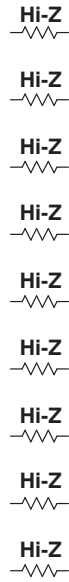


Figure 35. 10000 and 10001

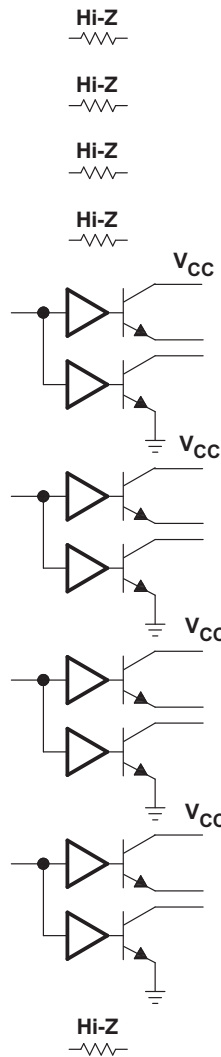


Figure 36. 10010 and 10011

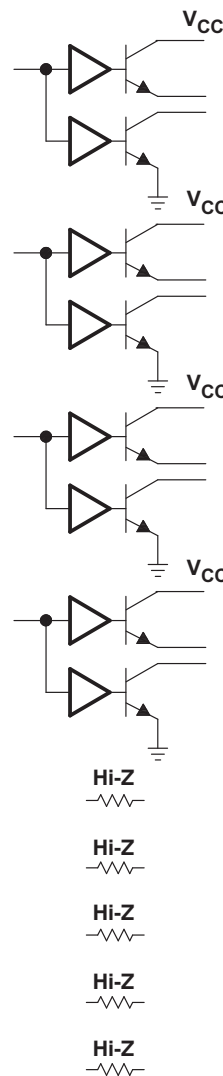


Figure 37. 10100 and 10101

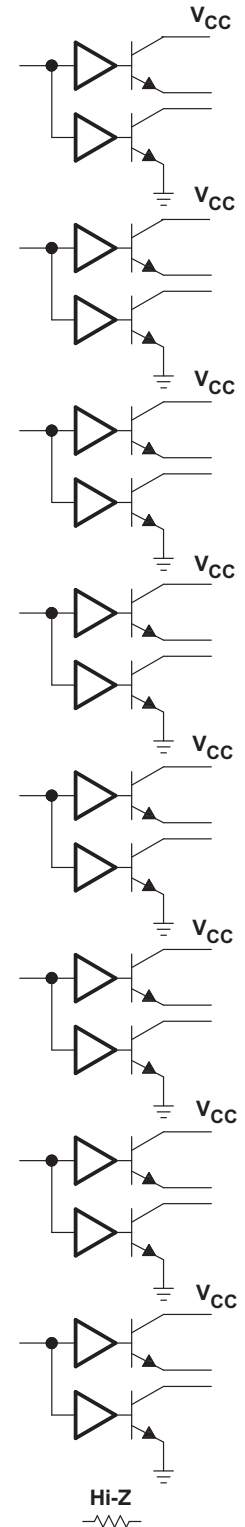


Figure 38. 10110 and 10111

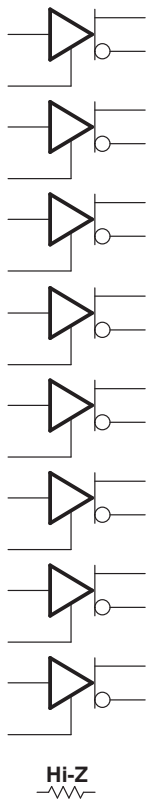


Figure 39. 11000 and 11001

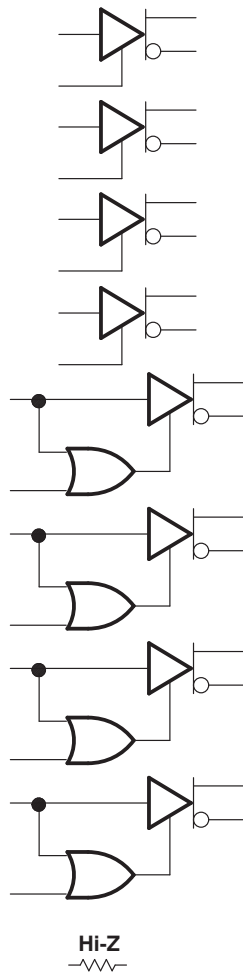


Figure 40. 11010 and 11011

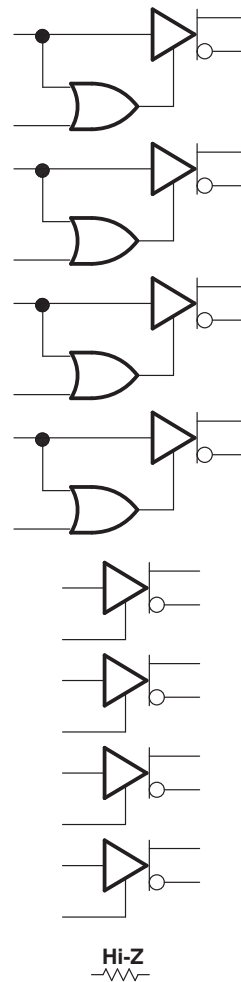


Figure 41. 11100 and 11101

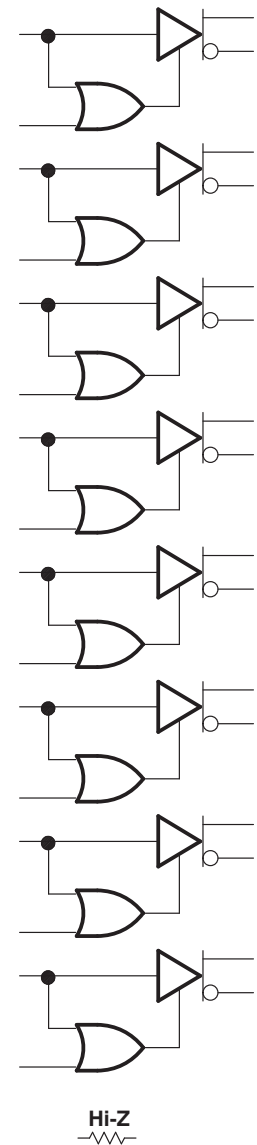


Figure 42. 11110 and 11111

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN65HVD09IDGGREP	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
V62/12607-01XE	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN65HVD09-EP :**

- Catalog: [SN65HVD09](#)

NOTE: Qualified Version Definitions:

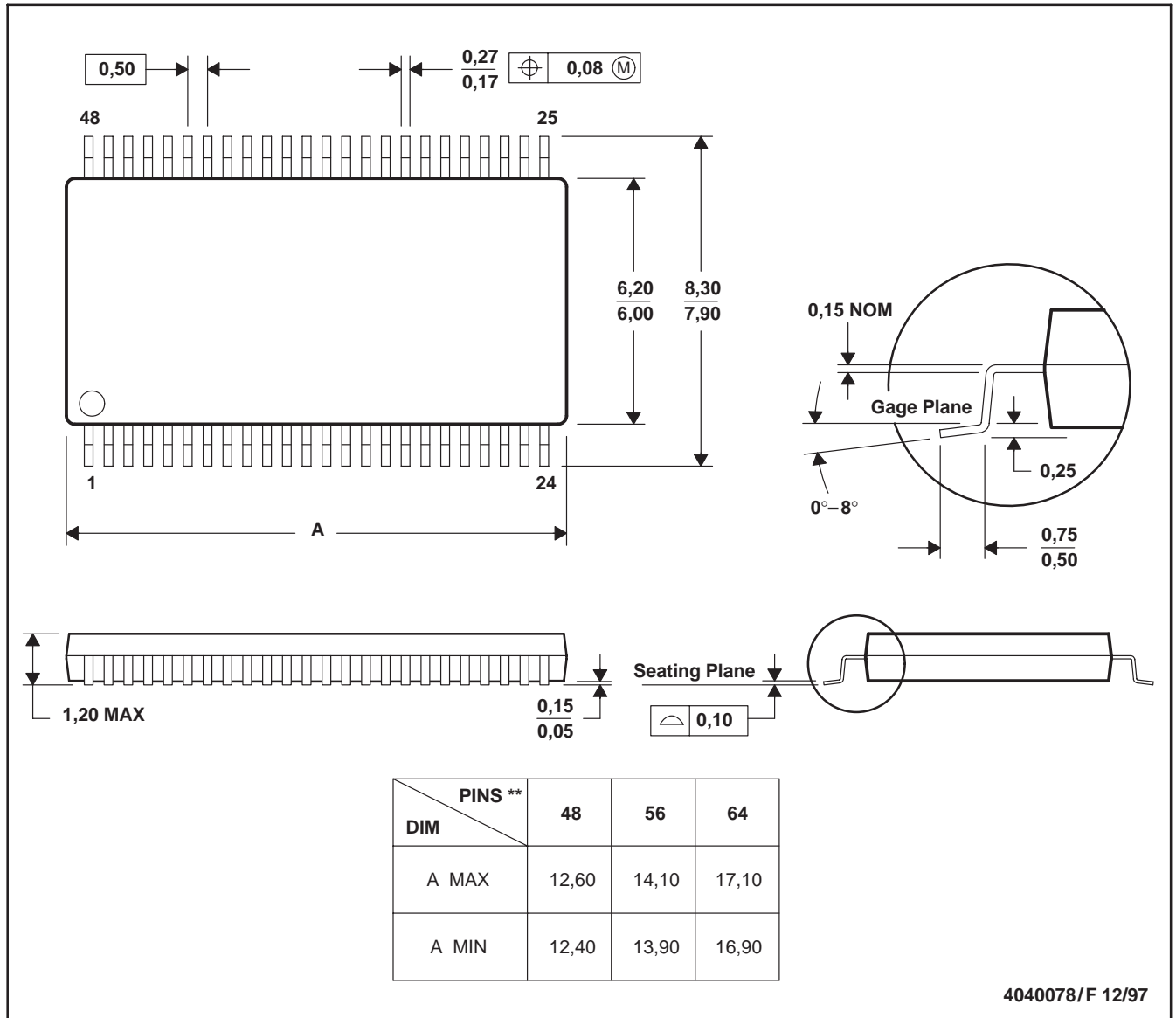
- Catalog - TI's standard catalog product



DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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