IO-LINK PHY for Device Nodes

Check for Samples: SN65HVD101, SN65HVD102

FEATURES

- **Configurable CQ Output: Push-Pull, High-Side, or Low-Side for SIO Mode**
- **Remote Wake-Up Indicator**
- **Current Limit Indicator**
- **Power-Good Indicator**
- **Overtemperature Protection**
- **Reverse Polarity Protection**
- **Configurable Current Limits**
- **9-V to 36-V Supply Range**
- **Tolerant to 50-V Peak Line Voltage**
- **3.3-V/5-V Configurable Integrated LDO (SN65HVD101 ONLY)**
- **20-pin QFN Package, 4 mm × 3.5 mm**

APPLICATIONS

- **Suitable for IO-Link Device Nodes**

DESCRIPTION

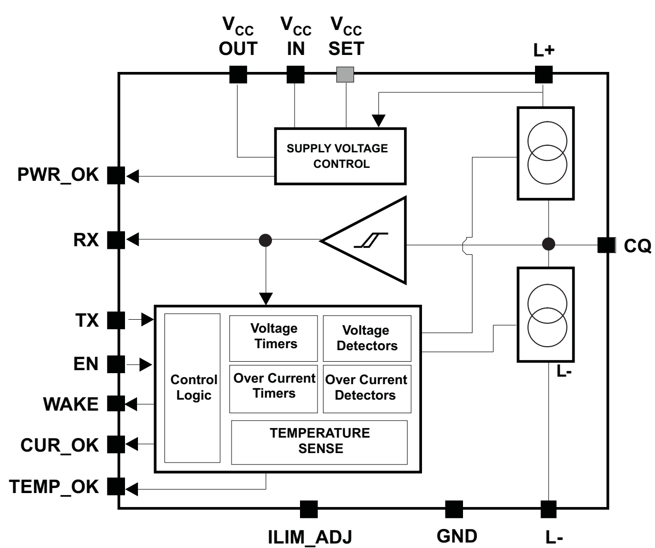
The SN65HVD101 and 'HVD102 IO-LINK PHYs implement the IO-LINK interface for industrial point-to-point communication. When the device is connected to an IO-Link master through a 3-wire interface, the master can initiate communication and exchange data with the remote node while the SN65HVD10X acts as a complete physical layer for the communication.

The IO-LINK driver output (CQ) can be used in push-pull, high-side, or low-side configurations using the EN and TX input pins. The PHY receiver converts the 24-V IO-LINK signal on the CQ pin to standard logic levels on the RX pin. A simple parallel interface is used to receive and transmit data and status information between the PHY and the local controller.

The SN65HVD101 and 'HVD102 implement protection features for overcurrent, overvoltage and overtemperature conditions. The IO-Link driver current limit can be set using an external resistor. If a short-circuit current fault occurs, the driver outputs are internally limited, and the PHY generates an error signal (SC). These devices also implement an overtemperature shutdown feature that protects the device from high-temperature faults.

The SN65HVD102 operates from a single external 3.3-V or 5-V local supply. The SN65HVD101 integrates a linear regulator that generates either 3.3 V or 5 V from the IO-Link L+ voltage for supplying power to the PHY as well as a local controller and additional circuits.

The SN65HVD101 and 'HVD102 are available in the 20-pin RGB package (4 mm × 3,5 mm QFN) for space-constrained applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

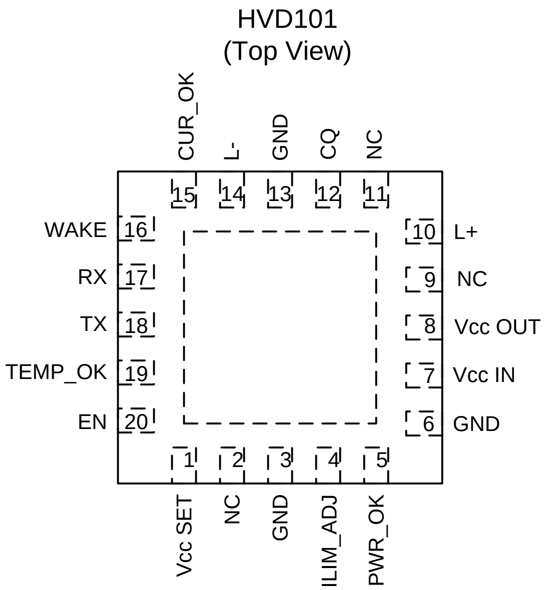
PIN DESCRIPTIONS

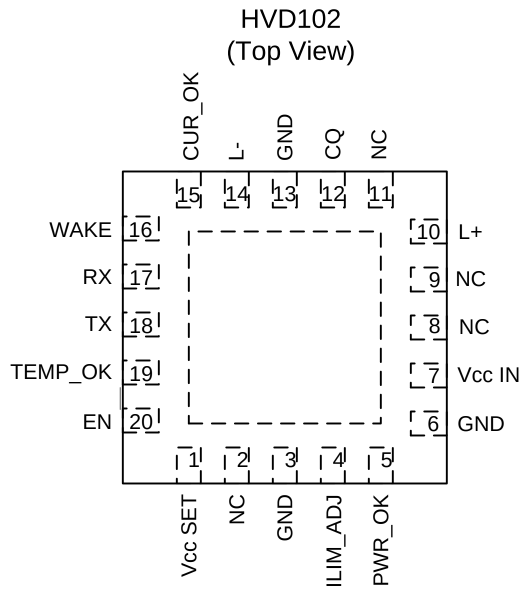
The definitions below define the functionality for each pin.

Type: I	Input	Type: O	CMOS Output
Type: I/O	Input/Output	Type: OD	Open Drain Output
Type: A	Analog	Type: P	Power

PIN FUNCTIONS

SIGNAL NAME	TYPE	PIN	DESCRIPTION
IO-LINK Interface			
L+	P	10	IO-Link supply voltage (24V nominal)
CQ	I/O	12	IO-Link data signal (bi-directional)
L–	P	14	IO-Link ground (connect to GND on board)
Local Controller Interface			
CUR_OK	OD	15	High-CQ-current fault indicator output signal from PHY to the microcontroller, a LOW level indicates over-current condition
WAKE	OD	16	Wake up indicator from the PHY to the local controller
RX	O	17	PHY data output to the local controller
TX	I	18	PHY data input from the local controller
EN	I	20	Driver enable control from the local controller
Power Supply Pins			
V_{CC} IN	A	7	Voltage supply input (HVD102) Voltage sense feedback input for voltage regulator (HVD101) - connect to pin 8 either directly or through a current boost transistor.
V_{CC} OUT	P	8	Output voltage from the voltage regulator (HVD101) - connect to pin 7 either directly or through a current boost transistor. No connect (HVD102)
GND	P	3, 6, 13	Ground pins
Special connect pins			
V_{CC} SET	I	1	If this pin is left floating then the Vcc supply is 5V. If this pin is connected to GND, then the Vcc supply is 3.3V
ILIMADJ	A	4	Sets the CQ Output Current. A resistor R_{SET} is connected to this pin. The output current is defined as V_{REF} / (R_{INT} + R_{SET}) × K_{SET}.
PWR_OK	OD	5	Power Good signal. A high impedance on this pin indicates that the L+ and Vcc outputs are at correct levels.
Temp_OK	OD	19	Temperature Good signal. A high impedance on this pin indicates that the internal temperature is at a safe level. If the internal device temperature reaches a level approaching the thermal shutdown temperature, this pin will go to an active low state.
NC		2, 9, 11	No Connect. Leave these pins floating (open)





In normal operation, the PHY sets the output state of the CQ pin when the driver is enabled. During fault conditions, the driver may be disabled by internal circuits.

Table 1. Driver Function

EN	TX	CQ	COMMENT
L or OPEN	X	Z	PHY is in ready-to-receive state
H	L	H	PHY CQ is sourcing current (high-side drive)
H	H or OPEN	L	PHY CQ is sinking current (low-side drive)

Table 2. Receiver Function

CQ Voltage	RX	Comment
VCQ < VTHL	H	Normal receive mode, input low
VTHL < VCQ < VTHH	?	Indeterminate output, may be either H or L
VTHH < VCQ	L	Normal receive mode, input high
OPEN	H	Failsafe output high

Table 3. Wake Up Function

EN	TX	CQ VOLTAGE	WAKE	COMMENT
L	X	X	Z	PHY is in ready-to-receive state
H	L	$V_{THH} < V_{CQ}$ (t_{WU})	L	PHY receives High-level wake-up request from Master
H	X	$V_{THL} < V_{CQ} < V_{THH}$	?	Indeterminate output, may be either H or L
H	H	$V_{CQ} < V_{THL}$ (t_{WU})	L	PHY receives Low-level wake-up request from Master

Table 4. Current Limit Indicator Function

CQ CURRENT	CUR_OK	COMMENT
|ICQ| < IO(LIM)	Z	Normal operation
|ICQ| > IO(LIM)	L	CQ current is at the internal limit

Table 5. Temperature Indicator Function

Internal Temperature	Overtemp (Internal)	TEMP_OK	Comment
$T < T_{WARN}$	not overtemp	Z	Normal operation
$T_{WARN} < T\uparrow < T_{SD}$	not overtemp	L	Temperature warning
$T_{SD} < T$	overtemp disable	L	Overtemp disable
$T_{WARN} < T\downarrow < T_{RE}$	not overtemp	L	Temperature recovery

Table 6. Power Supply Indicator Function

V_{L+}	V_{CC}	PWR_OK	Comment
$V_{L+} < V_{PG1}$	$V_{POR2} < V_{CC} < V_{PG2}$	L	Both supplies too low
$V_{PG1} < V_{L+}$	$V_{POR2} < V_{CC} < V_{PG2}$	L	V_{CC} too low
$V_{L+} < V_{PG1}$	$V_{PG2} < V_{CC}$	L	V_{L+} too low
$V_{PG1} < V_{L+}$	$V_{PG2} < V_{CC}$	Z	Both supplies correct

THERMAL INFORMATION

THERMAL METRIC(1)		SN65HVD10x RGB PACKAGE 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	33.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	36.6	
θ_{JB}	Junction-to-board thermal resistance	10.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	10.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.3	
T_{STG}	Storage temperature	65 to 150	°C

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE MIN	MAX	UNIT
V	L+, CQ	Line voltage – steady state	–40	+40(2) (3)	V
	L+, CQ	Line Voltage – transient, pulse width <100us		+50	V
	V_{CC}	Supply voltage	–0.3	6	V
	TX, EN, V_{CC}_SET, ILIMADJ,	Input voltage	–0.3	6	V
	RX, CUR_OK, WAKE, PWR_OK	Output voltage	–0.3	6	V
I_O	RX, CUR_OK, WAKE, PWR_OK	Output current	TBD		mA
Tstg		Storage temperature	–65	150	°C
TJ		Die temperature		180	°C
ESD		HBM (all pins)		2	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with reference to the GND pin, unless otherwise specified.
(3) GND pin and L- line should be at the same DC potential

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{L+}	Line voltage(1)		9	24	30	V
V_{CC}	Logic supply voltage (3.3V nominal)		3	3.3	3.6	V
V_{CC}	Logic supply voltage (5V nominal)		4.5	5	5.5	V
V_{IL}	Logic low input voltage				0.8	V
V_{IH}	Logic high input voltage		2			V
I_O	Logic output current		–4		4	mA
$I_{CC(OUT)}$	Logic supply current (HVD101)				20	mA
$I_{O(LIM)}$	CQ driver output current limit		100		450	mA
R_{SET}	External resistor for CQ current limit		0		20	kΩ
C_{COMP}	Compensation capacitor for voltage regulator (HVD101)		3.3			µF
$1/t_{BIT}$	Signaling rate	IO-Link mode			250	kbps
		SIO mode			10	
T_A	Ambient temperature		–40		105	°C
T_J	Junction temperature		–40		150	°C
P_D	Power dissipation		see Thermal Characteristics table			

(1) These devices will operate with line voltage as low as 9V and as high as 36V, however, the parametric performance is optimized for the IO-Link specified supply voltage range of 18V to 30V.

DEVICE CHARACTERISTICS

over all operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver Characteristics							
I_{IN}	Input current (TX, EN)	VIN = 0V to V_{CC}		–100		100	µA
VRQH	Residual voltage across the driver high side switch	ICQ = –250 mA	$18 < V_{L+}$	1.5		3	V
			$V_{L+} < 18$			3.5	V
		ICQ = –200 mA	$18 < V_{L+}$			2	V
			$V_{L+} < 18$			2.5	V
VRQL	Residual voltage across the driver low side switch	ICQ = 250 mA	$18 < V_{L+}$	1.5		3	V
			$V_{L+} < 18$			3.5	V
		ICQ = 200 mA	$18 < V_{L+}$			2	V
			$V_{L+} < 18$			2.5	V
t_{PLH}, t_{PHL}	Driver propagation delay	TX to CQ	Figure 1, Figure 2, Figure 3, R_L = 2 kΩ, C_L = 5 nF R_{SET} = 0 Ω		1	2	µs
$t_{P(skew)}$	Driver propagation delay skew				0.2		µs
t_{PZH}, t_{PZL}	Driver enable delay (EN to CQ)	18V < V_{L+} < 30 V				5	µs
		9V < V_{L+} < 18 V				8	µs
t_{PHZ}, t_{PLZ}	Driver disable delay	18V < V_{L+} < 30 V				5	µs
		V_{L+} < 18 V				8	µs
t_r , t_f	Driver output rise, fall time	18V < V_{L+}				896	ns
$\lvert t_r – t_f \rvert$	Difference in rise and fall time					300	ns
$\lvert I_{O(LIM)} \rvert$	Driver output current limit	R_{SET} = 20 kΩ		60	95	130	mA
		R_{SET} = 0 kΩ		300	400	480	mA
K_{SET}	Scale factor for current limit	See the Typical Characterisitics					
$I_{(OZ)}$	CQ leakage current with EN = L	VCQ = 8 V		–2		2	µA
RECEIVERS CHARACTERISTICS							
V_{THH}	Input threshold "H"	18 V < V_{L+} < 30 V		10.5		13	V
V_{THL}	Input threshold "L"			8		11.5	V
V_{HYS}	Receiver Hysteresis (V_{THH} – V_{THL})			0.5	1		V

DEVICE CHARACTERISTICS (continued)

over all operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{THH}	Input threshold "H"		9 V < V_{L+} < 18 V		Note [(1)]		Note[(2)]	V
V_{THL}	Input threshold "L"				Note [(3)]		Note[(4)]	V
V_{HYS}	Receiver Hysteresis (V_{THH}–V_{THL})				0.25			V
V_{OL}	Output low voltage	RX	I_{OL} = 4 mA				0.4	V
		OD outputs	I_{OL} = 1 mA				0.4	
V_{OH}	Output high voltage	RX	I_{OH} = –4 mA		V_{CC}–0.5			V
I_{OZ}	Output leakage current	OD outputs	Output in Z state, V_O = V_{CC}			.03	1	µA
t_{WU1}	Wake-up recognition begin		See Figure 6		45	60	75	µs
t_{WU2}	Wake-up recognition end				85	100	135	
t_{WAKE}	Wake-up output delay						155	
t_{ND}	Noise suppression time [(5)]						250	ns
tpR	Receiver propagation delay		See Figure 4	18 V < V_{L+}		300	600	ns
				V_{L+} < 18 V			800	ns
PROTECTION THRESHOLDS								
T_{SD}	Shutdown temperature		Die Temperature		160	175	190	°C
T_{RE}	Re-enable temperature [(6)]				110	125	140	
T_{WARN}	Thermal warning temperature (TEMP_OK)				120	135	150	
t_{pSC}	Current limit indicator delay				85		175	µs
V_{PG1}	V_{L+} threshold for PWR_OK				8		10	V
V_{PG2}	V_{CC} threshold for PWR_OK		V_{CC} Set = GND		2.45	2.75	3	V
			V_{CC} Set = OPEN		3.9	4.25	4.6	
V_{POR1}	Power-on Reset for V_{L+}					6		V
V_{POR2}	Power-on Reset for V_{CC}					2.5		V
VOLTAGE REGULATOR CHARACTERISTICS (HVD101)								
V_{CC}	Voltage regulator output		18 V < V_{L+} < 30 V	V_{CC}_SET is OPEN	4.5	5	5.5	V
				V_{CC}_SET to GND	3	3.3	3.6	
	Voltage regulator output		9 V < V_{L+} < 18 V	V_{CC}_SET is OPEN	4.5	5	5.5	V
				V_{CC}_SET to GND	3	3.3	3.6	
	Voltage regulator drop-out voltage (V_{L+} – V_{CC})		I_{CC} = 20 mA load current			3.2	3.9	V
	Line regulation		9 V < V_{L+} < 30 V, I_{VCC} = 1 mA			4		mV/V
	Load regulation		V_{L+} = 24 V, I_{VCC} = 100 µA to 20 mA			1.3%	5%	
	PSRR		100 kHz, I_{VCC} = 20 mA		30	40		dB
SUPPLY CURRENT								
I_{L+}	Quiescent supply current, Driver disabled		No Load	HVD102		1	2	mA
				HVD101		1.3	3	
	Dynamic supply current, Driver disabled		L+ = 24V, No Load 1/t_{BIT} = 250 kbps	HVD101		2		mA
	Dynamic supply current, Driver enabled			HVD102		1.5		
					See Typical Characteristics			mA

(1) $V_{THH}(min) = 5V + (11/18)[V_{L+} - 9V]$
(2) $V_{THH}(max) = 6.5V + (13/18)[V_{L+} - 9V]$
(3) $V_{THL}(min) = 4V + (8/18)[V_{L+} - 9V]$
(4) $V_{THL}(max) = 6V + (11/18)[V_{L+} - 9V]$
(5) Noise suppression time is defined in the IO-Link standard as the permissible duration of a receive signal above/below the detection threshold without detection taking place.
(6) T_{RE} is always less than T_{WARN} so TEMP_OK is de-asserted (high impedance) when the device is re-enabled

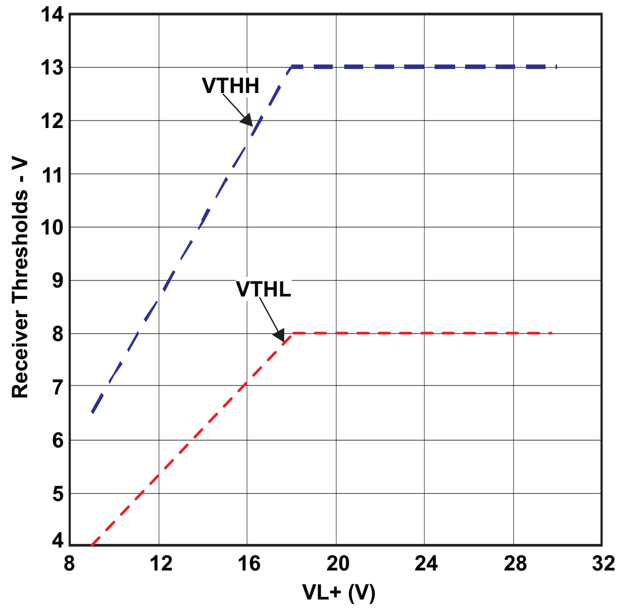


Figure 1. Receiver Threshold Boundaries

PARAMETER MEASUREMENT

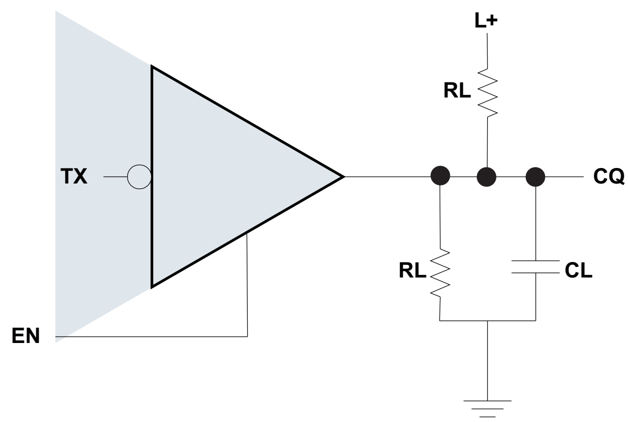


Figure 2. Test Circuit for Driver Switching

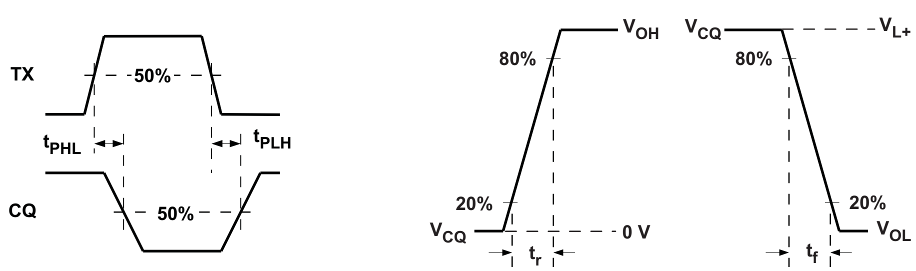


Figure 3. Waveforms for Driver Output Switching Measurements

PARAMETER MEASUREMENT (continued)

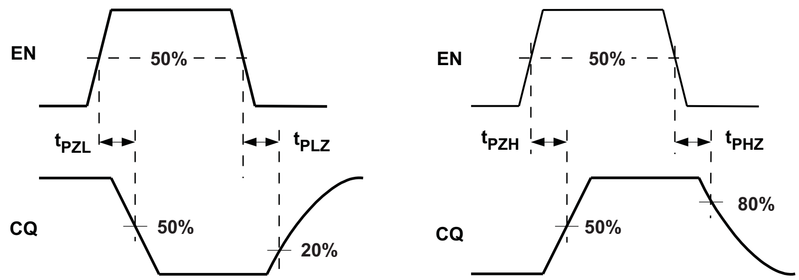


Figure 4. Waveform for Driver Enable/Disable Time Measurements

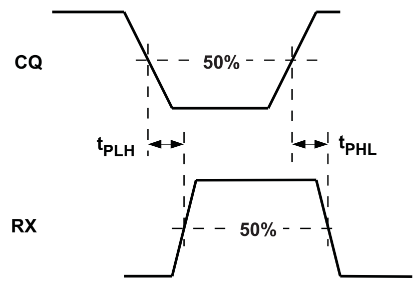


Figure 5. Receiver switching measurements

APPLICATION INFORMATION

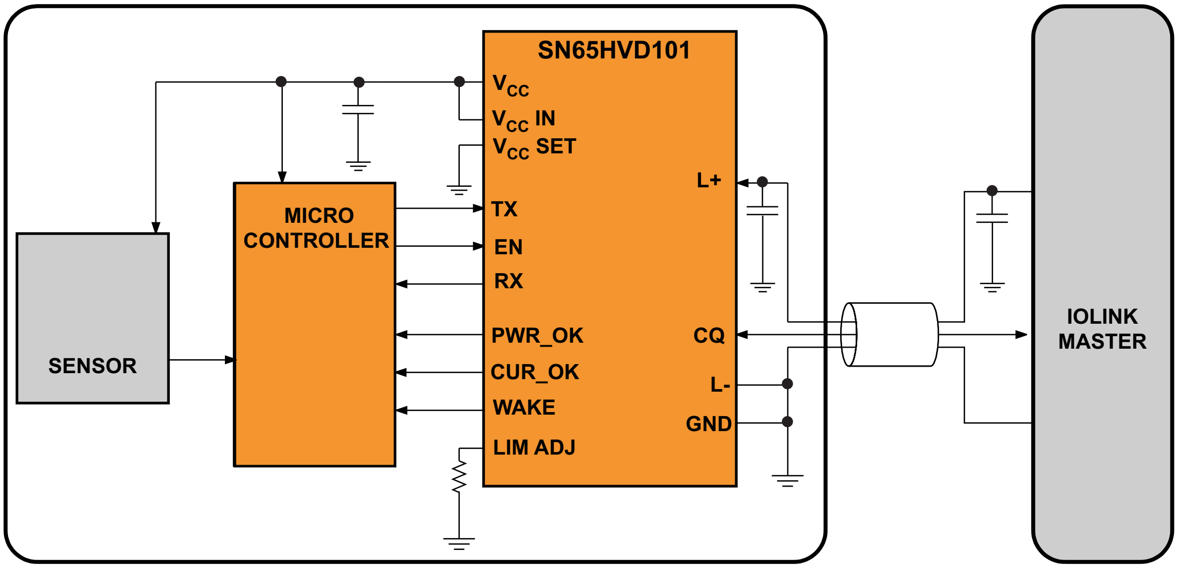


Figure 6. Application Example With V_{CC} = 3.3 V

N-Switch SIO Mode

Set TX pin High and use EN pin as the control to realize the function of N-switch (low-side driver) on the CQ pin.

EN	TX	CQ
L	H	Hi-Z
H	H	N-Switch

P-Switch SIO Mode

Set TX pin Low and use EN pin as the control to realize the function of P-switch (high-side driver) on the CQ pin.

EN	TX	CQ
L	L	Hi-Z
H	L	P-Switch

Push-Pull / Communication Mode

Set TX pin Low and use EN pin as the control to realize the function of P-switch (high-side driver) on the CQ pin.

EN	TX	CQ
L	X	Hi-Z
H	H	N-Switch
H	L	P-Switch

Wake up detection

The device may be in IO-Link mode or SIO mode. If the device is in SIO mode and the master node wants to initiate communication with the device node, the master drives the CQ line to the opposite of its present state, and will either sink or source the wake up current (IQ_{WU} is typically up to 500 mA) for the wake-up duration (T_{WU} is typically 80 µs) depending on the CQ logic level as per the IO-LINK specification. The SN65HVD1XX IO-LINK PHY detects this wake-up condition and communicates to the local microcontroller via the WAKE pin. The IO-Link Communication Specification requires the device node to switch to receive mode within 500 microseconds after receiving the Wake Up signal.

For over-current conditions shorter or longer than a valid Wake-Up pulse, the WAKE pin will remain in a high-impedance (inactive) state. This is illustrated in Figure 7, and discussed in the following paragraph.

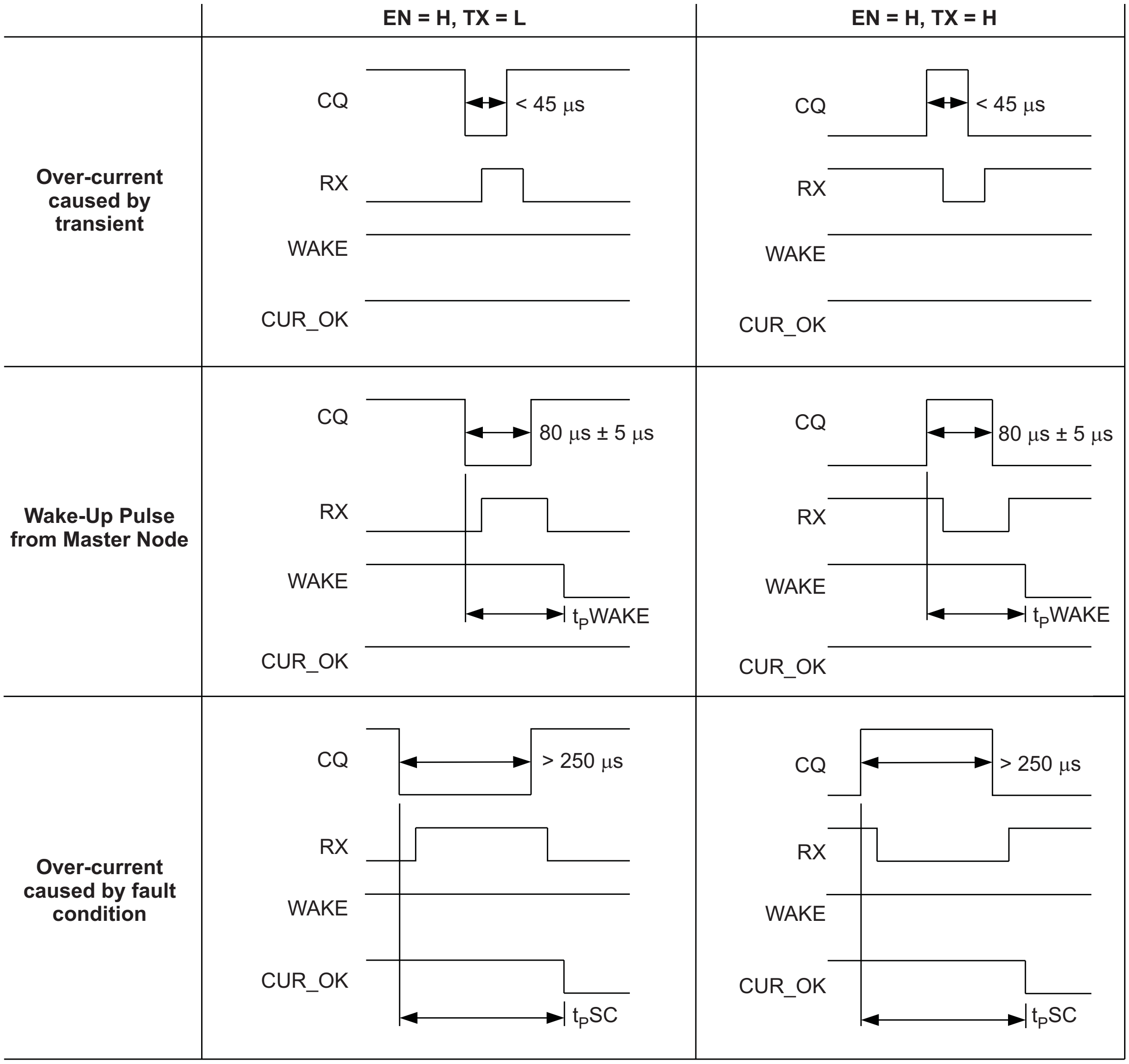


Figure 7. Over-Current and Wake Conditions

Current Limit Indication, Short Circuit Current Detection

If the output current at CQ remains at the internally set current limit IO(LIM) for a duration longer than a wake-up pulse (longer than 80 usec) the CUR_OK pin will be driven to a logic LOW state. The CUR_OK pin will return to the high-impedance (inactive) state when the CQ pin is no longer in a current limit condition.

The state diagram shown in Figure 8 illustrates the various states and under what conditions the device transitions from one state to another.

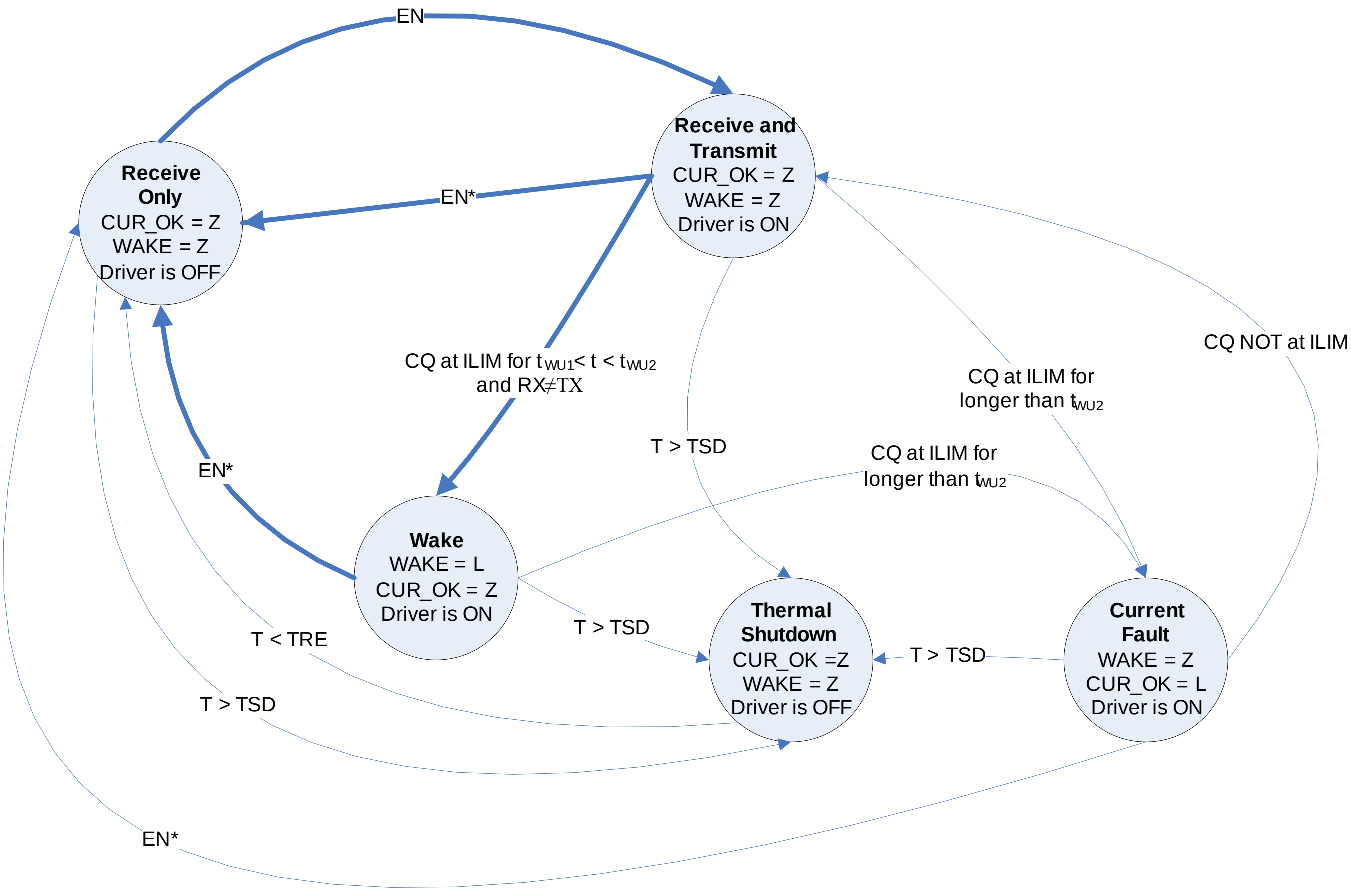


Figure 8. State Diagram

Over Temperature detection

If the internal temperature of the device exceeds the over-temperature threshold (θ_{TSD}), then the CQ driver and voltage regulator (HVD101) will be internally disabled. When the temperature falls below the temperature threshold the internal circuit re-enables the voltage regulator (HVD101) and the output driver, subject to the state of the EN and TX pins.

CQ Current Limit Adjustment

The CQ driver output current limit can be set using an external resistor on the LIMADJ pin. The current limit is given by:

$I_{(LIM)}$ = I_Ref × KSET where I_Ref = V_{REF} / (R_{INT} + R_{SET})

Note that both the positive and negative current limits are set by a single resistor value. If no R_{SET} is used (LIMADJ is tied directly to GND) then the current limit is set to the maximum value of 400 mA.

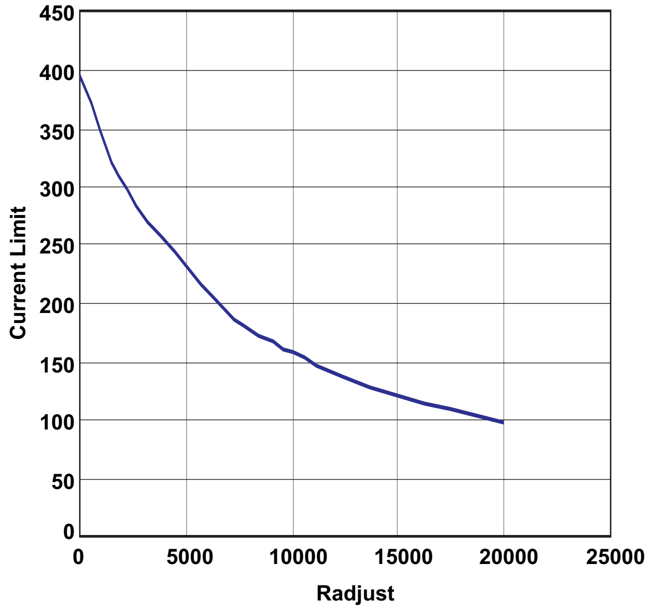


Figure 9. Typical Current Limit Characteristics

Over-Voltage and Reverse Polarity protection

Reverse polarity protection is included in the device. Any combination of voltages between 0 and 40V may be applied at the pins L+, CQ and L- without causing device damage. For protection against higher levels of faults, including transient over-voltage conditions, external protection devices can be added as shown in Figure 10. This will protect the device against high-power transients, and will also stand-off a steady-state reverse polarity fault of up to 33V.

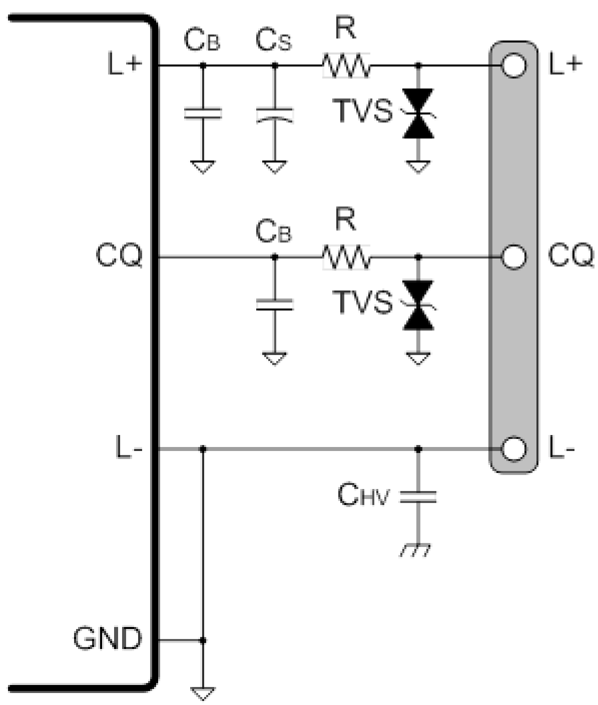


Figure 10.

Table 7. Suggested External Protection Components

Device	Function	Part-No.	Manufacturer
XCVR	I/O Link transceiver	SN65HVD101	Texas Instruments
R	1Ω, 0.25W MELF resistor	MMA02040B1008FB300	Vishay
TVS	Bidirectional 1500W TVS	SMCJ33CA	Bourns
CS	2.2uF, 100V, X7R, 10%	HMK325B7225KN-T	Taiyo Yuden
CB	0.1uF, 100V, X7R, 10%	C2012X7R2A104K	TDK
CHV	4700 pF, 2kV, X7R, 10%	1812B472K202NT	Nocacap

Voltage Regulator (Not available in the SN65HVD102)

The SN65HVD101 integrates a linear voltage regulator which supplies power to external components as well as to the PHY itself. The voltage regulator is specified for L+ voltages in the range of 9V to 30V with respect to GND. The output voltage can be set using the VccSET pin. When this pin is left open (floating) then the output voltage is 5V. When it is connected to GND then the output voltage is 3.3V. The integrated voltage regulator can supply a maximum current of 20 mA to external components. When more supply current is needed, an external transistor can be connected as shown in Figure 11 and Figure 12.

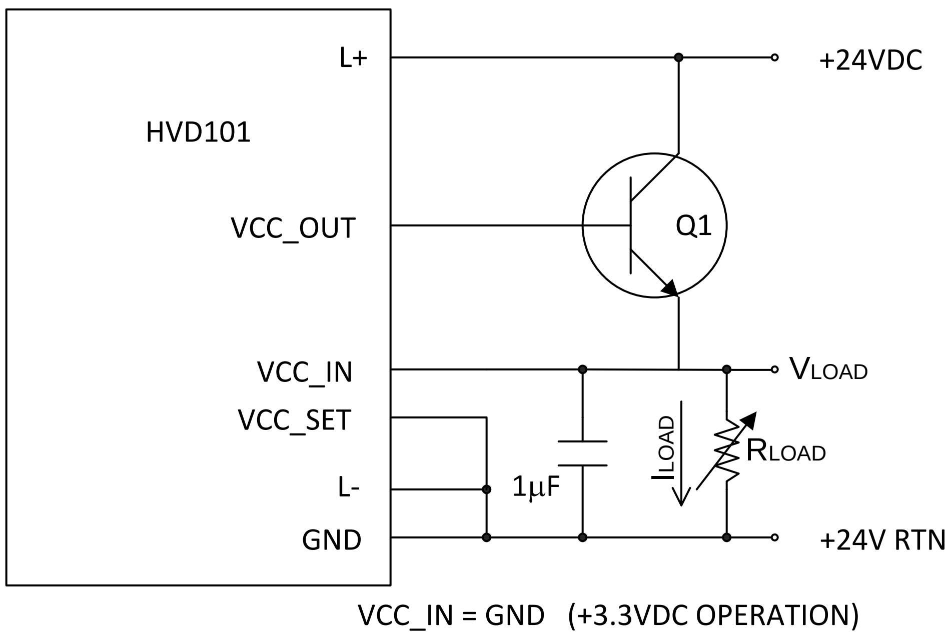


Figure 11. Example Circuit for Boosted 3.3V-Supply Current

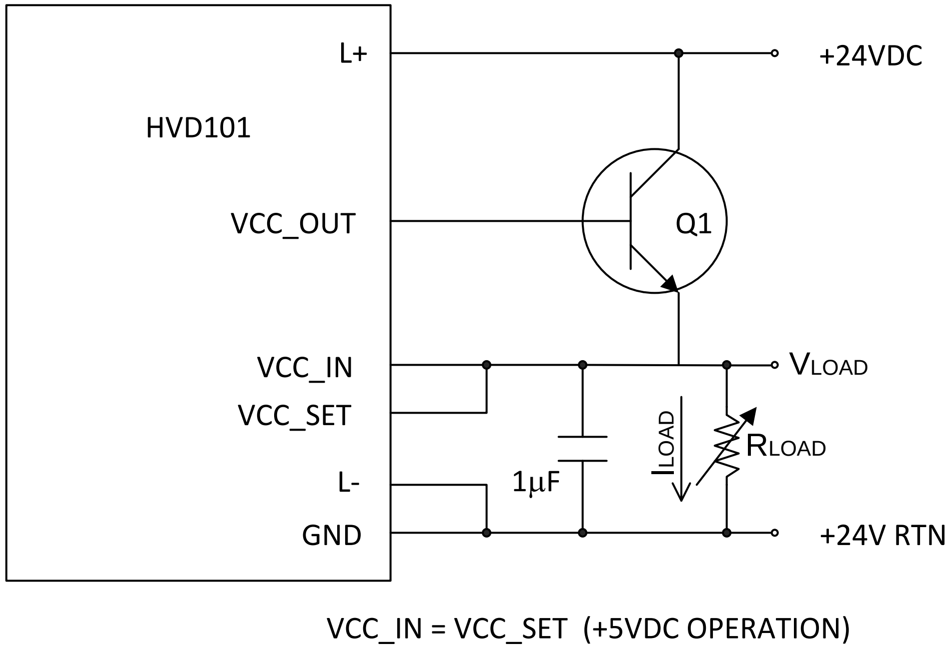


Figure 12. Example Circuit for Boosted 5V-Supply Current

Incandescent Lamp Loads

The resistance of an incandescent lamp filament varies strongly with temperature. The initial (cold-filament) resistance of tungsten-filament lamps is less than 10% of the steady-state (hot-filament) resistance. For example, a 100-watt, 120-volt lamp has a resistance of 144 Ω when lit, but the cold resistance is much lower (about 9.5 Ω). The initial “in-rush” current is therefore high compared to the steady-state current. Within 3 to 5 ms the current falls to approximately twice the hot current. For typical general-service lamps, the current reaches steady-state conditions in less than about 100 milliseconds. The ‘HVD10x CQ output will remain at the selected current-limit as the filament warms up, and then will stay at the steady-state current level. For example, a 6W, 24VDC indicator lamp has a steady-state current of 250 mA. However, the initial in-rush current could be over 2 Amps if unlimited. If the HVD10x current limit is set to 350 mA, this current will warm up the filament during the initial lamp turn-on, and the final current will be below the current limit. If the CQ output current is at the limit for longer than t_{SC}, the SC output will be active. The local controller can disable the CQ driver if the high current is not expected, or can re-check the SC output after 100 ms if the load is known to be incandescent.

SN65HVD101 Replaces ELMOS E981.10

The SN65HVD101 can replace the ELMOS E981.10 Basic IO-Link transceiver with a minimum of board re-configuration. See **the SN65HVD101 Evaluation Module** for board design guidelines to accommodate both devices.

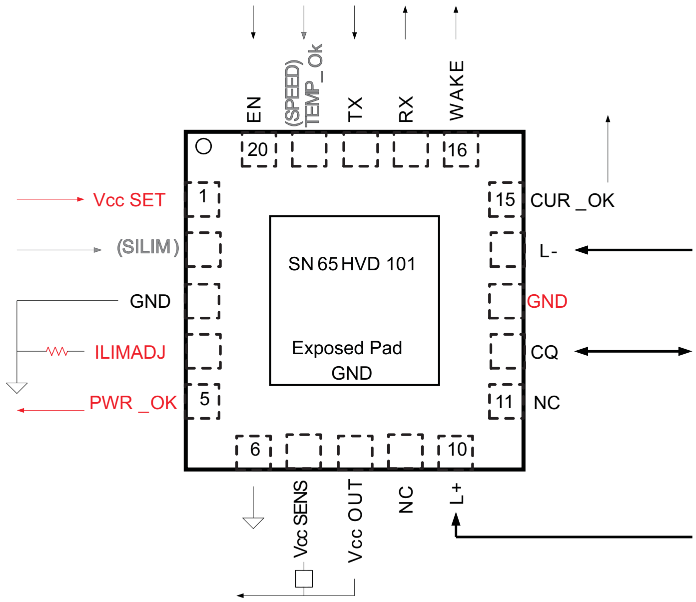


Figure 13. Comparison of HVD10x Pin-out to E981.10 Pin-out

REVISION HISTORY

Changes from Original (May 2011) to Revision A	Page
• Changed the devices From: Product Preview To: Production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVD101RGBR	ACTIVE	VQFN	RGB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD101	Samples
SN65HVD101RGBT	ACTIVE	VQFN	RGB	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD101	Samples
SN65HVD102RGBR	ACTIVE	VQFN	RGB	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD102	Samples
SN65HVD102RGBT	ACTIVE	VQFN	RGB	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD102	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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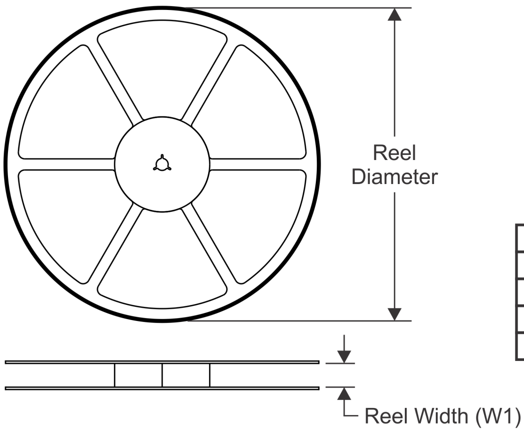
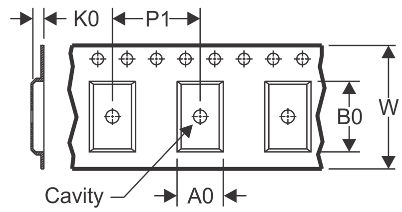
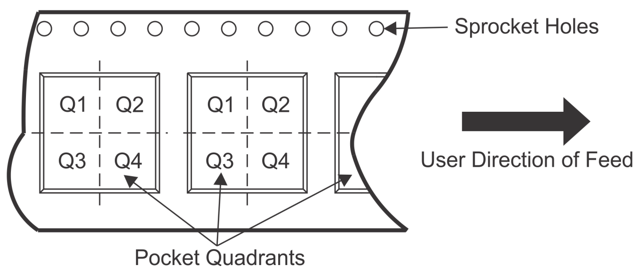
TAPE AND REEL INFORMATION





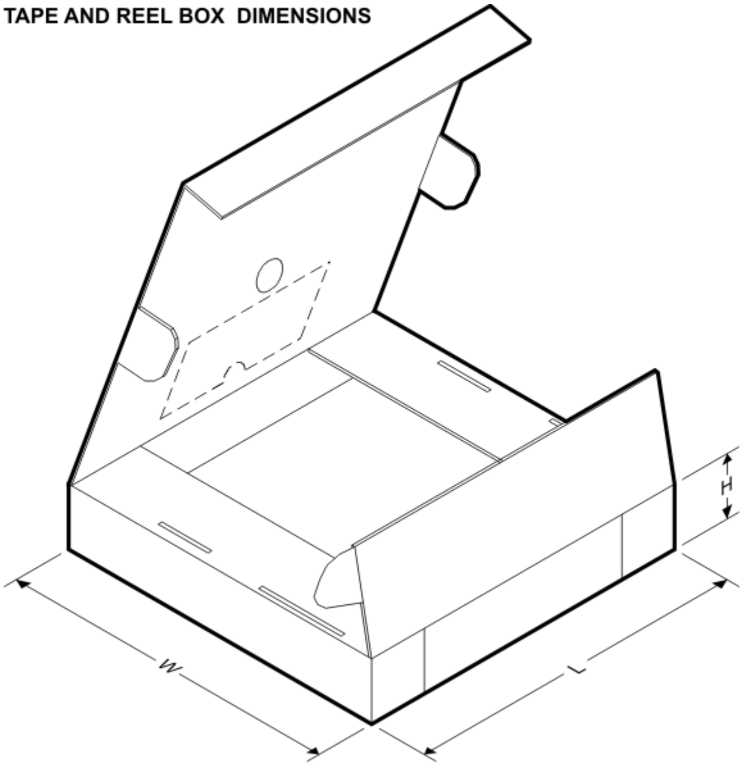
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD101RGBR	VQFN	RGB	20	1000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65HVD101RGBT	VQFN	RGB	20	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65HVD102RGBR	VQFN	RGB	20	1000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN65HVD102RGBT	VQFN	RGB	20	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

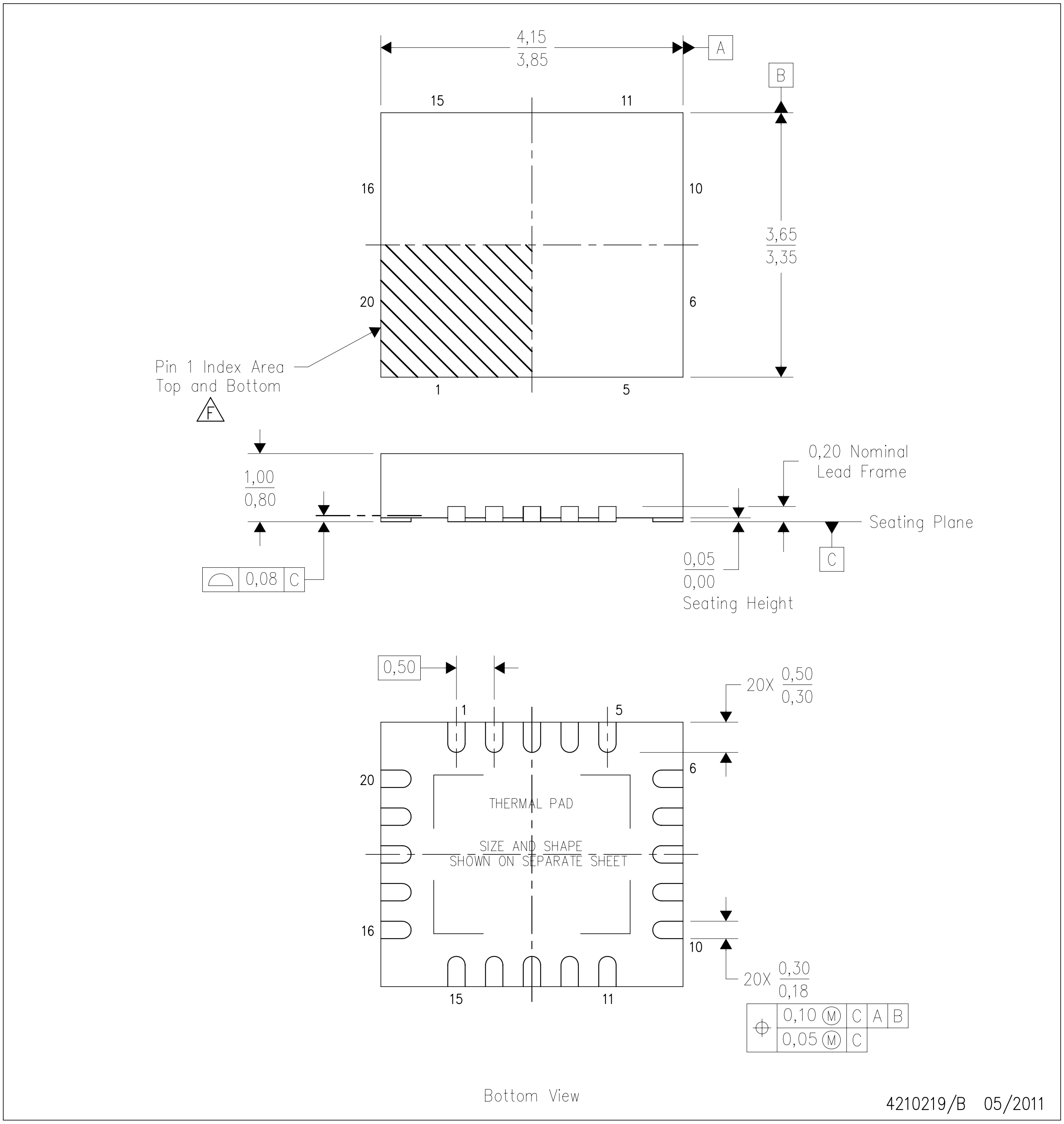
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD101RGBR	VQFN	RGB	20	1000	367.0	367.0	35.0
SN65HVD101RGBT	VQFN	RGB	20	250	210.0	185.0	35.0
SN65HVD102RGBR	VQFN	RGB	20	1000	367.0	367.0	35.0
SN65HVD102RGBT	VQFN	RGB	20	250	210.0	185.0	35.0

RGB (R-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

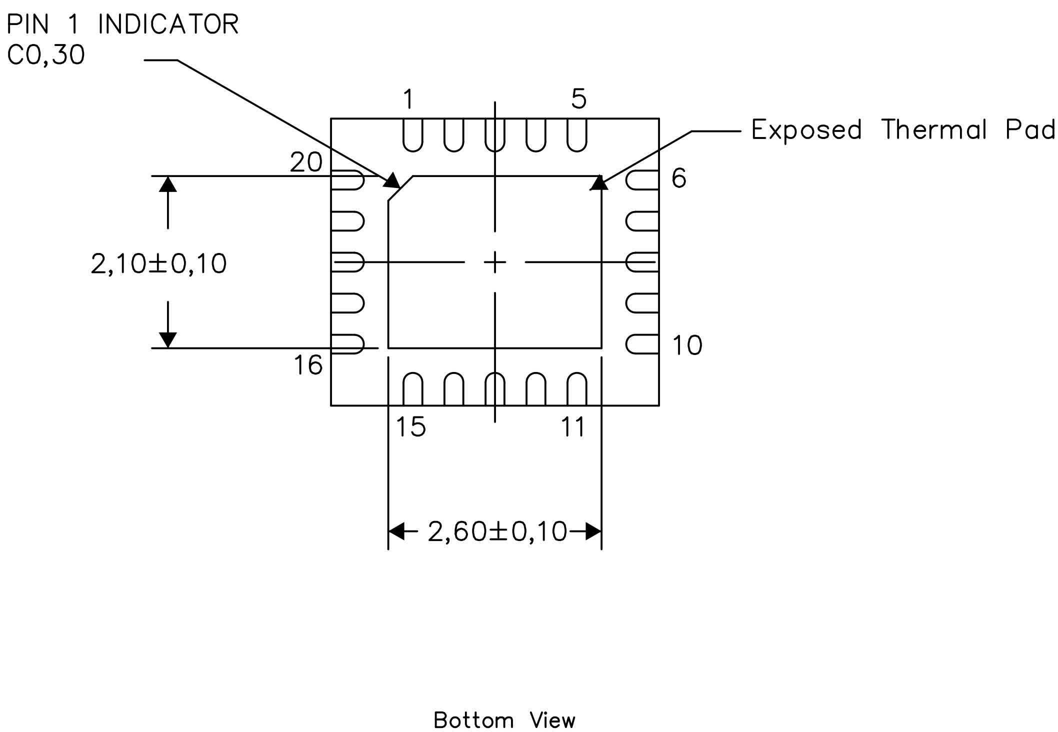
RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

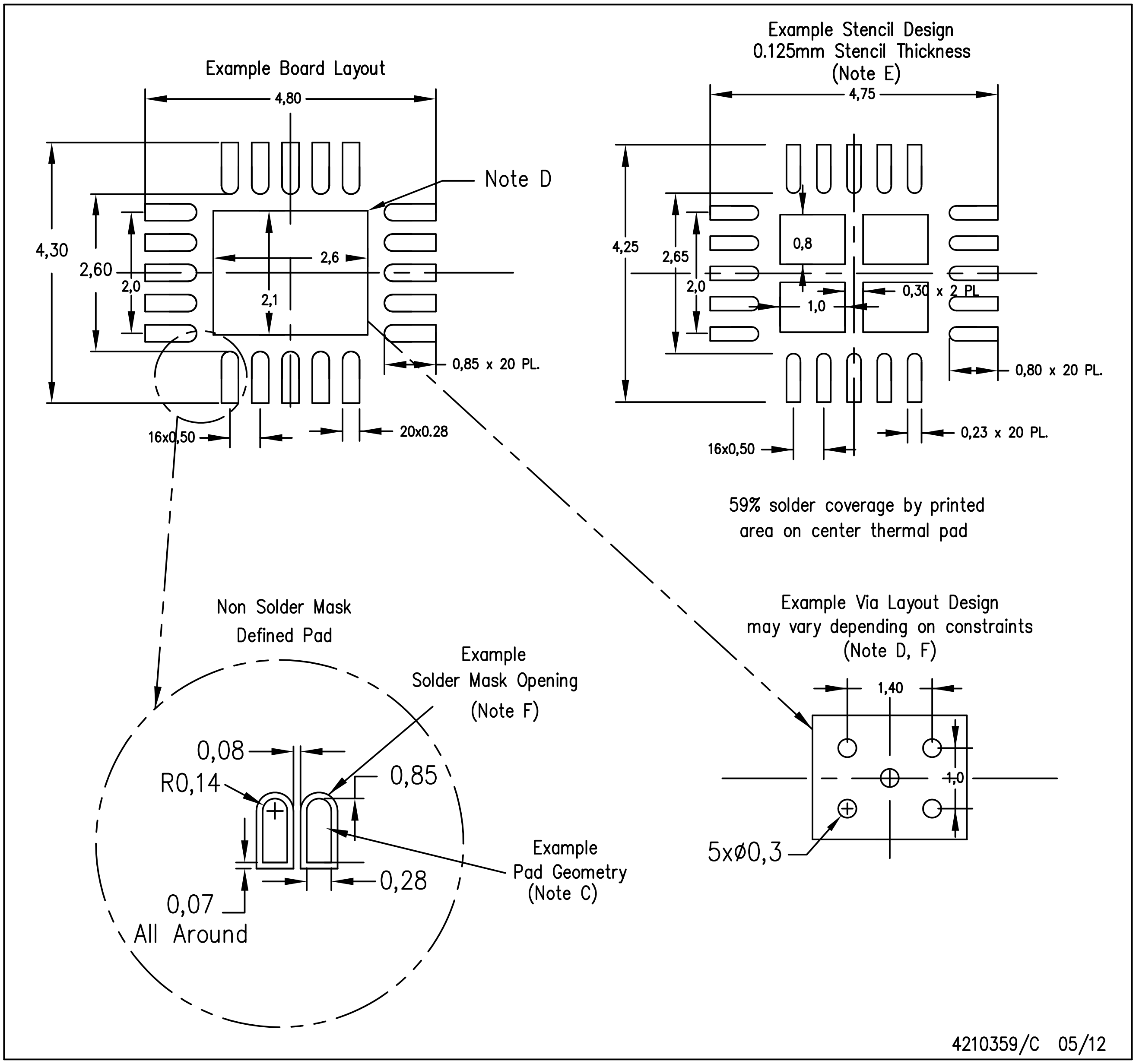


Exposed Thermal Pad Dimensions

4210242/C 05/12

NOTE: All linear dimensions are in millimeters

RGB (R-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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