3.3 V RS-485 TRANSCEIVERS

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of Up to –40°C to 125°C and –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Operates With a 3.3 V Supply**
- **Bus-Pin ESD Protection Exceeds 16 kV HBM**
- **1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)**
- **Optional Driver Output Transition Times for Signaling Rates of 1 Mbps, 10 Mbps, and 25 Mbps** (2)
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-485-A**
- **Bus-Pin Short Circuit Protection From –7 V to 12 V**
- **Low-Current Standby Mode . . . 1 µA (Typ)**
- **Open-Circuit, Idle-Bus, and Shorted-Bus Failsafe Receiver**
- **Thermal Shutdown Protection**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **SN75176 Footprint**

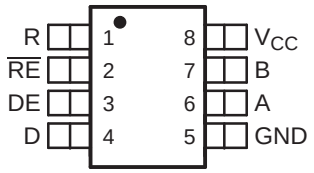
(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

(2) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

APPLICATIONS

- **Digital Motor Control**
- **Utility Meters**
- **Chassis-to-Chassis Interconnects**
- **Electronic Security Stations**
- **Industrial Process Control**
- **Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**

D PACKAGE
(TOP VIEW)



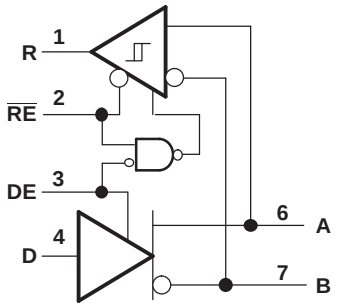
DESCRIPTION/ORDERING INFORMATION

The SN65HVD10, SN65HVD11, and SN65HVD12 combine a 3-state differential line driver and differential input line receiver that operate with a single 3.3 V power supply. They are designed for balanced transmission lines and meet or exceed ANSI standard TIA/EIA-485-A and ISO 8482:1993. These differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The drivers and receivers have active-high and active-low enables respectively, that can be externally connected together to function as direction control. Low device standby supply current can be achieved by disabling the driver and the receiver.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These parts feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM (POSITIVE LOGIC)



ORDERING INFORMATION(1)

SIGNALING RATE	UNIT LOADS	T_A	PACKAGE SOIC(2)(3)	SOIC MARKING
25 Mbps	1/2	–40°C to 125°C	SN65HVD10QDREP	V10QEP
10 Mbps	1/8		SN65HVD11QDREP(4)	V11QEP
1 Mbps	1/8	–40°C to 85°C	SN65HVD12IDREP	V12IEP
25 Mbps	1/2	–55°C to 125°C	SN65HVD10MDREP	V10MEP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The D package is taped and reeled as indicated by the R suffix to the part number (i.e., SN65HVD10QDREP).
(4) Product Preview

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			SN65HVD10-EP SN65HVD11-EP SN65HVD12-EP
Supply voltage range, V_{CC}			–0.3 V to 6 V
Voltage range at A or B			–9 V to 14 V
Input voltage range at D, DE, R, or $\overline{RE}$			–0.5 V to V_{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 11)			–50 V to 50 V
Electrostatic discharge	Human body model(3)	A, B, and GND	16 kV
		All pins	4 kV
	Charged-device model(4)	All pins Charge	1 kV
Continuous total power dissipation			See Package Dissipation Rating Table
Storage temperature range, T_{stg}			–65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s			260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D(2)	597 mW	4.97 mW/°C	373 mW	298 mW	100 mW
D(3)	990 mW	8.26 mW/°C	620 mW	496 mW	165 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7.

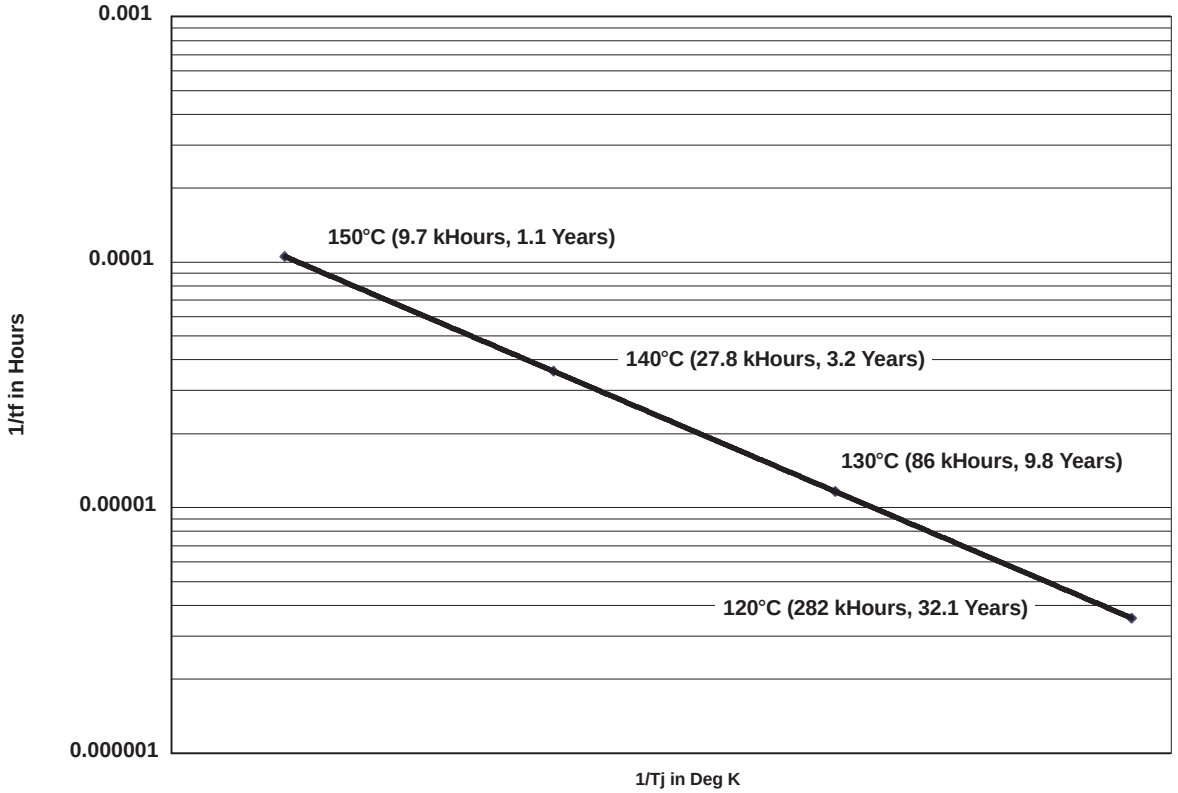


Figure 1. Estimated Device Life Based Kirkendall Voiding Failure Mode

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3		3.6	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		–7 (1)		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2		V_{CC}	V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$	0		0.8	V
Differential input voltage, V_{ID} (see Figure 8)		–12		12	V
High-level output current, I_{OH}	Driver	–60			mA
	Receiver	–8			
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Differential load resistance, R_L		54	60		Ω
Differential load capacitance, C_L			50		pF
Signaling rate	HVD10			25	Mbps
	HVD11			10	
	HVD12			1	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA		–1.5			V
$\|V_{OD}\|$	Differential output voltage(2)		I_O = 0		2		V_{CC}	V
			R_L = 54 Ω, See Figure 2		1.5			
			V_{test} = –7 V to 12 V, See Figure 3		1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage		See Figure 2 and Figure 3		–0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See Figure 4			400		mV
$V_{OC(SS)}$	Steady-state common-mode output voltage				1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.05		0.05	V
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			–100		0	µA
		DE			0		100	
I_{OS}	Short-circuit output current		–7 V ≤ V_O ≤ 12 V		–250		250	mA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15.5	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	µA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15.5	mA

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) For T_A > 85°C, V_{CC} is ±5%.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	HVD10	R_L = 54 Ω, C_L = 50 pF, See Figure 5	5	8.5	16	ns
		HVD11		18	25	40	
		HVD12		135	200	330	
t_{PHL}	Propagation delay time, high-to-low level output	HVD10		5	8.5	16	ns
		HVD11		18	25	40	
		HVD12		135	200	330	
t_r	Differential output signal rise time	HVD10		3	4.5	11.5	ns
		HVD11		10	20	30	
		HVD12		100	170	330	
t_f	Differential output signal fall time	HVD10		3	4.5	11.5	ns
		HVD11		10	20	30	
		HVD12		100	170	330	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD10				1.5	ns
		HVD11				2.5	
		HVD12				9	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD10				6	ns
		HVD11				11	
		HVD12				100	
t_{PZH}	Propagation delay time, high impedance-to-high level output	HVD10	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 6			33	ns
		HVD11				55	
		HVD12				320	
t_{PHZ}	Propagation delay time, high level-to-high-impedance output	HVD10				26	ns
		HVD11				55	
		HVD12				320	
t_{PZL}	Propagation delay time, high impedance-to-low-level output	HVD10	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 7			26	ns
		HVD11				55	
		HVD12				320	
t_{PLZ}	Propagation delay time, low level-to-high-impedance output	HVD10				26	ns
		HVD11				75	
		HVD12				420	
t_{PZH}	Propagation delay time, standby-to-high-level output	I and Q-temp	R_L = 110 Ω, $\overline{RE}$ at 3 V, See Figure 6			6	µs
		M-temp				14	
t_{PZL}	Propagation delay time, standby-to-low-level output	I and Q-temp	R_L = 110 Ω, $\overline{RE}$ at 3 V, See Figure 7			6	µs
		M-temp				14	

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA					–0.01	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA			–0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)					35		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA			–1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –8 mA,	See Figure 8	2.4			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA,	See Figure 8			0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 or V_{CC}	$\overline{RE}$ at V_{CC}		–1		1	µA
I_I	Bus input current	V_A or V_B = 12 V		HVD11, HVD12, Other input at 0 V		0.05	0.11	mA
		V_A or V_B = 12 V,	V_{CC} = 0 V			0.06	0.13	
		V_A or V_B = –7 V			–0.1	–0.05		
		V_A or V_B = –7 V,	V_{CC} = 0 V		–0.05	÷0.04		
		V_A or V_B = 12 V		HVD10, Other input at 0 V		0.2	0.5	mA
		V_A or V_B = 12 V,	V_{CC} = 0 V			0.25	0.5	
		V_A or V_B = –7 V			–0.4	–0.2		
		V_A or V_B = –7 V,	V_{CC} = 0 V		–0.4	–0.15		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V			–30		0	µA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V			–30		0	µA
C_{ID}	Differential input capacitance	V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V				15		pF
I_{CC}	Supply current	$\overline{RE}$ at 0 V, D and DE at 0 V, No load	Receiver enabled and driver disabled			4	8	mA
		$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load	Receiver disabled and driver disabled (standby)			1	5	µA
		$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled			9	15.5	mA

(1) All typical values are at 25°C and with a 3.3 V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	HVD10	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 9	12.5	20	25	ns
t_{PHL}	Propagation delay time, high-to-low level output	HVD10		12.5	20	25	ns
t_{PLH}	Propagation delay time, low-to-high level output	HVD11 HVD12		30	55	70	ns
t_{PHL}	Propagation delay time, high-to-low level output	HVD11 HVD12		30	55	70	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	HVD10				1.5	ns
		HVD11				4	
		HVD12				4	
$t_{sk(pp)}$(2)	Part-to-part skew	HVD10				8	ns
		HVD11				15	
		HVD12				15	
t_r	Output signal rise time		C_L = 15 pF, See Figure 9	1	2	6	ns
t_f	Output signal fall time			1	2	6	
t_{PZH}(1)	Output enable time to high level		C_L = 15 pF, DE at 3 V, See Figure 10			16	ns
t_{PZL}(1)	Output enable time to low level					16	
t_{PHZ}	Output disable time from high level					21	
t_{PLZ}	Output disable time from low level					16	
t_{PZH}(2)	Propagation delay time, standby-to-high-level output	I and Q-temp	C_L = 15 pF, DE at 0, See Figure 11			6	µs
		M-temp				14	
t_{PZL}(2)	Propagation delay time, standby-to-low-level output	I and Q-temp				6	
		M-temp				14	

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

THERMAL CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	High-K board(3), No airflow	D package		121		°C/W
θ_{JB}	Junction-to-board thermal resistance	High-K board	D package		67		°C/W
θ_{JC}	Junction-to-case thermal resistance		D package		41		°C/W
P_D	Device power dissipation	R_L = 60 Ω, C_L = 50 pF, DE at V_{CC} $\overline{RE}$ at 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate	HVD10 (25 Mbps)		198	233	mW
			HVD11 (10 Mbps)		141	176	mW
			HVD12 (500 kbps)		133	161	mW
T_{JSD}	Thermal shutdown junction temperature				165		°C

(1) See *Application Information* section for an explanation of these parameters.
(2) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
(3) JSD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

PARAMETER MEASUREMENT INFORMATION

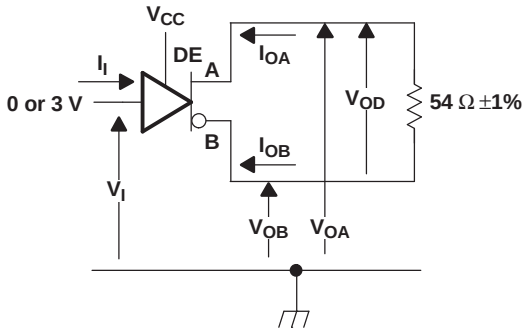


Figure 2. Driver V_{OD} Test Circuit and Voltage and Current Definitions

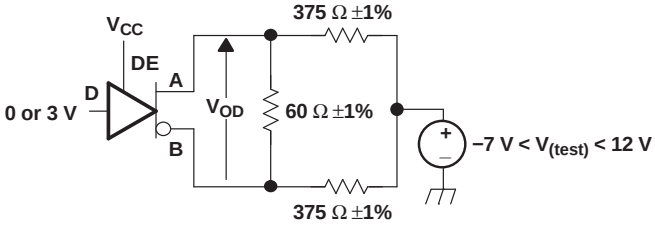
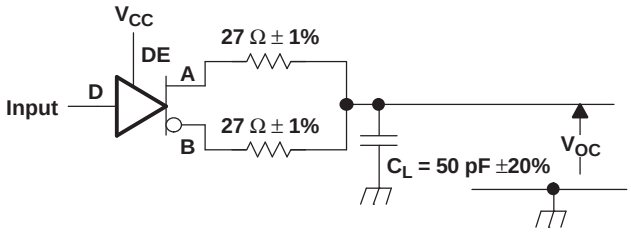


Figure 3. Driver V_{OD} With Common-Mode Loading Test Circuit



C_L Includes Fixture and Instrumentation Capacitance

Input: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

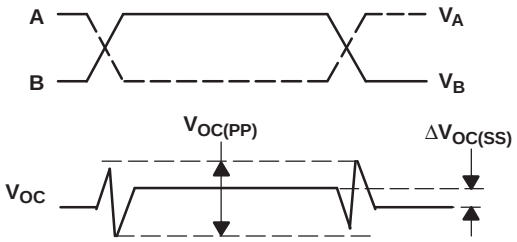
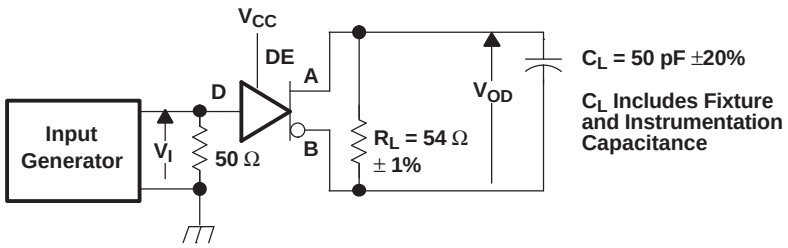
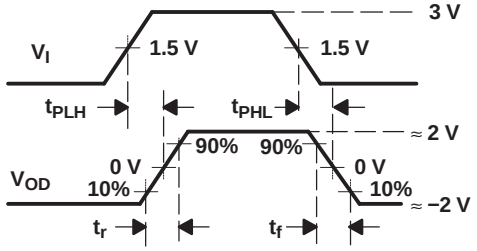


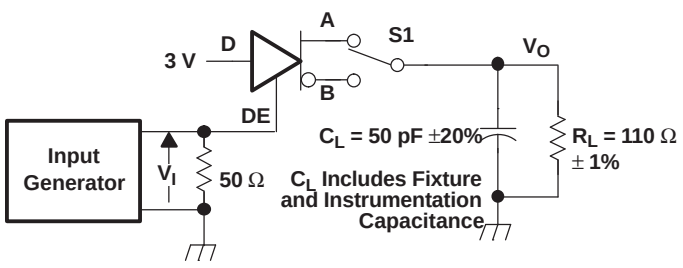
Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

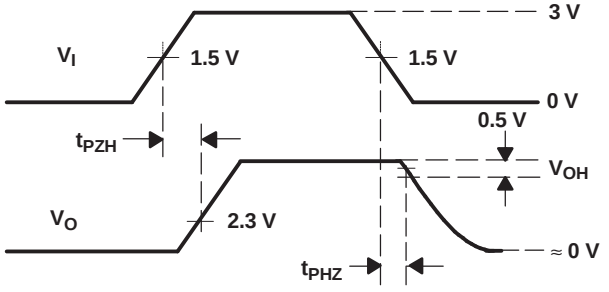




Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω

Figure 5. Driver Switching Test Circuit and Voltage Waveforms

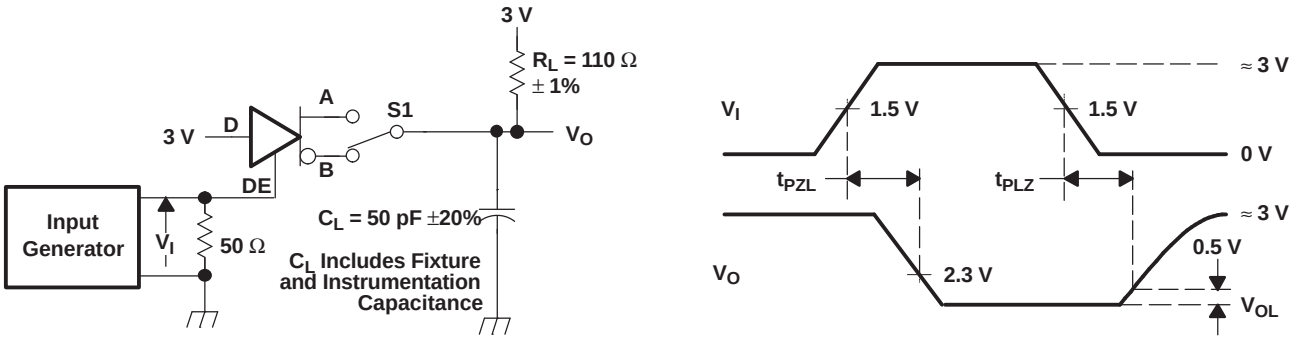




Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω

Figure 6. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω

Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

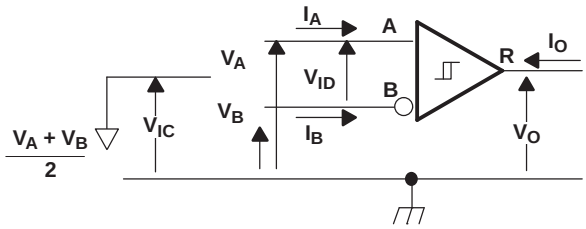
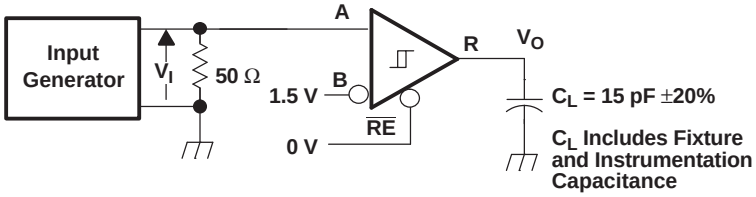


Figure 8. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω

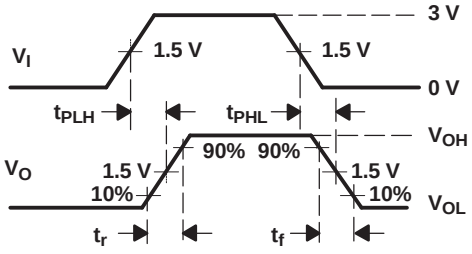
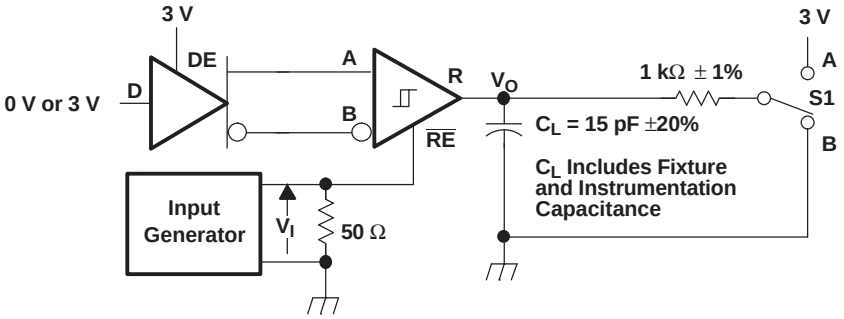


Figure 9. Receiver Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω

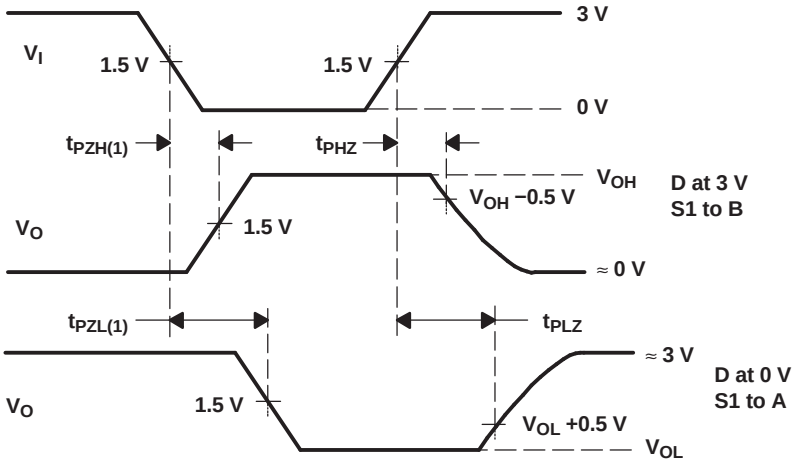
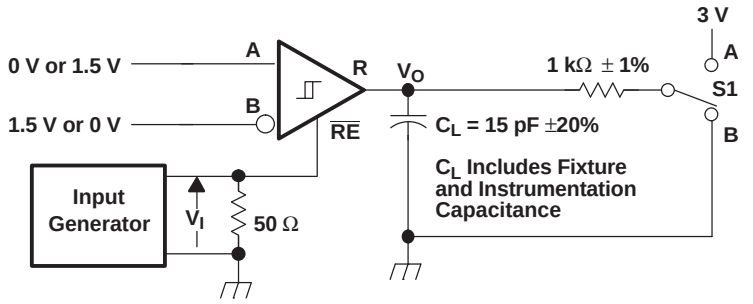


Figure 10. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 100 kHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω

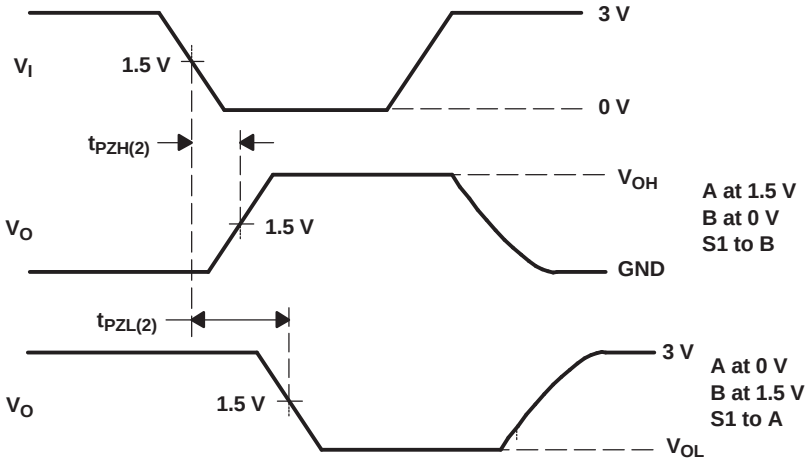
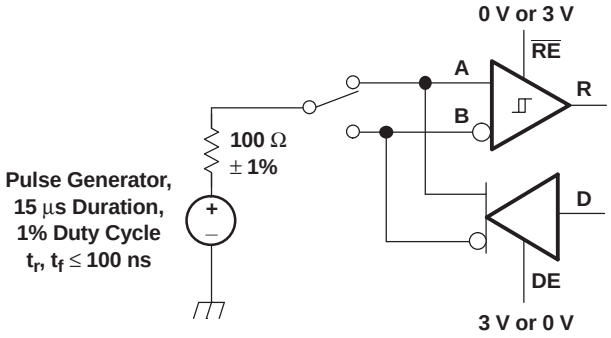


Figure 11. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 12. Test Circuit, Transient Over Voltage Test

Function Tables

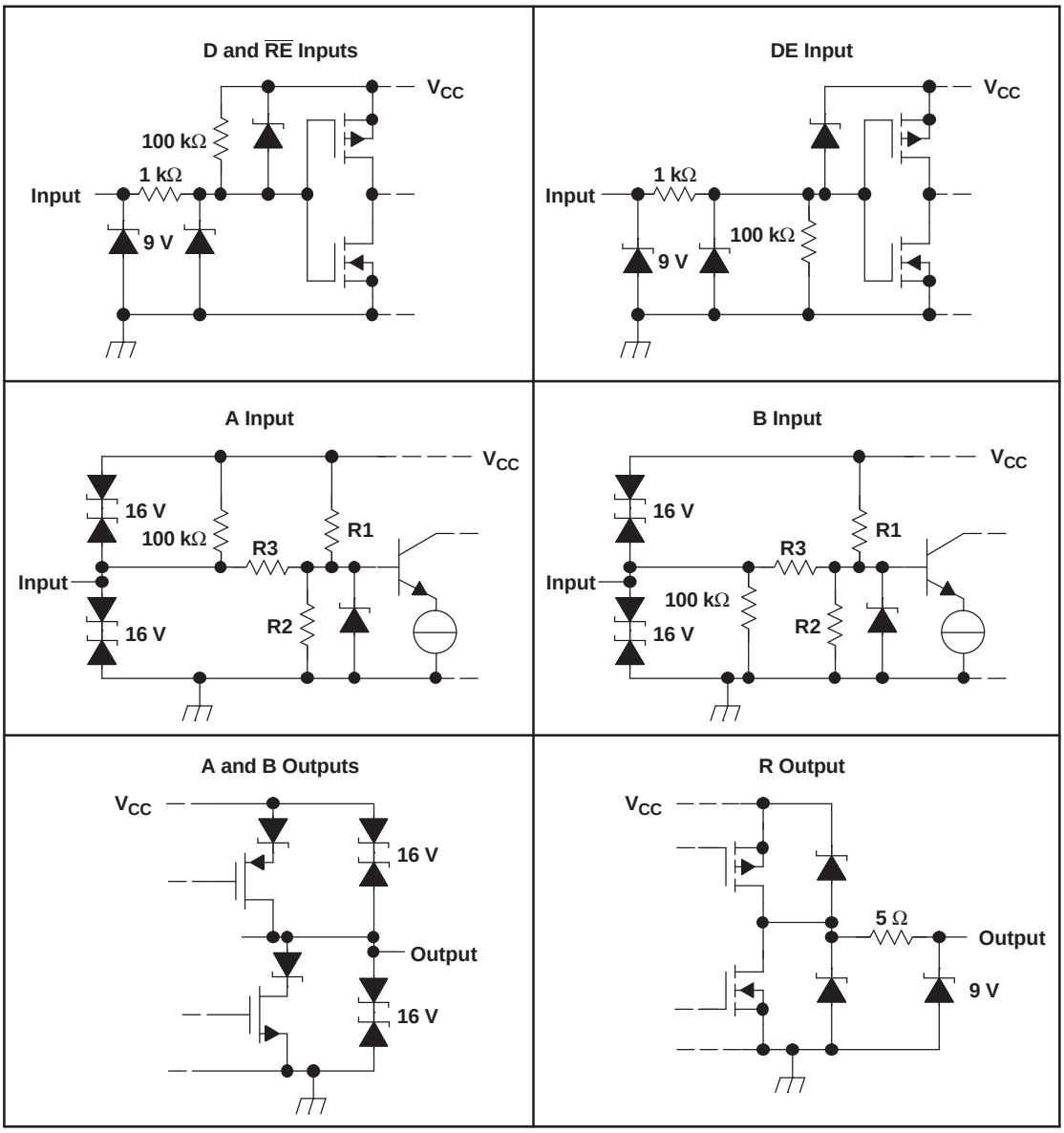
DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \leq -0.2$ V	L	L
-0.2 V $< V_{ID} < -0.01$ V	L	?
-0.01 V $\leq V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD10	9 kΩ	45 kΩ
SN65HVD11	36 kΩ	180 kΩ
SN65HVD12	36 kΩ	180 kΩ

TYPICAL CHARACTERISTICS

HVD10 OR HVD12
RMS SUPPLY CURRENT
vs
SIGNALING RATE

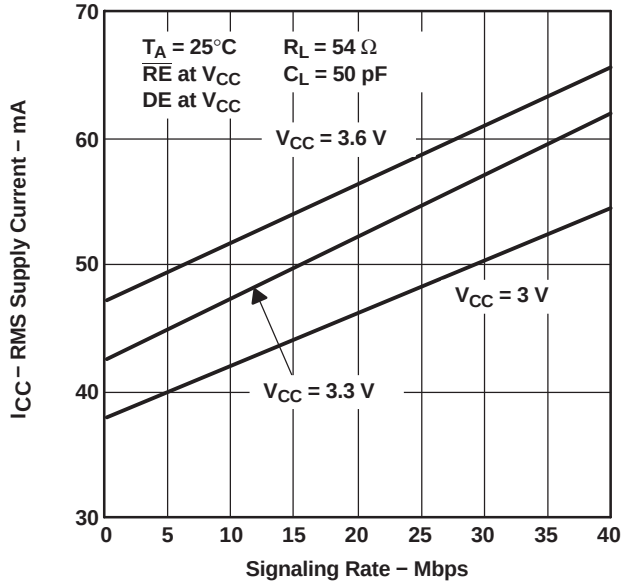


Figure 13.

HVD11
RMS SUPPLY CURRENT
vs
SIGNALING RATE

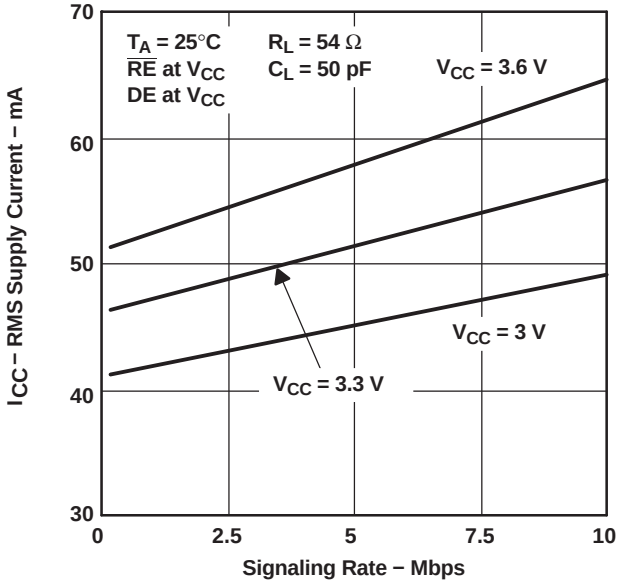


Figure 14.

HVD12
RMS SUPPLY CURRENT
vs
SIGNALING RATE

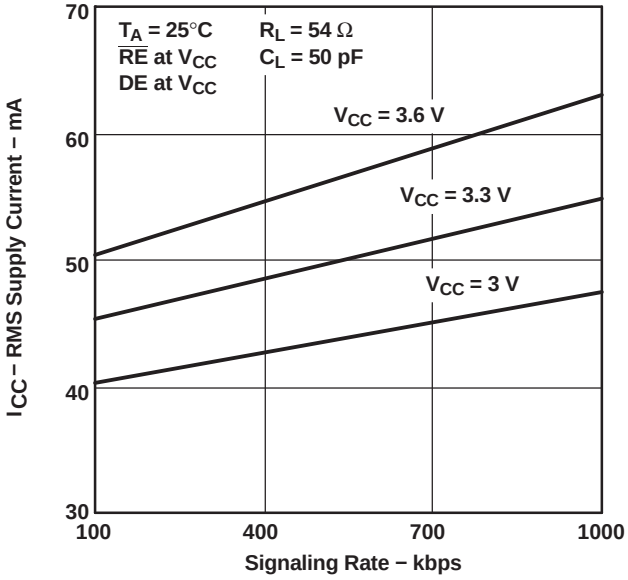


Figure 15.

HVD10
BUS INPUT CURRENT
vs
BUS INPUT VOLTAGE

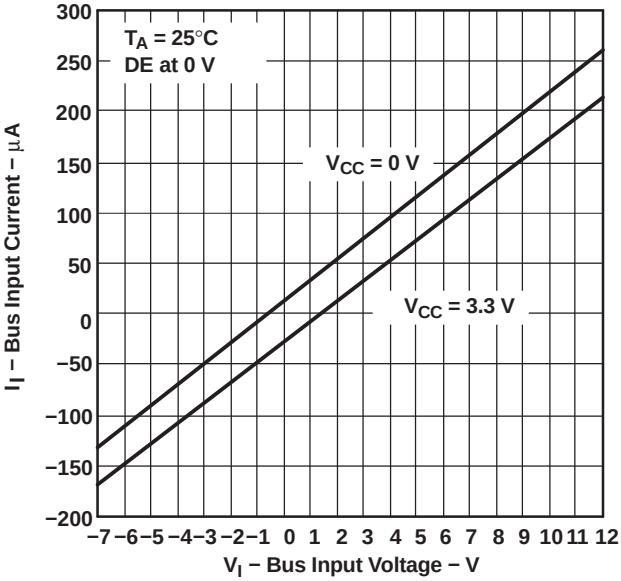


Figure 16.

TYPICAL CHARACTERISTICS (continued)

HVD11 OR HVD12
BUS INPUT CURRENT
vs
BUS INPUT VOLTAGE

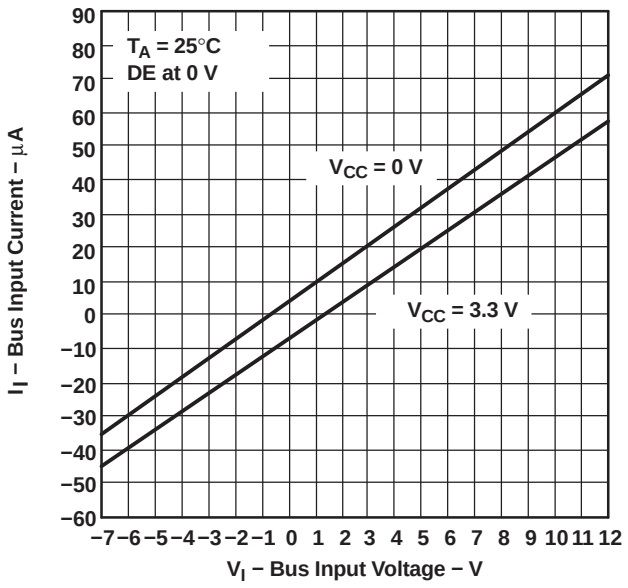


Figure 17.

HIGH-LEVEL OUTPUT CURRENT
vs
DRIVER HIGH-LEVEL OUTPUT VOLTAGE

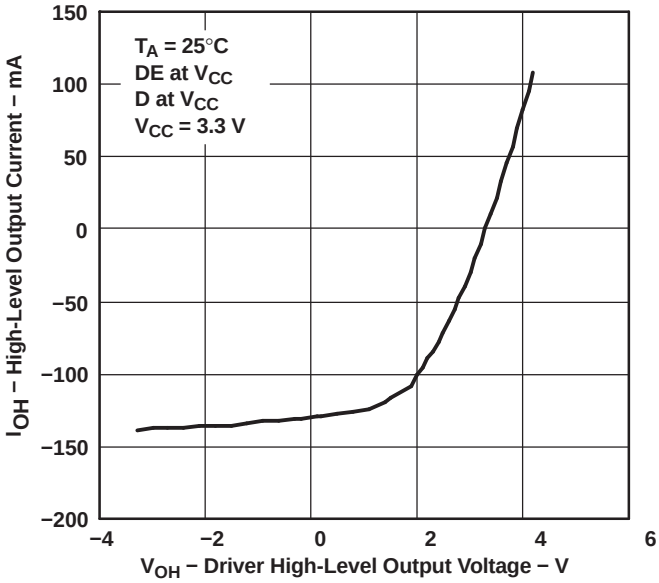


Figure 18.

LOW-LEVEL OUTPUT CURRENT
vs
DRIVER LOW-LEVEL OUTPUT VOLTAGE

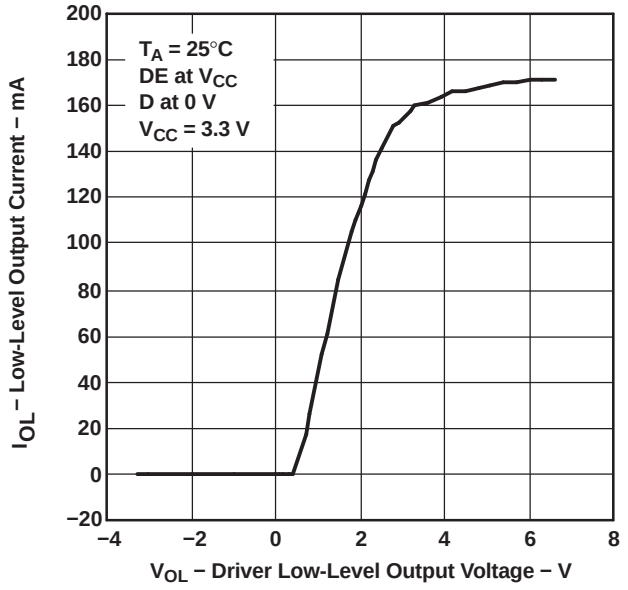


Figure 19.

DRIVER DIFFERENTIAL OUTPUT
vs
FREE-AIR TEMPERATURE

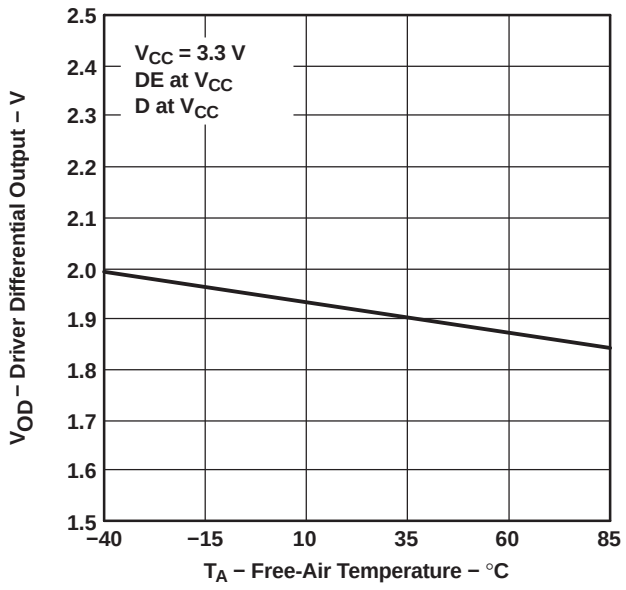


Figure 20.

TYPICAL CHARACTERISTICS (continued)

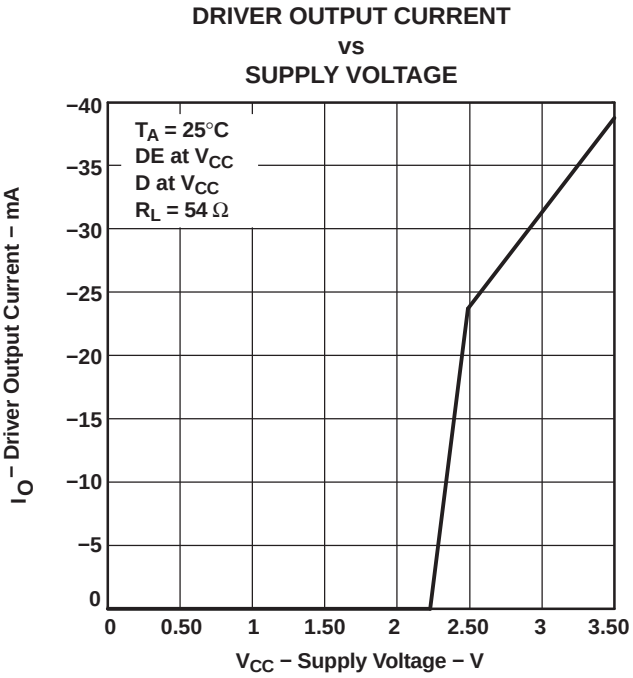
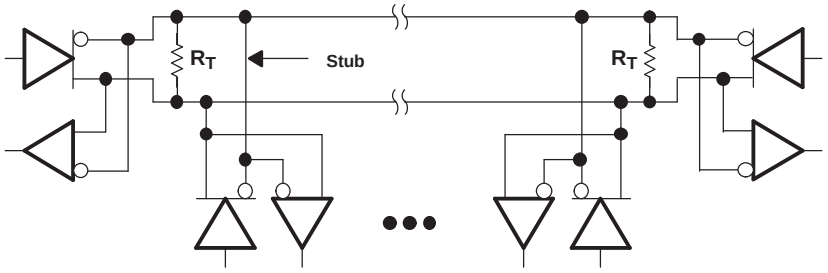


Figure 21.

APPLICATION INFORMATION

An example application for the HVD12 is illustrated in Figure 22. Two HVD12 transceivers are used to communicate data through a 2000 foot (600 m) length of Commscope 5524 category 5e+ twisted pair cable. The bus is terminated at each end by a 100 Ω resistor, matching the cable characteristic impedance. Figure 23 illustrates operation at a signaling rate of 250 kbps.



Device	Number of Devices on Bus
HVD10	64
HVD11	256
HVD12	256

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 22. Typical Application Circuit

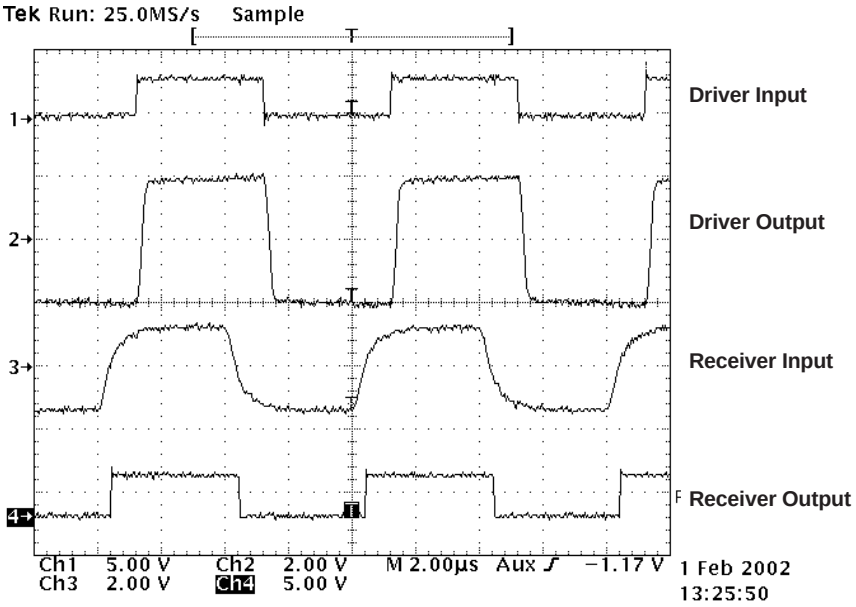


Figure 23. HVD12 Input and Output Through 2000 Feet of Cable

THERMAL CHARACTERISTICS OF IC PACKAGES

Junction-to-Ambient Thermal Resistance (θ_{JA}) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is *not* a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

Texas Instruments uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single copper trace layer 25 mm long and 2 oz thick. The high-k board gives *best case* in-use condition and it consists of two 1 oz buried power planes with a single copper trace layer 25 mm long and 2 oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

Junction-to-Case Thermal Resistance (θ_{JC}) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in one-dimensional thermal simulation of a package system.

Junction-to-Board Thermal Resistance (θ_{JB}) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is defined only for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGAs with thermal balls) and can be used for simple one-dimensional network analysis of the package system (see Figure 24).

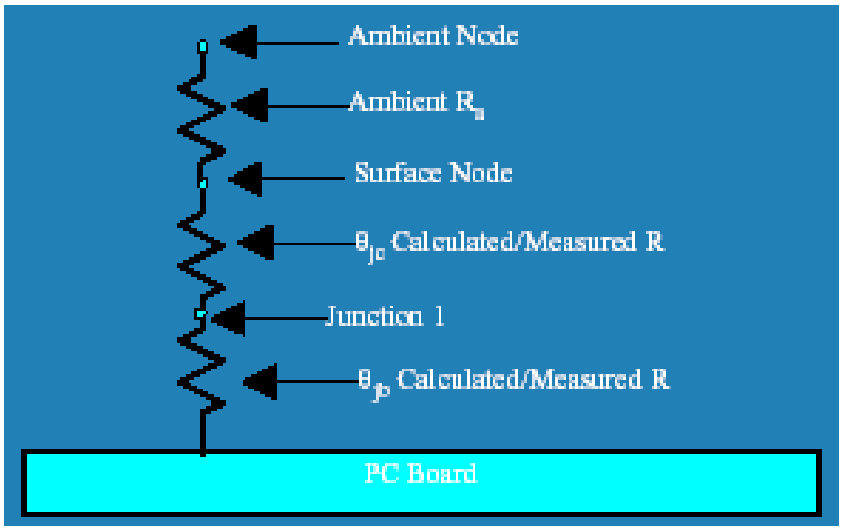


Figure 24. Thermal Resistance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD10MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
SN65HVD10QDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
SN65HVD12IDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
V62/05604-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
V62/05604-03XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
V62/05604-04XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVD10-EP, SN65HVD12-EP :

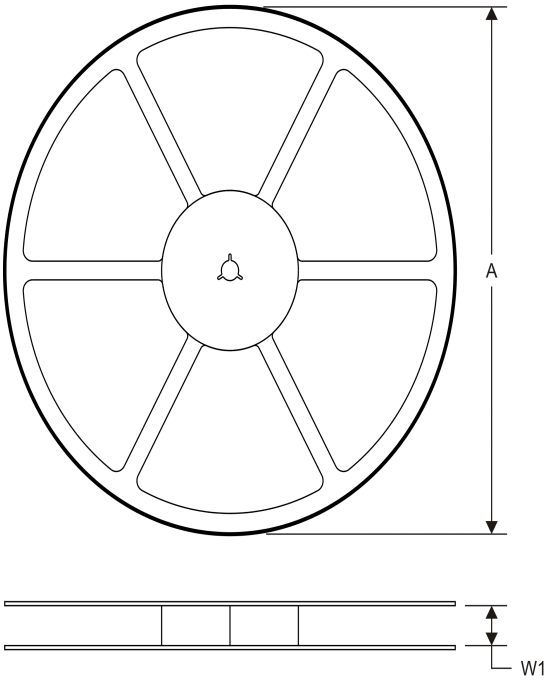
- Catalog: SN65HVD10, SN65HVD12

NOTE: Qualified Version Definitions:

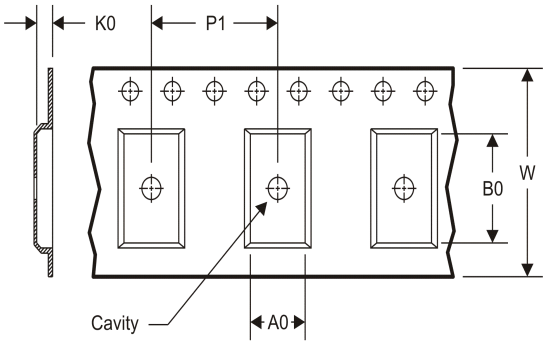
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



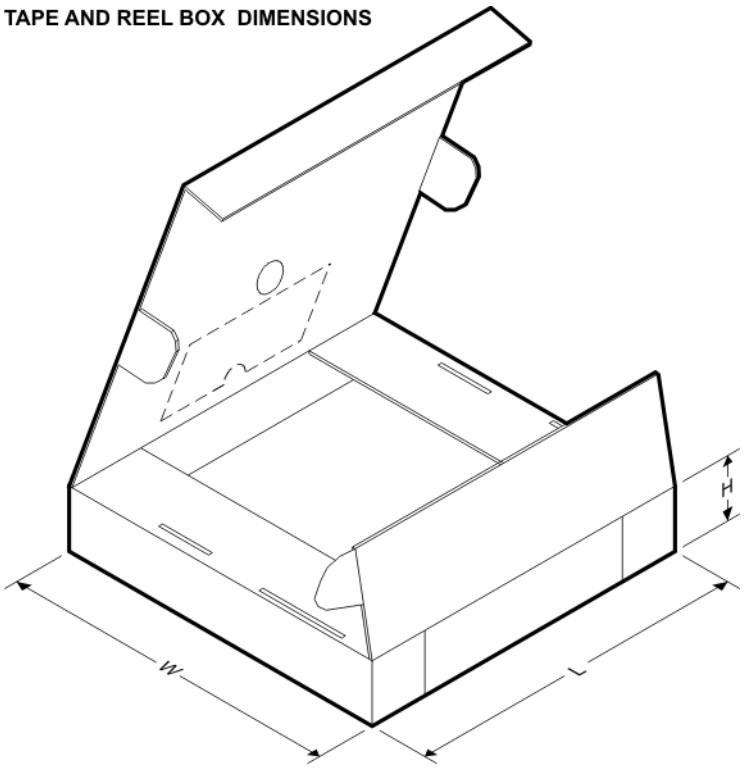
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD10MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD10QDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD12IDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

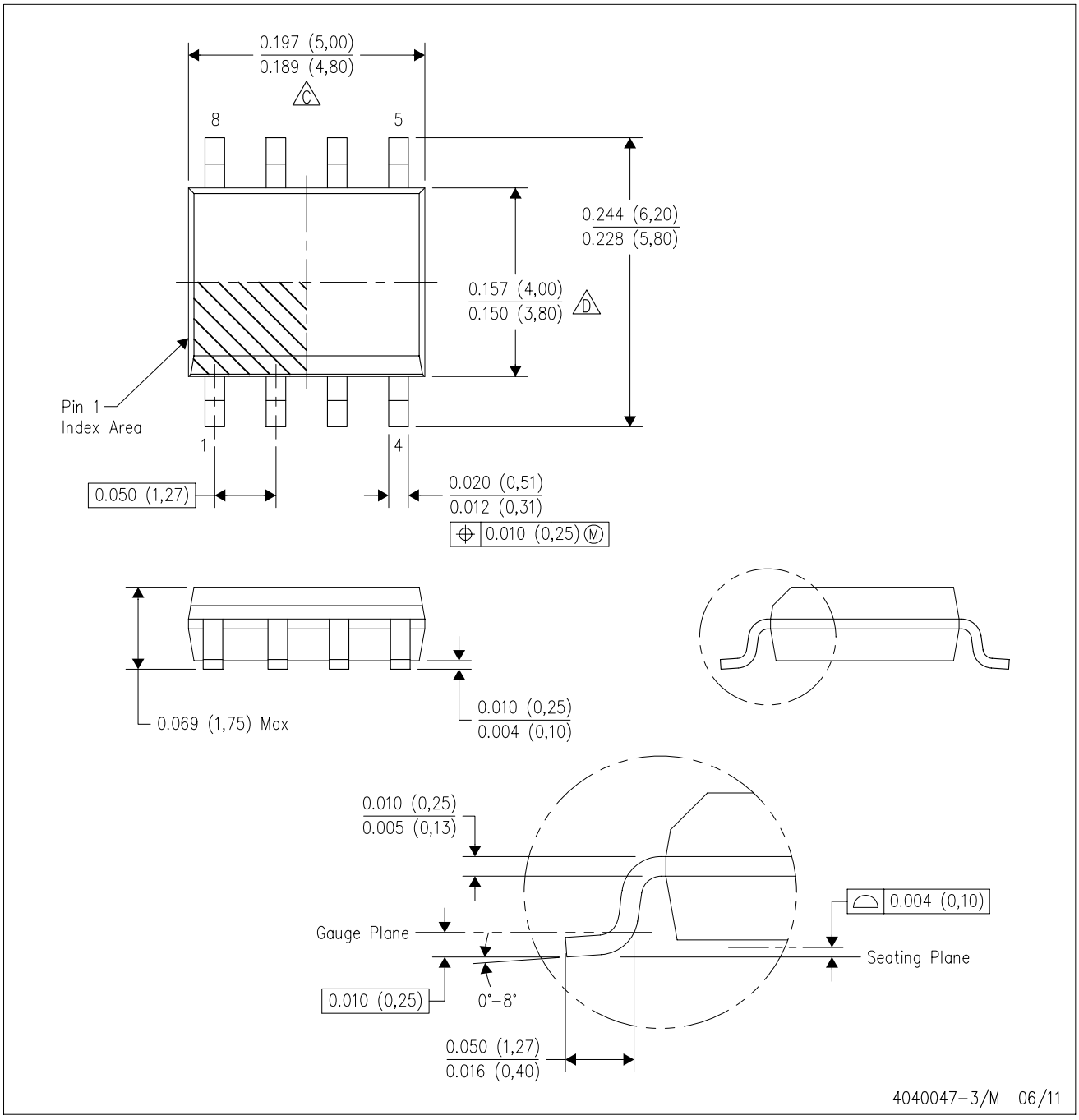
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

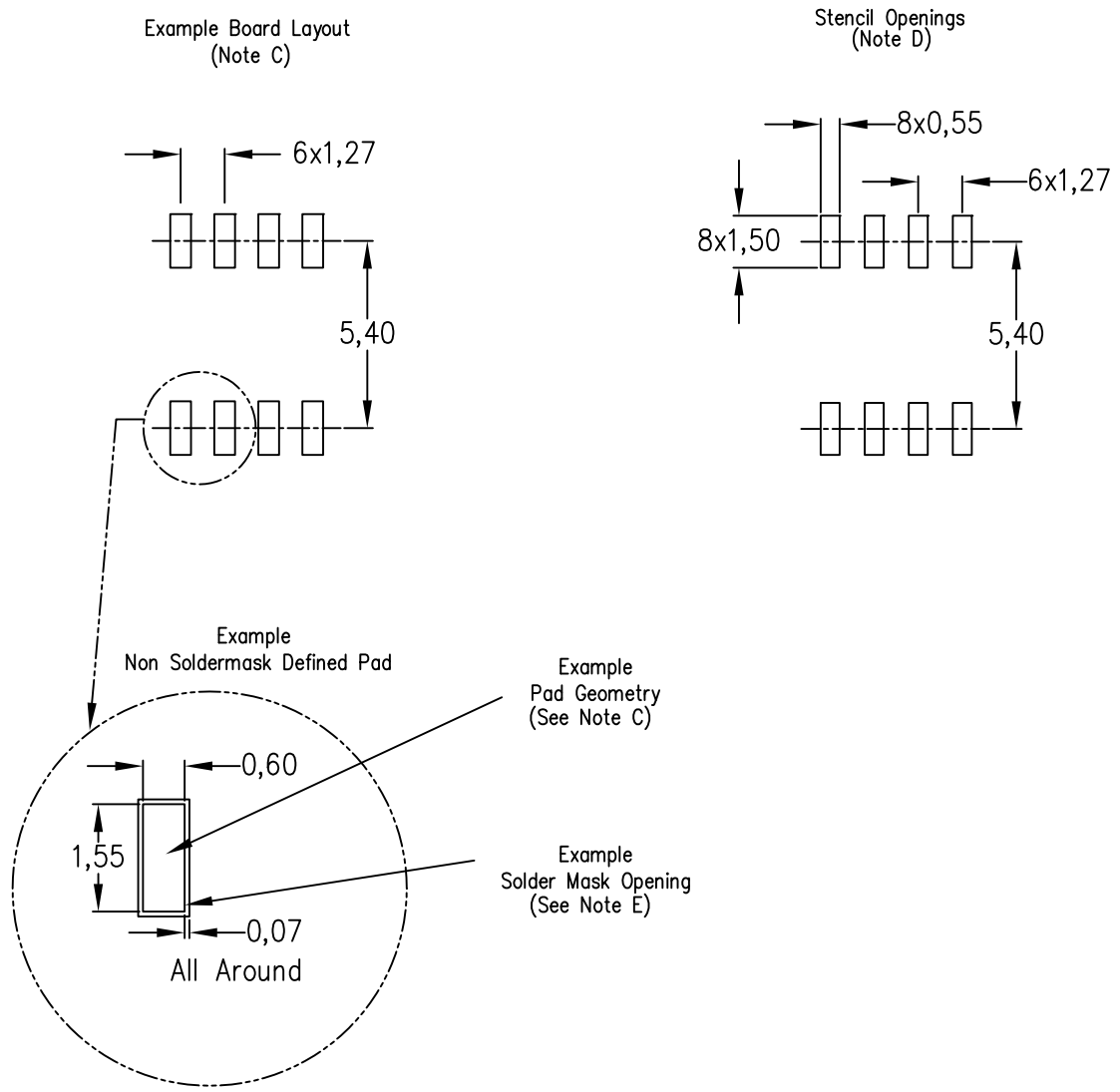
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD10MDREP	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD10QDREP	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD12IDREP	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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