EMC-OPTIMIZED HIGH SPEED CAN TRANSCEIVER

Check for Samples: SN65HVDA1040A-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Meets or Exceeds the Requirements of ISO 11898-2 and -5**
- **GIFT/ICT Compliant**
- **ESD Protection up to ±12 kV (Human-Body Model) on Bus Pins**
- **Low-Current Standby Mode With Bus Wake-Up, <12 μA Max**
- **High Electromagnetic Compliance (EMC)**
- **SPLIT Voltage Source for Common-Mode Stabilization of Bus Via Split Termination**
- **Digital Inputs Compatible with 3.3V and 5V Microprocessors**
- **Package Options: SOIC and VSON**
- **Protection Features**
  - **Bus-Fault Protection of –27 V to 40 V**
  - **TXD Dominant Time-Out**
  - **Thermal Shutdown Protection**
  - **Power-Up/Down Glitch-Free Bus Inputs and Outputs**
  - **High Bus Input Impedance With Low V_{CC} (Ideal Passive Behavior on Bus When Unpowered)**

APPLICATIONS

- **GMW3122 Dual-Wire CAN Physical Layer**
- **SAE J2284 High-Speed CAN for Automotive Applications**
- **SAE J1939 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**

DESCRIPTION

The SN65HVDA1040A meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). The device is qualified for use in automotive applications. As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps)(1) .

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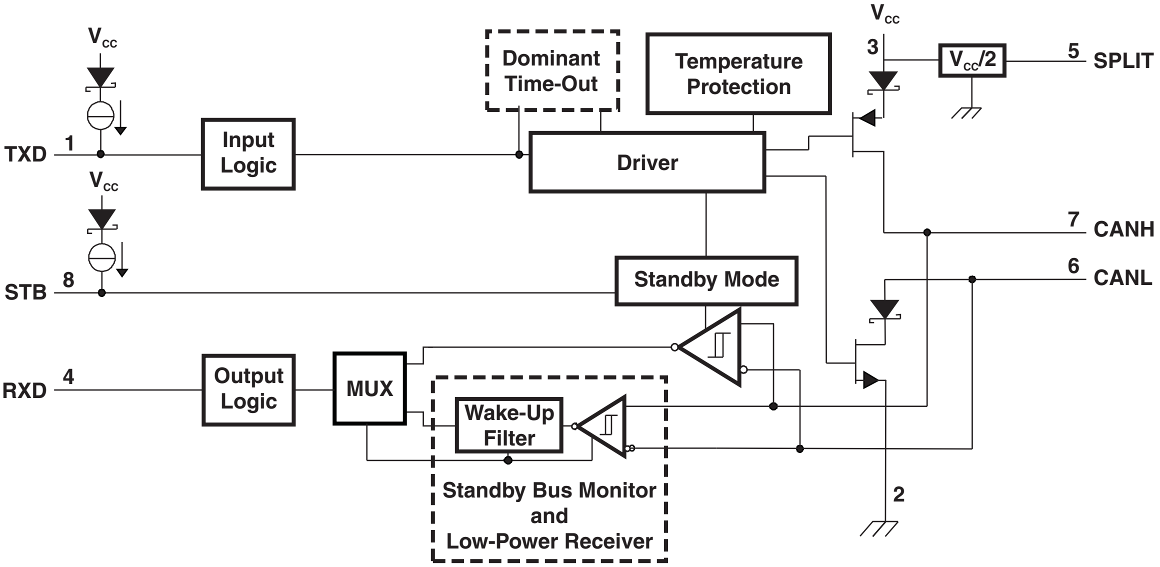
(1) The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

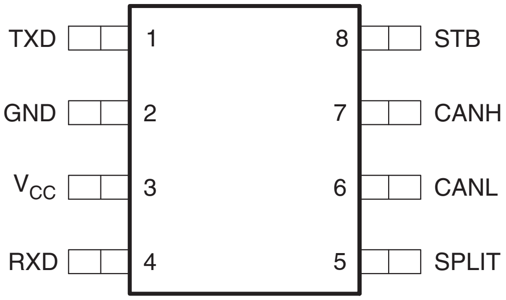
FUNCTIONAL BLOCK DIAGRAM



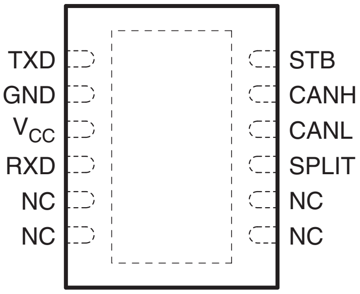
DESCRIPTION (CONTINUED)

The device is designed for operation in especially harsh environments and includes many device protection features such as undervoltage lock out, over temperature thermal shutdown, wide common-mode range and loss of ground protection. The bus pins are also protected against external cross-wiring, shorts to -27 V to 40 V and voltage transients according to ISO 7637.

D PACKAGE
(TOP VIEW)



DSJ PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NAME	SOIC NO.	VSON NO.		
TXD	1	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
GND	2	2	GND	Ground connection
VCC	3	3	Supply	Transceiver 5V supply voltage input
RXD	4	4	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
SPLIT	5	9	O	Common mode stabilization output
CANL	6	10	I/O	LOW-level CAN bus line
CANH	7	11	I/O	HIGH-level CAN bus line
STB	8	12	I	Standby mode select pin (active high)
NC	NA	5, 6, 7, 8	NC	No connect

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	SN65HVDA1040AQDRQ1	A1040A
–40°C to 125°C	VSON – DSJ	Reel of 3000	HVDA1040AQDSJRQ1	A1040A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL DESCRIPTION

Operating Modes

The device has two main operating modes: normal mode and standby mode. Operating mode selection is made via the STB input pin.

Table 1. Operating Modes

STB PIN	MODE	DRIVER	RECEIVER	RXD PIN
LOW	NORMAL	Enabled (On)	Enabled (On)	Mirrors CAN bus
HIGH	STANDBY	Disabled (Off)	Low-power wake-up receiver and bus monitor enabled (On)	Low = wake-up request received High = no wake-up request received

Bus States by Mode

The CAN bus has three valid states during powered operation depending on the mode of the device. In normal mode the bus may be dominant (logic LOW) where the bus lines are driven differentially apart or recessive (logic HIGH) where the bus lines are biased to $V_{CC}/2$ via the high-ohmic internal input resistors R_{IN} of the receiver. The third state is low power standby mode where the bus lines will be biased to GND via the high-ohmic internal input resistors R_{IN} of the receiver.

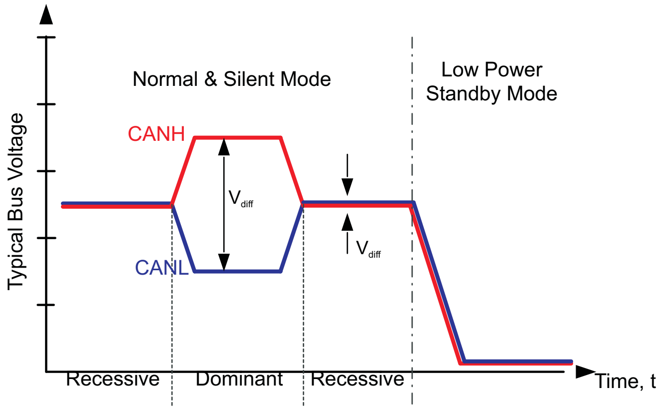


Figure 1. Bus States (Physical Bit Representation)

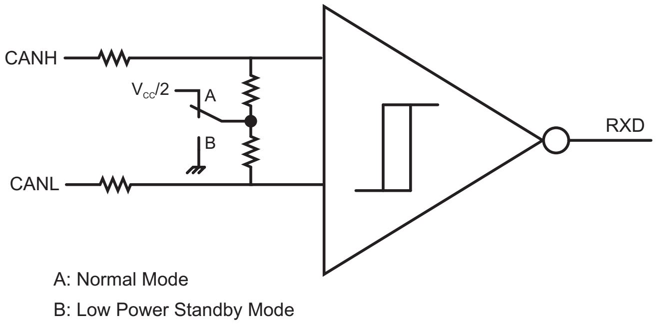


Figure 2. Simplified Common Mode Bias and Receiver Implementation

Normal Mode

This is the normal operating mode of the device. It is selected by setting STB low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state the bus pins are biased to 0.5 × V_{CC}. In dominant state the bus pins (CANH and CANL) are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

The SPLIT pin is biased to 0.5 × V_{CC} for bus common mode bus voltage bias stabilization in split termination network applications (see application information).

Standby Mode and RXD Wake-Up Request

This is the low power mode of the device. It is selected by setting STB high. The CAN driver and main receiver are turned off and bi-directional CAN communication is not possible. The low power receiver and bus monitor are enabled to allow for wake up requests via the bus. A wake up request will be output to RXD (driven low) for any dominant bus transmissions longer than the filter time t_{BUS}. The local protocol controller (MCU) should monitor RXD for transitions and then reactivate the device to normal mode based on the wake up request. The CAN bus pins are weakly pulled to GND and the SPLIT pin is off (floating).

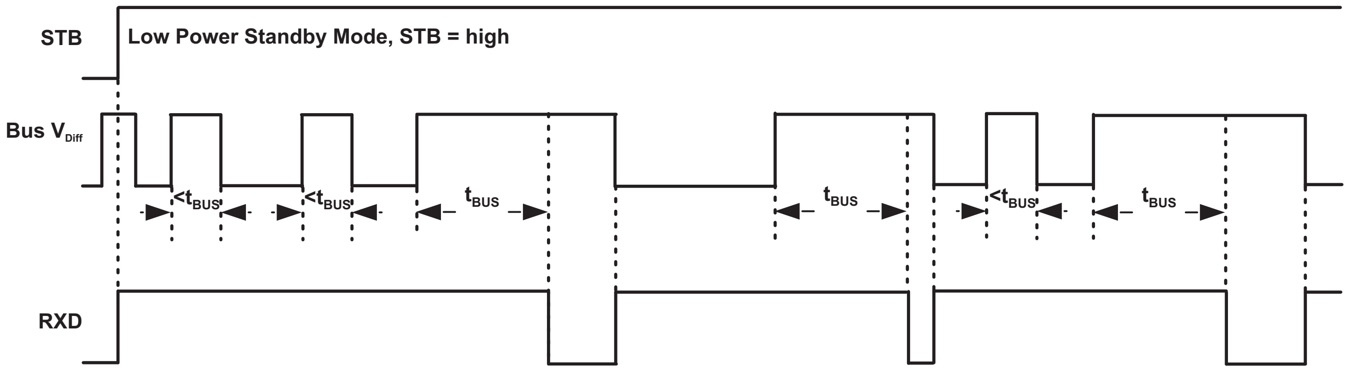


Figure 3. Standby Mode Low Power Receiver and Bus Monitor Behavior

Driver and Receiver Function Tables

Table 2. Driver Function Table[(1)]

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	Dominant
H	L	Z	Z	Recessive
Open	L	Z	Z	Recessive
X	H or Open	Y	Y	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = weak pull down to GND, ? = indeterminate, Z = high impedance

Table 3. Receiver Function Table

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	STB	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9$ V	L	L	Dominant
$V_{ID} \geq 1.15$ V	H or Open	L	Dominant
$0.5 \text{ V} < V_{ID} < 0.9$ V	X	?	?
$V_{ID} \leq 0.5$ V	X	H	Recessive
Open	X	H	Recessive

Protection Features

TXD Dominant State Timeout

During normal mode (only mode where CAN driver is active) the TXD dominant time-out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period t_{DST}. The dominant time out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit expires (t_{DST}) the CAN bus driver is disabled freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on TXD pin, thus clearing the dominant state time out. The CAN bus pins will be biased to recessive level during a TXD dominant state time-out and SPLIT will remain on.

APPLICATION NOTE: The maximum dominant TXD time allowed by the TXD Dominant state time out limits the minimum possible data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t(dom) minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:

Minimum Bit Rate = $11/t_{(dom)}$

Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device will turn off the CAN driver circuits, including SPLIT pin. This condition is cleared once the temperature drops below the thermal shut down temperature of the device.

Undervoltage Lockout / Unpowered Device

The device has undervoltage detection and lockout on the V_{CC} supply. If an undervoltage condition is detected on V_{CC}, the device protects the bus.

The TXD pin is pulled up to V_{CC} to force a recessive input level if the pin floats. The STB is pulled up to V_{CC} to force the device in standby mode (low power) if the pin floats.

The bus pins (CANH, CANL, and SPLIT) all have extremely low leakage currents when the device is un-powered so it will not load down the bus but be an “ideal passive” load to the bus. This is critical, especially if some nodes of the network will be unpowered while the rest of the network remains in operation.

Application Hints

Using With 3.3-V Microcontrollers

The input level threshold for the digital input pins of this device are 3.3V compatible, however a few application considerations must be taken if using this device with 3.3-V microcontrollers. Both TXD and STB input pins have internal pull up sources to V_{CC}. Some microcontroller vendors recommend using an open drain configuration on their I/O pins in this case even though the pullup limits the current. As such care must be taken at the application level that TXD and STB have sufficient pull up to meet system timing requirements for CAN. The internal pullup on TXD especially may not be sufficient to overcome the parasitic capacitances and allow for adequate CAN timing; thus, an additional external pullup may be required. Care should also be taken with the RXD pin of the microcontroller as this device's RXD output drives the full V_{CC} range (5 V). If the microcontroller RXD input pin is not 5-V tolerant, this must be addressed at the application level. Other options include using a CAN transceiver from Texas Instruments with I/O level adapting or a 3.3-V CAN transceiver.

Using SPLIT With Split Termination

The SPLIT pin voltage output provides $0.5 \times V_{CC}$ in normal mode. The circuit may be used by the application to stabilized the common-mode voltage of the bus by connecting it to the center tap of split termination for the CAN network (see Figure 17 and Figure 4). This pin provides a stabilizing recessive voltage drive to offset leakage currents of un-powered transceivers or other bias imbalances that might bring the network common mode voltage away from $0.5 \times V_{CC}$. Utilizing this feature in a CAN network improves electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start of message transmissions.

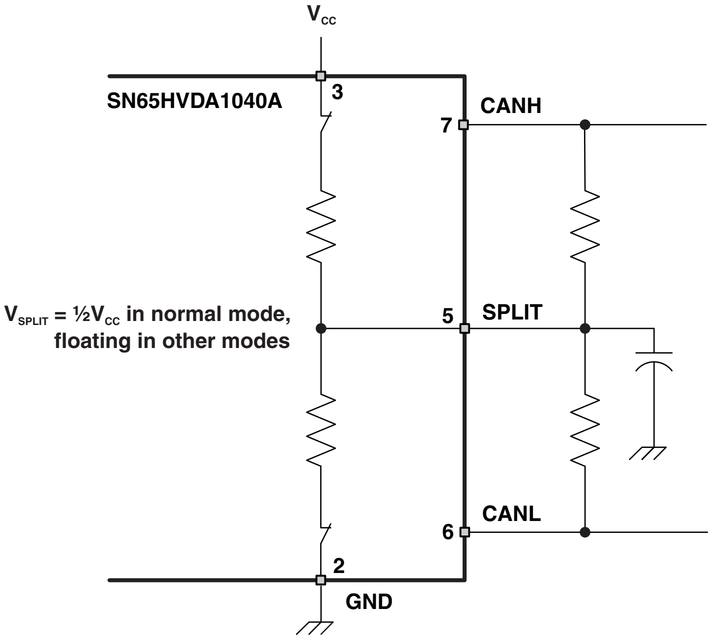


Figure 4. Split Pin Stabilization Circuitry and Application

PCB and Thermal Considerations for VSON Package

The VSON package verson of this device has an exposed thermal pad which should be connected with vias to a thermal plane. Even though this pad is not electrically connected internally it is recommended that the exposed pad be connected to the GND plane. Please refer to the mechanical information on the package at the end of this datasheet and application report SLUA271 "QFN/SON PCB Attachement" for more information on proper use of this package.

ABSOLUTE MAXIMUM RATINGS(1)(2)

1.1	V_{CC}	Supply voltage range	–0.3 V to 6 V
1.2		Voltage range at bus terminals (CANH, CANL, SPLIT)	–27 V to 40 V
1.3	I_O	Receiver output current	20 mA
1.4	V_I	Voltage input range, ISO 7637 transient pulse(3) (CANH, CANL)	–150 V to 100 V
1.5	V_I	Voltage input range (TXD, STB)	–0.3 V to 6 V
1.6	T_J	Junction temperature range	–40°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637 test pulses 1, 2, 3a, 3b per IBEE system level test (Pulse 1 = –100 V, Pulse 2 = 100 V, Pulse 3a = –150 V, Pulse 3b = 100 V). If dc may be coupled with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal. This device has been tested with dc bus shorts to +40 V with leading common-mode chokes. If common-mode chokes are used in the system and the bus lines may be shorted to dc, ensure that the choke type and value in combination with the node termination and shorting voltage either will not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

ELECTROSTATIC DISCHARGE PROTECTION

	PARAMETER	TEST CONDITIONS		VALUE
2.1	Electrostatic discharge(1)	Human-Body Model(2)	CANH and CANL(3)	±12 kV
2.2			SPLIT(4)	±10 kV
2.3			All pins	±4 kV
2.4		Charged-Device Model(5)	All pins	±1.5 kV
2.5		Machine Model(6)		±200 V
2.6		IEC 61000-4-2 according to IBEE CAN EMC test specification	CANH and CANL pins to GND	±7 kV

(1) All typical values at 25°C.
(2) Tested in accordance JEDEC Standard 22 Test Method A114F and AEC-Q100-002.
(3) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
(4) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, SPLIT pin stressed with respect to GND.
(5) Tested in accordance JEDEC Standard 22 Test Method C101D and AEC-Q100-011.
(6) Tested in accordance JEDEC Standard 22 Test Method A115A and AEC-Q100-003.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
3.1	V_{CC}	Supply voltage		4.75	5.25	V
3.2	V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
3.3	V_{IH}	High-level input voltage	TXD, STB	2	5.25	V
3.4	V_{IL}	Low-level input voltage	TXD, STB	0	0.8	V
3.5	V_{ID}	Differential input voltage		–6	6	V
3.6	I_{OH}	High-level output current	Driver	–70		mA
3.7			Receiver (RXD)	–2		
3.8	I_{OL}	Low-level output current	Driver		70	mA
3.9			Receiver (RXD)		2	
3.10	T_A	Operating free-air temperature range	See Thermal Characteristics table	–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

	PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
Supply								
4.1	I_{CC}	5-V supply current	Standby mode	STB at V_{CC}, $V_I = V_{CC}$		6	12	µA
4.2			Dominant	V_I = 0 V, 60-Ω load, STB at 0 V		50	70	mA
4.3			Recessive	$V_I = V_{CC}$, No load, STB at 0 V		6	10	
4.4	UV_{VCC}	Undervoltage reset threshold			2.8		4.0	V
Device Switching Characteristics								
5.1	$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant		STB at 0 V, See Figure 12	90		230	ns
5.2	$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive		STB at 0 V, See Figure 12	90		230	ns
Driver								
6.1	$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 5 and Figure 1	2.9	3.4	4.5	V
6.2			CANL		0.8		1.75	
6.3	$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 5 and Figure 1	2	2.5	3	V
6.4	V_O	Bus output voltage (standby mode)		STB at Vcc, R_L = 60 Ω, See Figure 5 and Figure 1	–0.1		0.1	V
6.5	$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 5, Figure 1, and Figure 6	1.5		3	V
6.6				V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 5, Figure 1, and Figure 6	1.4		3	
6.7	$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 5 and Figure 1	–0.012		0.012	V
6.8				V_I = 3 V, STB at 0 V, No load	–0.5		0.05	
6.9	V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)} + V_{O(CANL)}$)		STB at 0 V, R_L = 60 Ω, See Figure 16	0.9 V_{CC}	V_{CC}	1.1 V_{CC}	V
6.10	$V_{OC(ss)}$	Steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 11	2	2.5	3	V
6.11	$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 11		30		mV
6.12	V_{IH}	High-level input voltage, TXD input			2			V
6.13	V_{IL}	Low-level input voltage, TXD input					0.8	V
6.14	I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	µA
6.15	I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	µA
6.16	$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	µA
6.17	$I_{OS(ss)}$	Short-circuit steady-state output current, Dominant		V_{CANH} = –12 V, CANL open, TXD = low, See Figure 14	–120	–85		mA
6.18				V_{CANH} = 12 V, CANL open, TXD = low, See Figure 14		0.4	1	
6.19				V_{CANL} = –12 V, CANH open, TXD = low, See Figure 14	–1	–0.6		
6.20				V_{CANL} = 12 V, CANH open, TXD = low, See Figure 14		75	120	
6.21				V_{CANH} = 0 V, CANL open, TXD = low, See Figure 14	-100	-75		
6.22				V_{CANL} = 32 V, CANH open, , TXD = low, See Figure 14		75	125	
6.23	$I_{OS(ss)}$	Short-circuit steady-state output current, Recessive		-20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, See Figure 14	-10		10	mA
6.24				-20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, See Figure 14	-10		10	
6.25	C_O	Output capacitance		See receiver input capacitance				

(1) All typical values are at 25°C with a 5-V supply.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Driver Switching Characteristics							
7.1	t_{PLH}	Propagation delay time, low-to-high level output	STB at 0 V, See Figure 7	25	65	120	ns
7.2	t_{PHL}	Propagation delay time, high-to-low level output	STB at 0 V, See Figure 7	25	45	120	ns
7.3	t_r	Differential output signal rise time	STB at 0 V, See Figure 7		25		ns
7.4	t_f	Differential output signal fall time	STB at 0 V, See Figure 7		45		ns
7.5	t_{en}	Enable time from standby mode to normal mode and transmission of dominant	See Figure 10			10	μs
7.6	$t_{(dom)}$	Dominant time out(2)	↓V_I, See Figure 13	300	450	700	μs
Receiver							
8.1	V_{IT+}	Positive-going input threshold voltage, high-speed mode	STB at 0 V, See Table 4		800	900	mV
8.2	$V_{IT–}$	Negative-going input threshold voltage, high-speed mode	STB at 0 V, See Table 4	500	650		mV
8.3	V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)		100	125		mV
8.4	V_{IT}	Input threshold voltage, standby mode	STB at V_{CC}	500		1150	mV
8.5	V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 9	4	4.6		V
8.6	V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 9		0.2	0.4	V
8.7	$I_{I(off)}$	Power-off bus input current (unpowered bus leakage current)	CANH = CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			3	μA
8.8	$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	μA
8.9	C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
8.10	C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		6		pF
8.11	R_{ID}	Differential input resistance	TXD at 3 V, STB at 0 V	30		80	kΩ
8.12	R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, STB at 0 V	15	30	40	kΩ
8.13	$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$	–3	0	3	%
Receiver Switching Characteristics							
9.1	t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V , See Figure 9	60	90	130	ns
9.2	t_{PHL}	Propagation delay time, high-to-low-level output	STB at 0 V , See Figure 9	45	70	130	ns
9.3	t_r	Output signal rise time	STB at 0 V , See Figure 9		8		ns
9.4	t_f	Output signal fall time	STB at 0 V , See Figure 9		8		ns
9.5	t_{BUS}	Dominant time required on bus for wake-up from standby	STB at V_{CC}, See Figure 15	1.5		5	μs
STB Pin							
10.1	V_{IH}	High-level input voltage, STB input		2			V
10.2	V_{IL}	Low-level input voltage, STB input				0.8	V
10.3	I_{IH}	High-level input current	STB at 2 V	–10		0	μA
10.4	I_{IL}	Low-level input current	STB at 0.8 V	–10		0	μA
SPLIT Pin							
11.1	V_O	Output voltage	–500 μA < I_O < 500 μA	0.3 V_{CC}	0.5 V_{CC}	0.7 V_{CC}	V
11.2	$I_{O(stb)}$	Leakage current, standby mode	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	μA

(2) The TXD dominant time out ($t_{(dom)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(dom)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(dom)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:
Minimum Bit Rate = 11/ $t_{(dom)}$ = 11 bits / 300 μs = 37 kbps

THERMAL CHARACTERISTICS

over recommended operating conditions, T_A = –40°C to 125°C (unless otherwise noted)

THERMAL METRIC(1)			TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL METRIC - SOIC 'D' PACKAGE							
12.1-D	θ_{JA}	Junction-to-air thermal resistance(2)	Low-K thermal resistance(3)		140		°C/W
12.2-D			High-K thermal resistance(4)		112		
12.3-D	θ_{JB}	Junction-to-board thermal resistance(5)			50		
12.4-D	$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(6)			56		
12.5-D	$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(7)			NA		
12.6-D	Ψ_{JT}	Junction-to-top characterization parameter(8)			13		
12.7-D	Ψ_{JB}	Junction-to-board characterization parameter(9)			55		
THERMAL METRIC - VSON 'DSJ' PACKAGE							
12.1-DSJ	θ_{JA}	Junction-to-air thermal resistance(2)	Low-K thermal resistance(3)		290		°C/W
12.2-DSJ			High-K thermal resistance(4)		52		
12.3-DSJ	θ_{JB}	Junction-to-board thermal resistance(5)			14		
12.4-DSJ	$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(6)			56		
12.5-DSJ	$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(7)			4.5		
12.6-DSJ	Ψ_{JT}	Junction-to-top characterization parameter(8)			6		
12.7-DSJ	Ψ_{JB}	Junction-to-board characterization parameter(9)			19		
AVERAGE POWER DISSIPATION AND THERMAL SHUTDOWN							
12.5	P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		112		mW
12.6			V_{CC} = 5.5 V, T_J = 130°C, R_L = 45 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			170	
12.7		Thermal shutdown temperature			185		°C

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

(2) The junction temperature (T_J) is calculated using the following $T_J = T_A + (P_D \times \theta_{JA})$. $\theta_{JA}$is PCB dependent, both JEDEC-standard Low-K and High-K values are given as reference points to standardized reference boards.

(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, Low-K board, as specified in JESD51-3, in an environment described in JESD51-2a.

(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(6) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(8) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

(9) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

PARAMETER MEASUREMENT INFORMATION

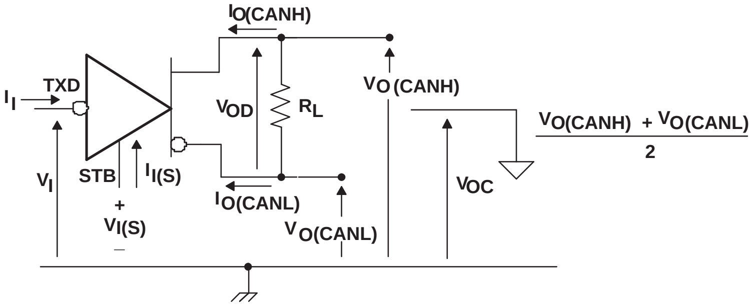


Figure 5. Driver Voltage, Current, and Test Definition

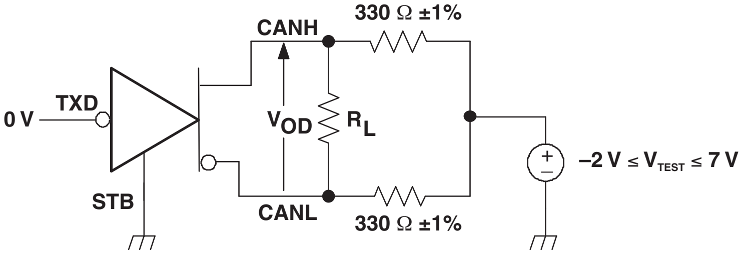


Figure 6. Driver V_{OD} Test Circuit

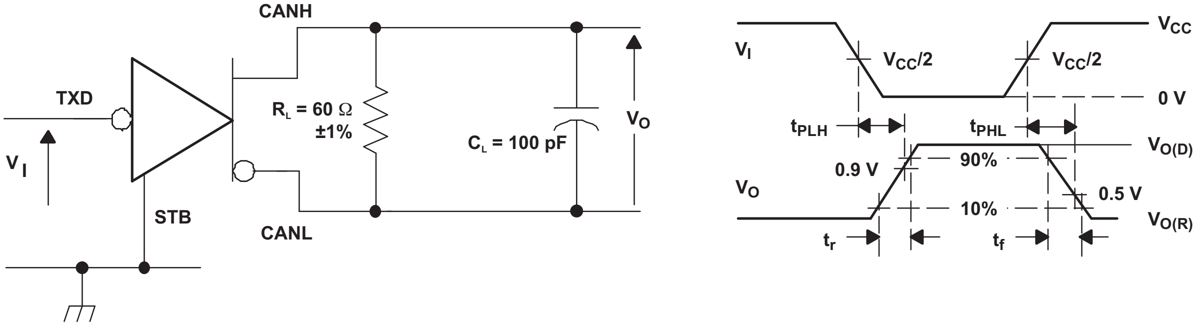


Figure 7. Driver Test Circuit and Voltage Waveforms

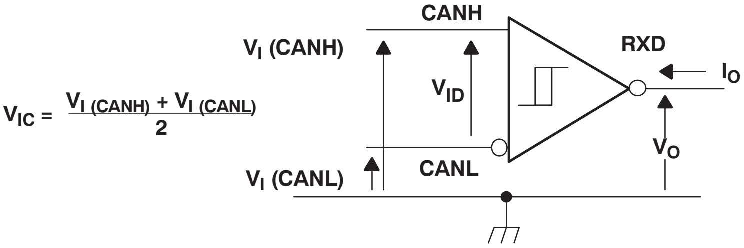
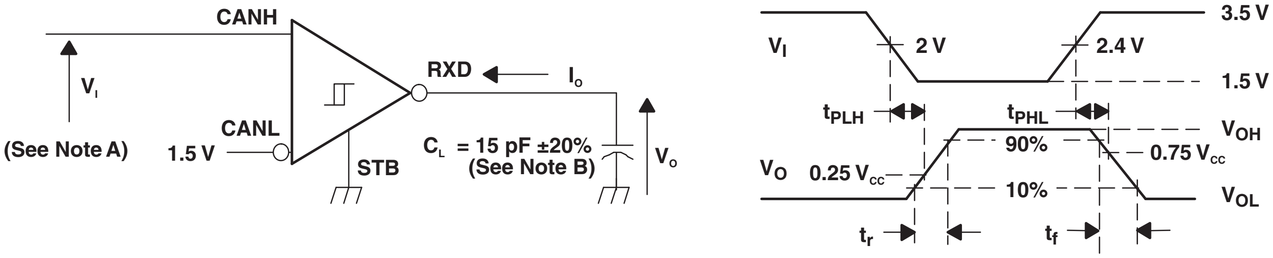


Figure 8. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



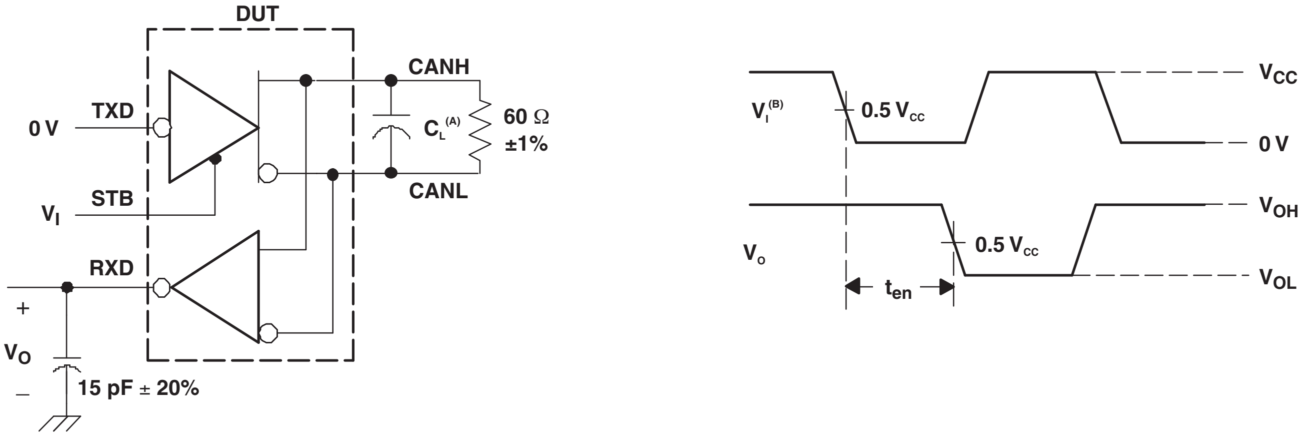
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 9. Receiver Test Circuit and Voltage Waveforms

Table 4. Differential Input Voltage Threshold Test

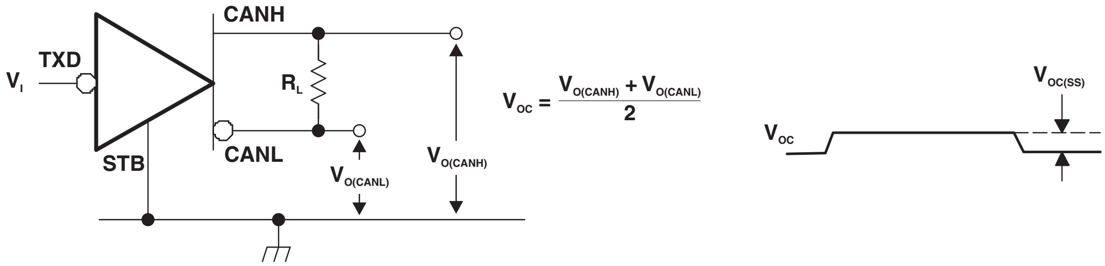
INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID} \rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

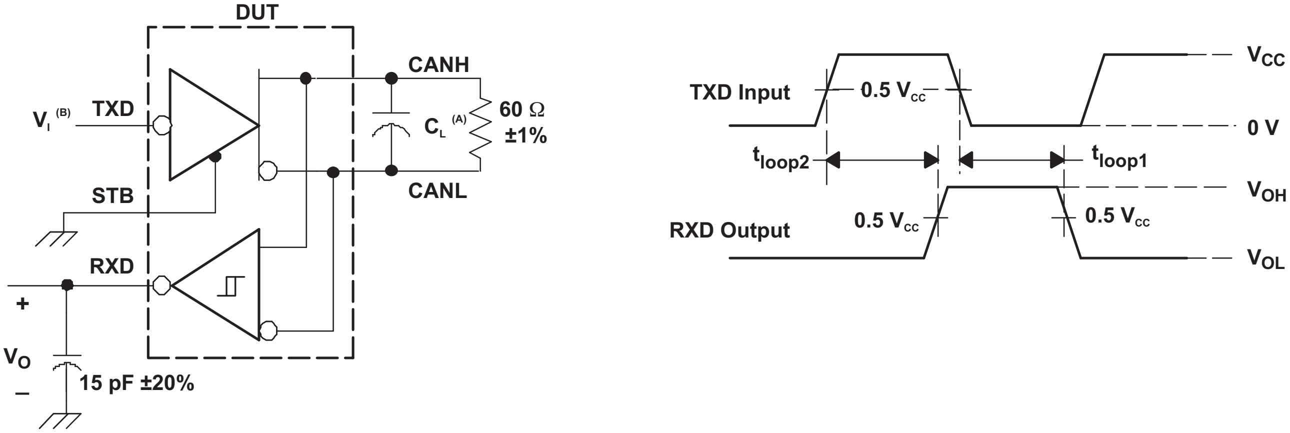
B. All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. t_{en} Test Circuit and Waveforms



NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

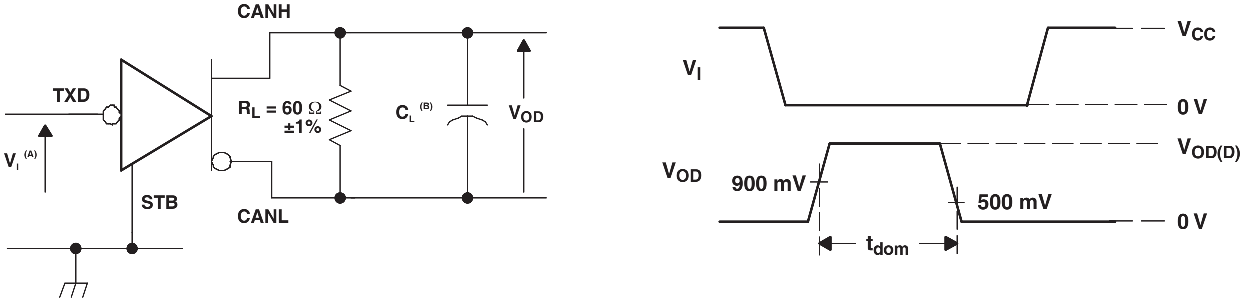
Figure 11. Common-Mode Output Voltage Test and Waveforms



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 12. $t_{(LOOP)}$ Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 13. Dominant Time-Out Test Circuit and Waveforms

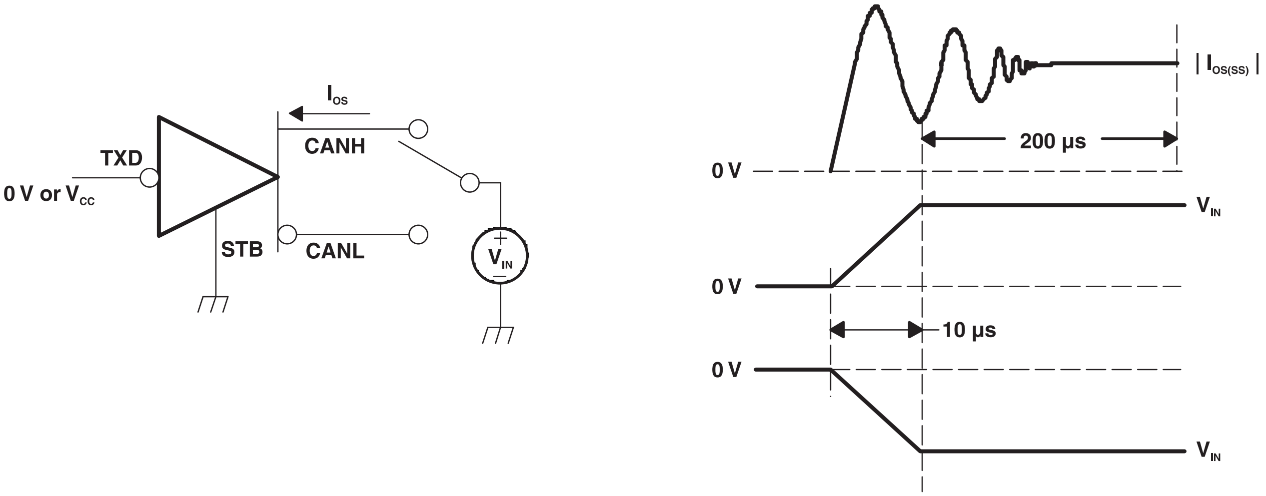
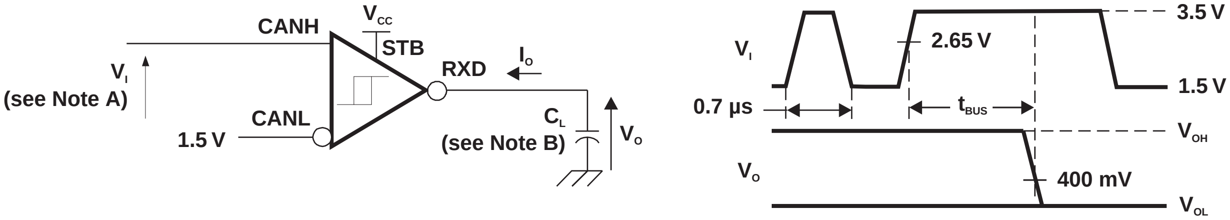


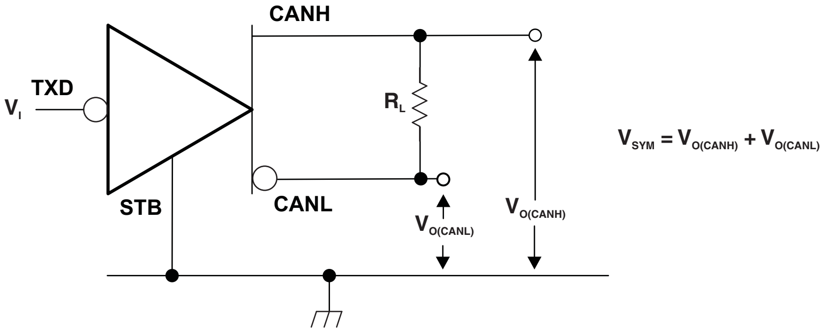
Figure 14. Driver Short-Circuit Current Test and Waveforms



A. For V_I bit width ≤ 0.7 µs, $V_O = V_{OH}$. For V_I bit width ≥ 5 µs, $V_O = V_{OL}$. V_I input pulses are supplied from a generator with the following characteristics: $t_r/t_f < 6$ ns.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

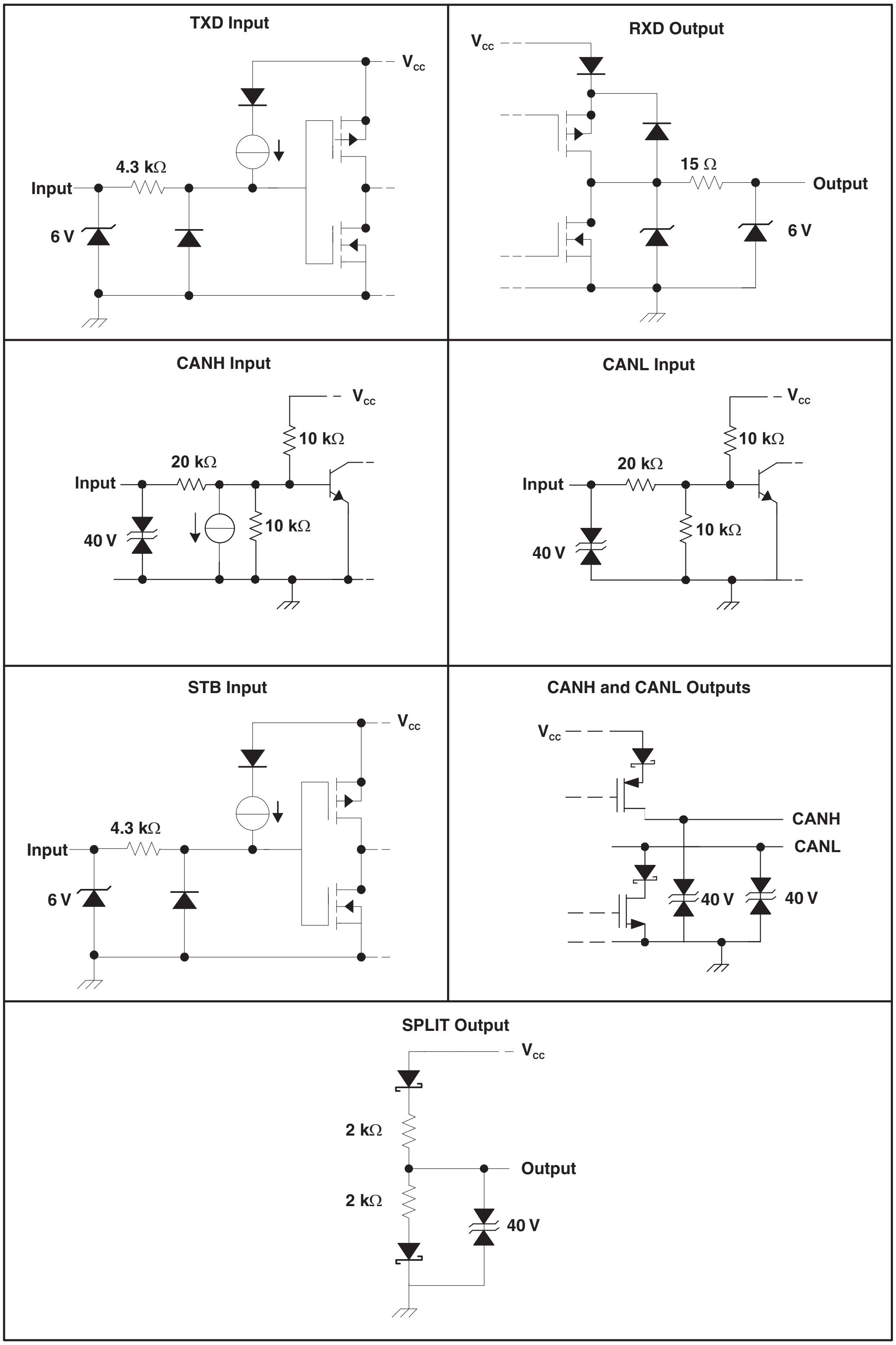
Figure 15. t_{BUS} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: $t_r/t_f \leq 6$ ns, pulse repetition rate (PRR) = 250 kHz, 50% duty cycle.

Figure 16. Driver Output Symmetry Test Circuit

Equivalent Input and Output Schematic Diagrams



APPLICATION INFORMATION

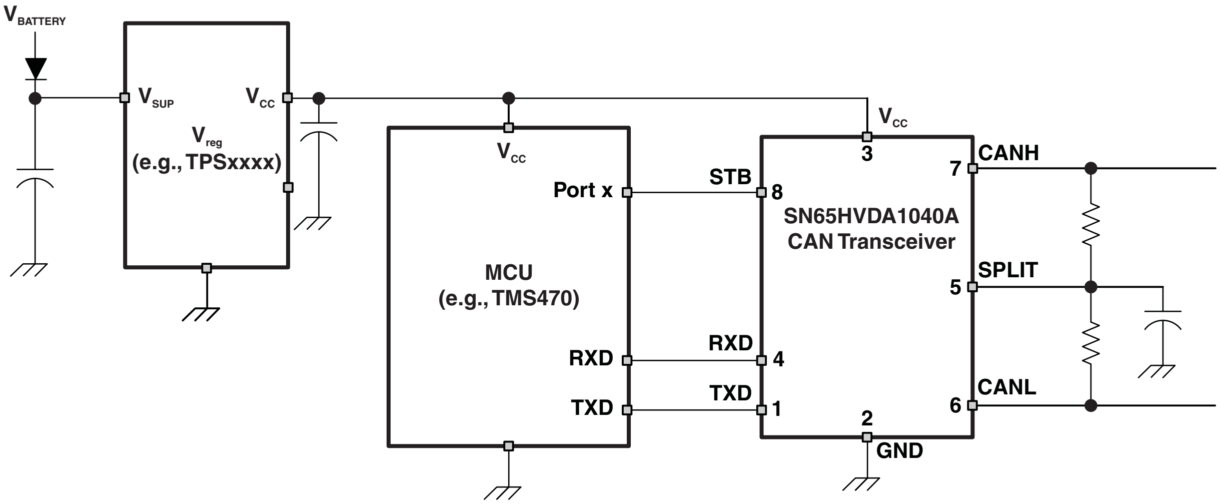


Figure 17. Typical Application Using Split Termination for Stabilization

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
HVDA1040AQDSJRQ1	ACTIVE	VSON	DSJ	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVDA1040AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

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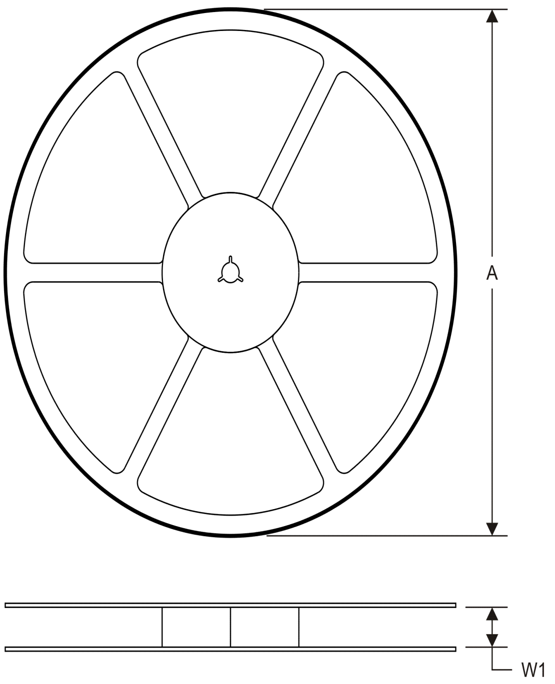
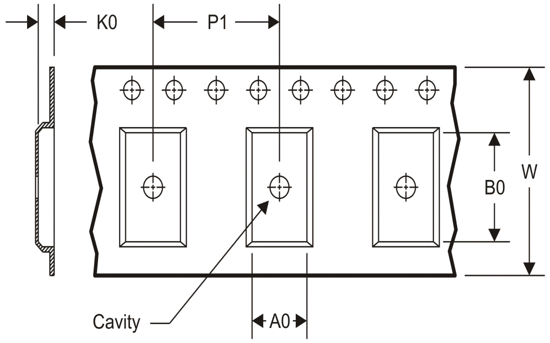


TAPE DIMENSIONS



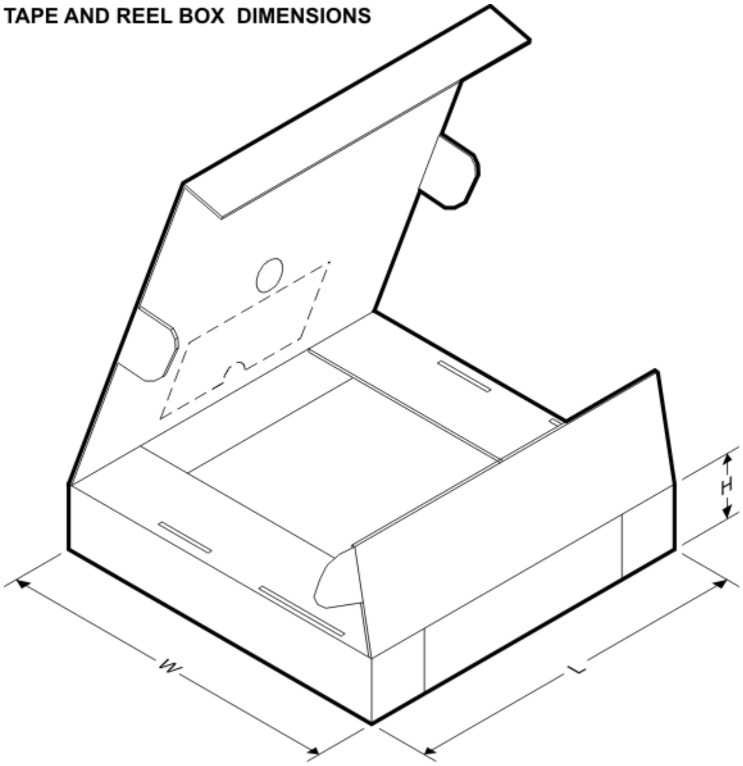
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HVDA1040AQDSJRQ1	VSON	DSJ	12	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1
SN65HVDA1040AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

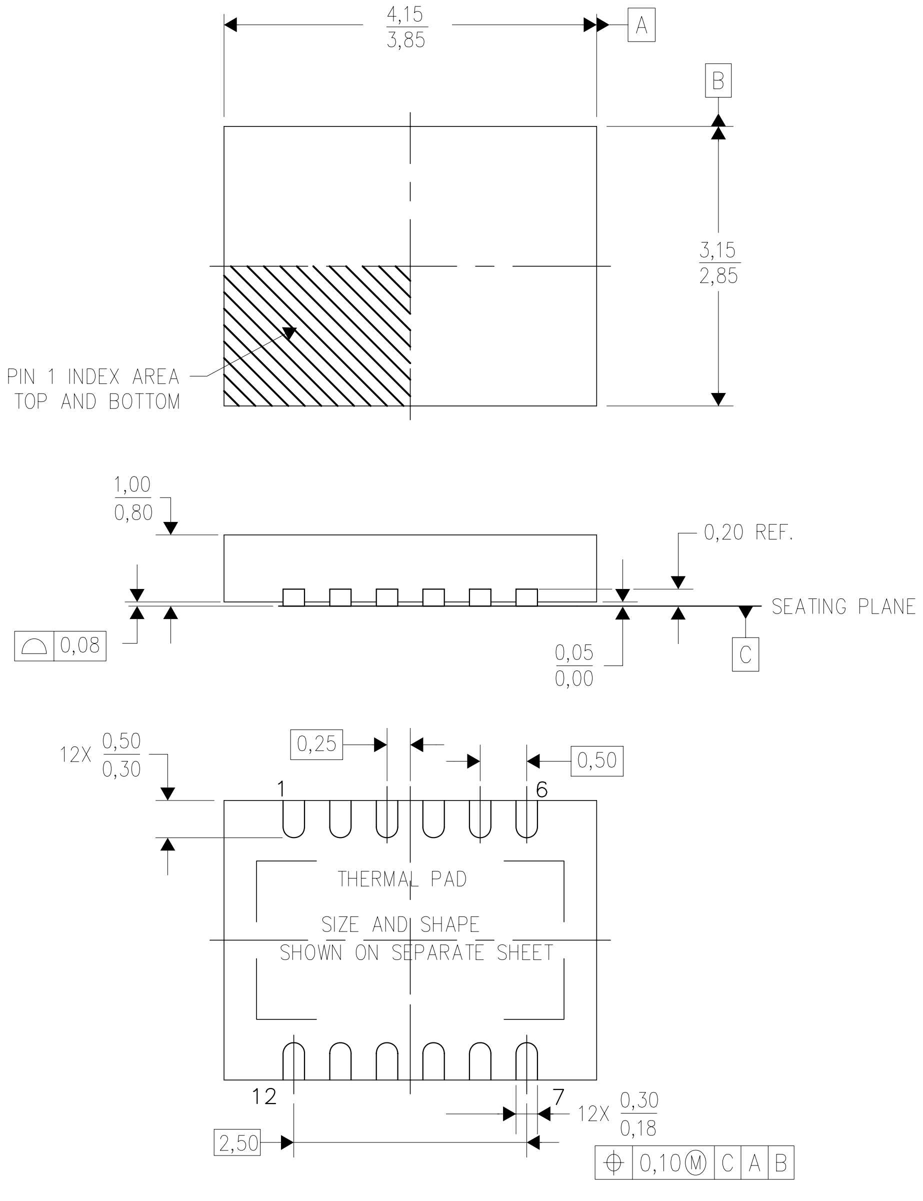
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HVDA1040AQDSJRQ1	VSON	DSJ	12	3000	367.0	367.0	35.0
SN65HVDA1040AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

DSJ (R–PVSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4208212–2/C 06/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–229.

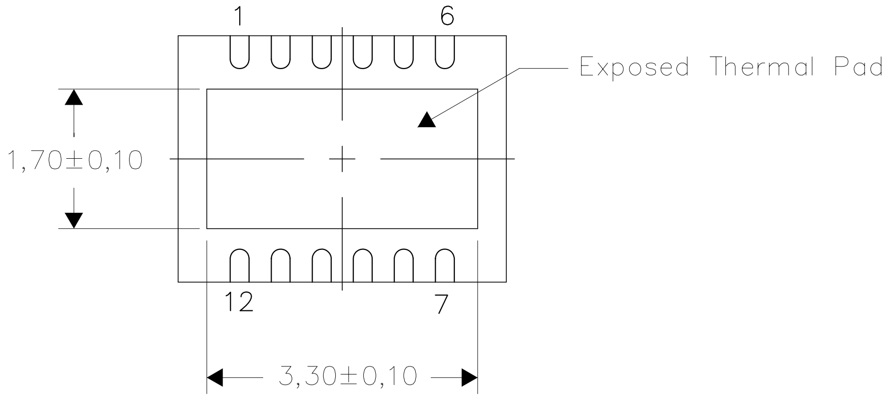
DSJ (R-PVSON-N12) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



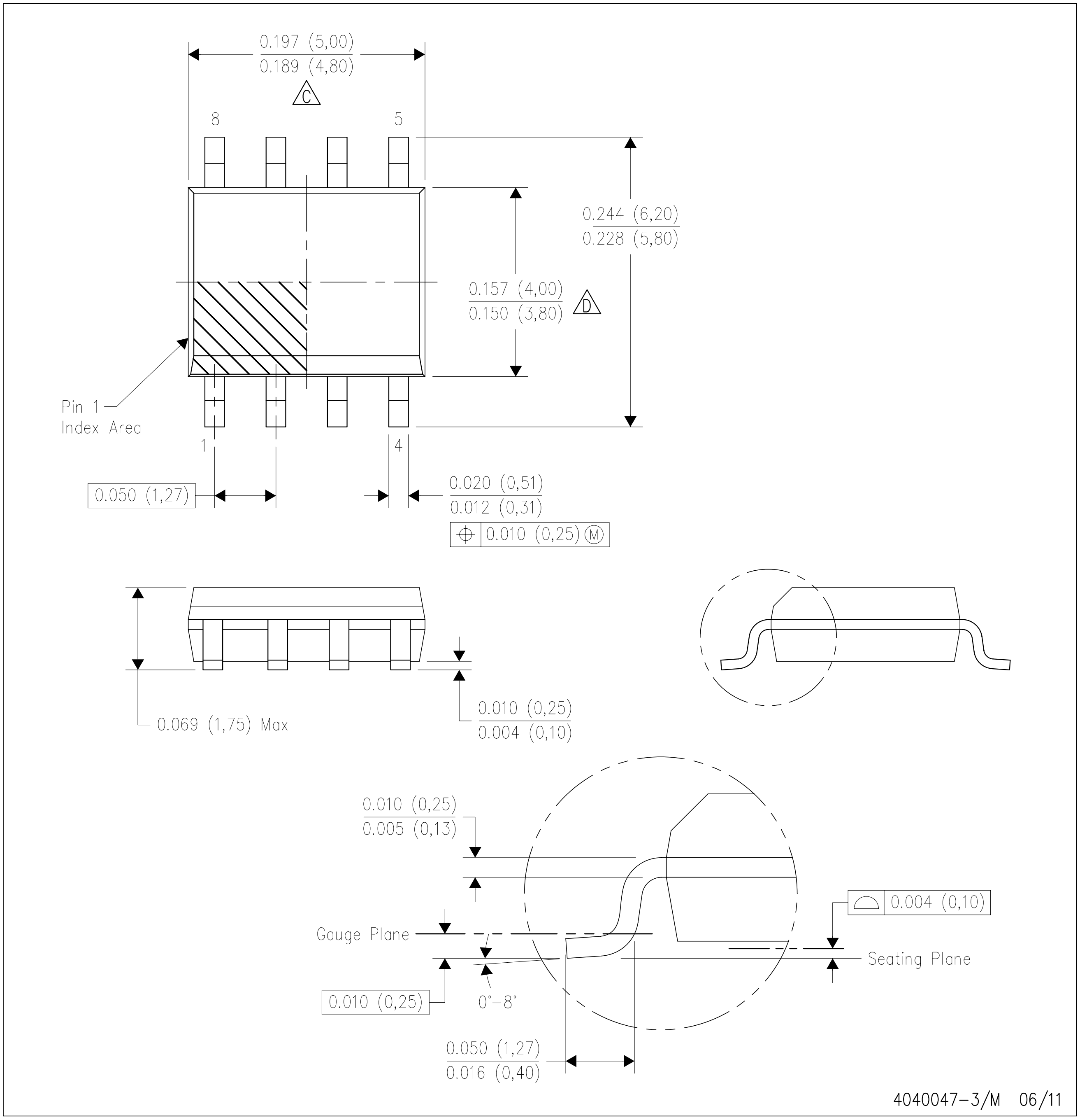
Bottom View

Exposed Thermal Pad Dimensions

4208549-2/E 05/11

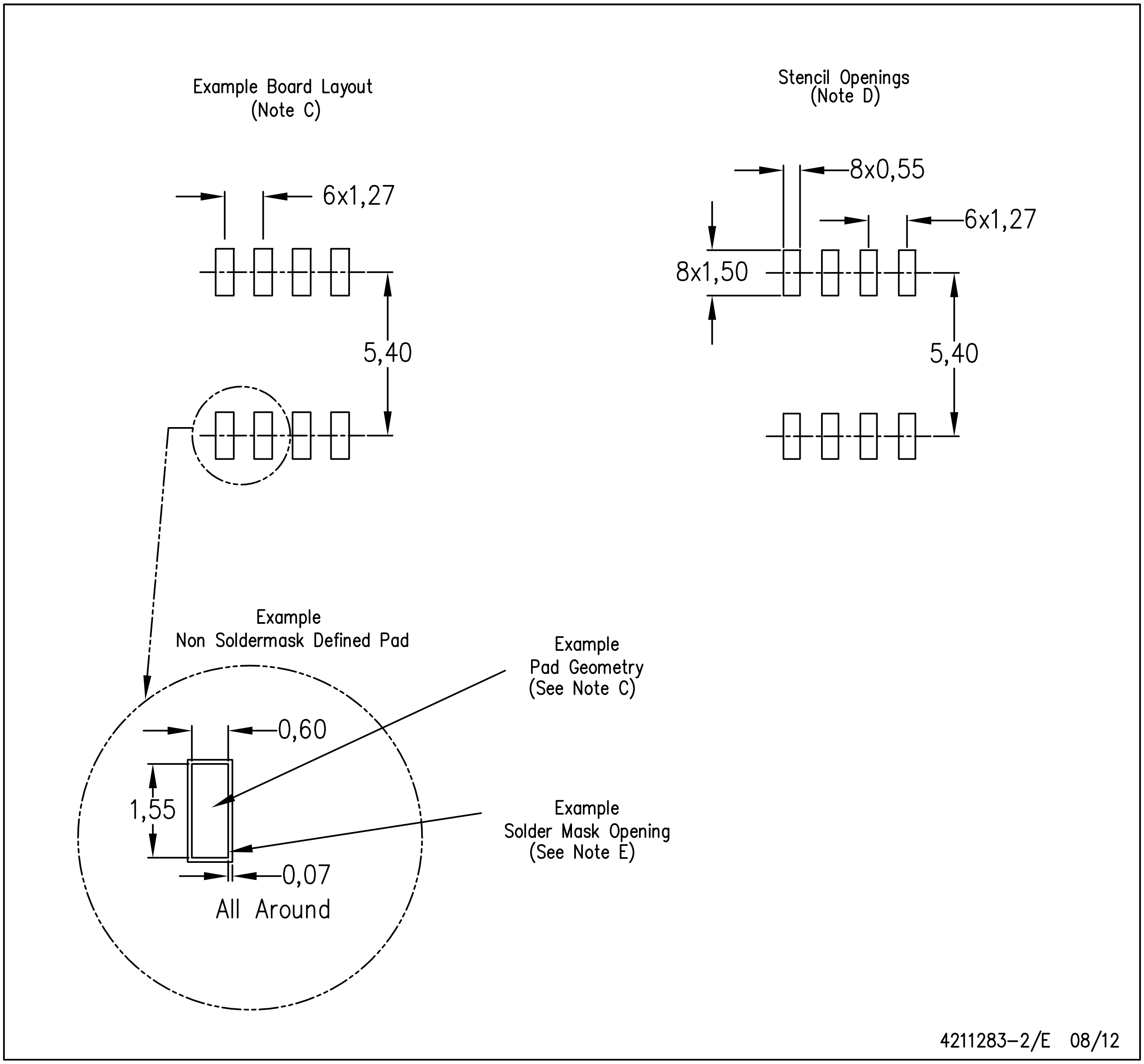
NOTE: All linear dimensions are in millimeters

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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