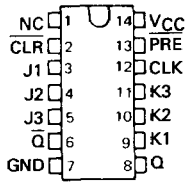
TYPES SN54110, SN74110
AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

REVISED DECEMBER 1983

- **Package Options Include Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54110 . . . J OR W PACKAGE
SN74110 . . . J OR N PACKAGE
(TOP VIEW)



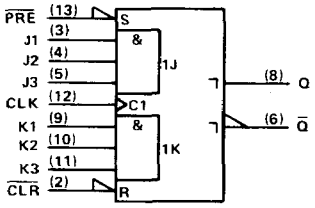
NC – No internal connection

description

The SN54110 and SN74110 are d-c coupled, variable-skew, J-K flips-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled only during a short period (20 nanoseconds maximum setup time plus 5 nanoseconds maximum hold time) on the rising edge of the clock pulse. After this, inputs may be changed while the clock is the at high level without affecting the state of the master. On the threshold level of the falling edge of the clock pulse, the data stored in the master during the rising edge will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptability to noise is thereby effectively reduced.

The SN54110/SN74110 has the same functional advantage as the SN5472/SN7472 in that three-input AND logic is provided for both the J and K data functions. Preset and clear inputs, which are completely independent of the state of the clock, are also provided. The SN54110 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74110 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

positive logic

$J = J1 \cdot J2 \cdot J3$

$K = K1 \cdot K2 \cdot K3$

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⊓	L	L	Q_0	$\bar{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

† This configuration is non-stable; that is, it will not persist when preset or clear return to their inactive (high) level.

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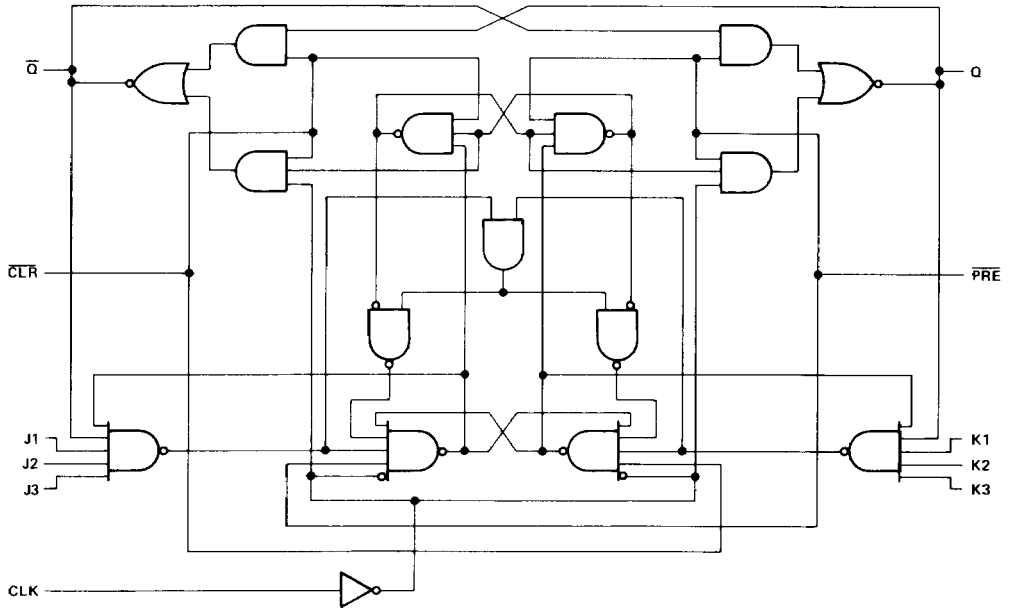
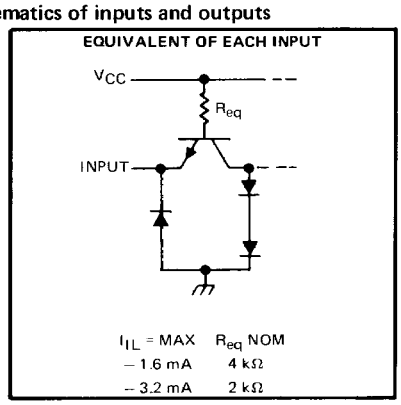
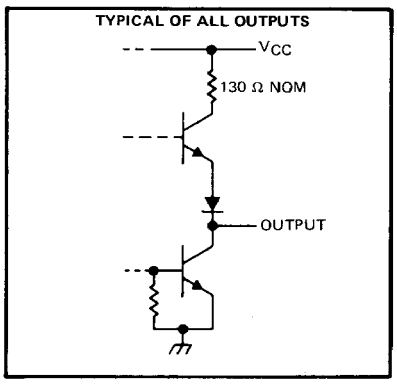
logic diagram



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54110			SN74110			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.8			−0.8	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high or low	25			25			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Input setup time before CLK ↑		20			20			ns
t_h	Input hold time-data after CLK ↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54110			SN74110			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.8 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	J, K or CLK	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
	$\overline{CLR}$ or $\overline{PRE}$						160			160	
	$\overline{PRE}$						160			160	
I_{IL}	J, K or CLK	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
	$\overline{CLR}$★						−3.2			−3.2	
	$\overline{PRE}$★						−3.2			−3.2	
I_{OS}§		V_{CC} = MAX			−20		−57	−18		−57	mA
I_{CC}		V_{CC} = MAX,	See Note 2			20	34		20	34	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
★ Clear is tested with preset high and preset is tested with clear high.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	20	25		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			12	20	ns
t_{PHL}					18	25	ns
t_{PLH}	CLK	Q or $\overline{Q}$			20	30	ns
t_{PHL}					13	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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