

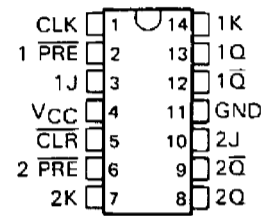
SN54LS78A, SN74LS78A DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

SDLS200

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instrument Quality and Reliability

SN54LS78A . . . J OR W PACKAGE
SN74LS78A . . . D OR N PACKAGE
(TOP VIEW)



description

The 'LS78A contains two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and k inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. The preset and clear are asynchronous active-low inputs. When low they override the clock and data inputs forcing the outputs to the steady-state levels as shown in the function table.

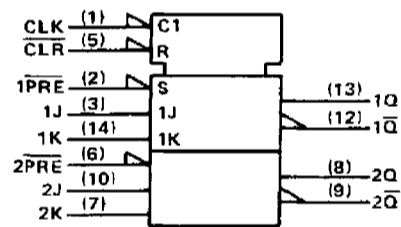
The SN54LS78A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS78A is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [‡]	H [‡]
H	H	↓	L	L	Q ₀	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	\bar{Q}_0

[‡]This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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SN54LS78A, SN74LS78A
DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

recommended operating conditions

		SN54LS78A			SN74LS78A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.75	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.7			0.8			V
I _{OH}	High-level output current	-0.4			-0.4			mA
I _{OL}	Low-level output current	4			8			mA
f _{clock}	Clock frequency	0			30			MHz
t _w	Pulse duration	CLK high		20		20		ns
		PRE or CLR low		25		25		
t _{su}	Setup time before CLK ↓	data high or low		20		20		ns
		PRE or CLR inactive		20		20		
t _h	Hold time-data after CLK ↓	0			0			ns
T _A	Operating free-air temperature	-65			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS78A		SN74LS78A		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.5		-1.5		V	
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.7 V, I _{OH} = -0.4 mA	2.5	3.4			V	
	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.4 mA			2.7	3.4		
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA	0.25	0.4	0.25 0.4		V	
	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA			0.35	0.5		
I _I	V _{CC} = MAX, V _I = 7 V	J or K	0.1		0.1		mA
		CLR	0.6		0.6		
		PRE	0.3		0.3		
		CLK	0.8		0.8		
I _{IH}	V _{CC} = MAX, V _I = 2.7 V	J or K	20		20		μA
		CLR	120		120		
		PRE	60		60		
		CLK	160		160		
I _{IL}	V _{CC} = MAX, V _I = 0.4 V	J or K	-0.4		-0.4		mA
		CLR	-1.6		-1.6		
		PRE	-0.8		-0.8		
		CLK	-1.6		-1.6		
I _{OS} §	V _{CC} = MAX, See Note 4	-20	-100	-20	-100	mA	
I _{CC} (Total)	V _{CC} = MAX, See Note 2	4	6	4	6	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

SN54LS78A, SN74LS78A
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				30	45		MHz
t_{PLH}	PRE, CLR or CLK	Q or \bar{Q}	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$		15	20	ns
t_{PHL}					15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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