DM7488(SN7488) 256-bit read only memory

general description

Large-scale integration and programming in the wafer stage of processing make this TTL high-performance ROM economical in applications such as table lookup, subroutine storage and random logic synthesis. The 256 bits are organized as 32 8-bit words. Other features are:

- On-chip decoding of 5-bit address
- Open-collector outputs for expansion to greater number of words
- Typical access time of 30 ns
- Overriding strobe input
- Input clamp diodes
- TTL and DTL compatible
- Typical power dissipation only 240 mW.

ROM expansion method

Word length may be expanded to n bits by operating several ROMs in parallel. The number of words may be expanded by wire-AND connecting the outputs, using pullup resistors connected to V_{CC} to define the "1" logic level. Chip-enable signals may be obtained from active-low TTL decoders addressed by the higher-order address bits. The strobe input enables an output if taken to the logical "0" level. All outputs are held high if the strobe input is high.

A tri-state replacement, the DM7598/DM8598 has been developed for applications where open-collector performance or pullup resistors are undesirable. It is expandable to 32,768 bits in word lengths from 8 bits to 1024 bits.

programming

Programming is ordered by filling in a truth table. The table is used to make changes in the metallization mask determining the storage transistor functions.

connection diagram